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ORIGINAL ARTICLE

Low Power 8T and 9T SRAM Cell Configurations using Improved SVL (I-SVL)

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Abstract

Background/Objectives: Memory is important in today's world of electronic equipment, such as processors and portable electronics, thanks to the use of static random-access memory (SRAM). Low-power electronic devices, such as PDAs and cell phones, are the goal of the current generation. Consequently, the design of low power SRAM has a vast array of uses. However, the SRAM design adds a higher power requirement. Therefore, there is still opportunity to develop an appropriate low-power memory cell. The implementation of low power reduction solutions satisfies this urgent demand. Additionally, these devices require cache memories, which are created using Static Random Access Memory cells (SRAMs). Using power reduction strategies to create SRAM cells with low leakage is now a difficulty. **Methods**: In the present context the designing and implementation of low power 8T and 9T SRAM cells has been carried using SVL and I-SVL techniques for various process corner models. The simulation has been carried using Microwind DSCH (version 3.5) and all simulations are carried out using Microwind version 3.1 with 90 nm technology library at 1.2 V of Vdd. **Findings**: The proposed 8T I-SVL based cells shows improvements in power by 18% and 69% using BSIM 4 in comparison with the Level 3 and Level 1 models respectively. The proposed 9T I-SVL based cells shows improvements in power by 30% and 1.8% using Level 3 in comparison with the Level 1 and BSIM 4 models respectively. **Novelty**: This study proposes Low power 8T and 9T based SRAM cells in terms of static and dynamic power in comparison with the existing literatures through the usage of I-SVL techniques. In addition, the proposed I-SVL 8T and 9T SRAM cell shows 52% and 68% improvements in terms of total power comparatively with the existing works.

Keywords: SRAM; Improved – Self Controllable Voltage level (I-SVL); Improved lower SVL (I-LSVL); Improved upper SVL (I-USVL); Self Controllable Voltage level (SVL)

1 Introduction

SRAMs, which are fast and low power, are now a distinguishing feature of every VLSI processor. This is always true for all the microchips, whose on-chip reserved volumes are drastically growing with passing generation to cover the widening gap between processors and cache memories rate. SRAM generally meant as high-speed cache memory to enhance the speed of processor and memory interface assignment. The operational speed of logic gates has enhanced significantly due to advanced VLSI innovation technologies, yet memory-operating speed is to be improved. SRAM cache memories are essential with the increasing operational speed in high-speed PCs, while Dynamic RAM used as a component of main memory, where density is more important than speed.

Widespread applications of VLSI technology may be found in a wide range of electronic devices, from basic mobile phones to smartphones, GPS positioning systems, and defense systems. The majority of these applications rely on memories as an essential component to carry out various tasks and store data when needed. Many types of memory can be utilized for different purposes and can have either temporary or permanent storage with either static or dynamic operations. Each year, new circuits and technologies are created, and while many memory types eventually become obsolete, SRAM is used in sophisticated microprocessors.

SRAM is more durable and faster. SRAM does not require periodic refreshes, in contrast to DRAM, which stores information in cells made of capacitors and transistors. While DRAM enables higher access periods than SRAM that provide shorter access times for faster access of data. SRAM is utilized in low power electronics applications for both primary memory and computer cache memory. Two inverters, each storing data in opposite polarity, make up SRAM. To manage the writing and reading processes in a single cell, more MOSFETs must be used. Numerous SRAM cell versions, such as 6 transistors (6T), 7T, 8T, and others, have been proposed thus far. On-chip memory cells use high-performance arrays of SRAM cells. The traditional six transistor SRAM (6T SRAM cell) that is used takes up more space than a DRAM cell, however SRAM cells do not require continuous bit monitoring.

Work[(1)] is about 8T SRAM design based on CNTFET cell and by the addition of positive feedback, control leakage has been resulted. The usage of carbon nanotube field-effect transistor (CNTFET) within the design has been resulted in low power consumption and higher current drive capabilities in comparison with the silicon-based transistors. The proposed work has been implemented through Positive feedback control (PFC), Positive power supply controlled (PPC) based transistors with the adoption of Synopsys Hspice. Work[(2)] reviews older SRAM cell proposals for exhibiting improvements in cell parameters of power, delay, leakage power, read and write stability. Five SRAM cell geometries, including the conventional 6T and 9T SRAM cell executions, are examined in this research. Particularly, each SRAM cell's read conduct, spillage fluxes, and spill force are examined. The most territory-productive SRAMs are the standard 6T, 7T, and 8T models, which also have the lowest transistor count[(3)].

For a range of frequencies, dynamic power is computed and contrasted with that of the typical SRAM 6T cell. With this suggested approach, the new SRAM cell could be used to provide low-power consumption for high-speed devices such as smartphones, laptops, programmable logic devices, and so on. The models' results indicate that the projected SRAM model's frequency will also rise while the facility dissipation remains nearly constant. With the prime frequency, SRAM CMOS cell arrangement, this guarantees less energy dissipation[(4)]. An enhanced single ended PPN inverter-based 10T SRAM cell is presented in this work. The suggested cell uses PPN-inverters as a method. In the traditional 8T SRAM cell, the PPN-inverter takes the place of the CMOS inverter to create an enhanced single-ended PPN-based 10T SRAM cell. Results of the suggested work is evaluated against other SRAM cells in terms of power dissipation, delay, and power delay product (PDP). The proposed cell is optimized in terms of power dissipation making it more efficient for use in portable battery-operated devices[(5)].

Numerous Static RAM cell architectures with 45nm technologies were simulated through the Tanner tool. In each configuration, simulation parameters like read & write latency, power consumption, and static noise margin (SNM) were evaluated. Out of those design configurations, the 7T based SRAM cell stands out through the lowest power consumption. Nevertheless, comparison through the 6T based SRAM cell, the 8T based SRAM cell configuration exhibited 44.15% power reduction during write operation. The 9T based SRAM configuration resulted with the lowest latency during write operation of all the cells implemented. Among the various simulated configurations, the conventional 6T based SRAM cell showed the larger RSNM value[(6)]. To overcome lacunas of 6T based SRAM cell, researchers have proposed various SRAM cell topologies such as 8T, 9T, 10T etc. bit cell design. These designs are meant in improving the cell stability, but they suffer in terms of leakage noise. Work[(7)] is about the designing a Static RAM memory that overcomes power consumption overhead. The proposed configuration shows improvements in terms of Cell stability through higher RSNM. The 7T based SRAM design was implemented through usage of SVL, I-SVL and MTCMOS techniques.

The leakage power analysis was carried using above said methods and detail comparative analysis are depicted in work[(8)] and[(9)]. Work[(10)] depicts the simulation of memory design through the usage of 6T and 10T SRAM cell based on CMOS and Fin

FET technologies. Various power reduction techniques have been applied for the proposed cells which shows improvements in SNM in comparison to the conventional SRAM cells. Work[11] is about proposing 10T CNTFET SRAM Cell design with the usage of Stable Feedback cutting technology. The proposed design FCPPN10T shows improvements in noise margin during Read and Write operations in comparison to 6T based SRAM Cell. The proposed work also shows improvements in delay and leakage power in comparison with the conventional 67 SRAM cell design. The proposed work has been simulated using Cadence Virtuoso at 32nm technology node. Work[12] proposes low power FINFET based 11T SRAM cell design. The proposed cell shows improvements in reduction of overall power consumption in comparison to conventional 6T SRAM Cell. The proposed 11T based cell also comes with the enhancements in terms of noise margin.

When feature sizes are small and the power supply is low, the traditional 6T SRAM cell exhibits poor stability. It uses a lot of power as well. The voltage division between the access and driver transistors significantly reduces stability during read operation. Write disturbance, which can happen when writing new data and may result in unwanted changes to the stored value because of bit line contention or weak access transistors, is one of the main problems with 7T SRAM cells. Some of the intrinsic problems with the conventional 6T and 7T SRAM cells were addressed by the design of the 8T and 9T SRAM cells. The power consumption of these sophisticated SRAM cell designs is all improved through the usage of Power Reduction techniques. The flow of current work is carried through various sub sections like Introduction, Literature survey, Existing and Proposed cell configuration, Results and discussions followed by conclusion.

2 Methodology

The performance and dependability of conventional 6T SRAM cells are improved by the 8T SRAM cell design, especially with regard to read and write stability. A read operation can disrupt the stored data in traditional 6T SRAM cells because the read and write operations are connected, particularly in noisy or low-voltage settings. An extra transistor that divides the read and write pathways is used by the 8T SRAM cell to get around this restriction. By guaranteeing that read operations don't alter the data that has been stored, this design greatly increases read stability and lowers the possibility of read disturbance. More dependable data writes are made possible by the additional transistor's improved write stability.

Compared to the 8T architecture, the 9T SRAM cell adds a transistor to enhance read reliability and write stability. Compared to previous SRAM designs, the 9T SRAM's use of a differential read mechanism, which enables more robust data preservation and less read disturbance, is one of its primary characteristics. Additionally, the additional transistor helps regulate the write assist, which guarantees more dependable data writing even at low voltages.

2.1 Proposed SRAM Cell configuration

A chip's architecture becomes more complex as the number of transistors it contains rises. These power consumption factors have an impact on stability, area, noise margins, and operating speed. It is also necessary to take some action regarding them. Among these, leakage power has the greatest impact because transistor leakage current accounts for 40% or more of the overall power usage. The processor's performance is limited by this leakage current. Reducing this leakage current is the primary goal, as it lowers the cell's overall power consumption. There are several different ways that power can be dissipated, including sub-threshold leakage, dynamic leakage, and gate leakage.

The "Self-Controllable Voltage Level Technique" (SVL technique) is employed in the current research work to lower transistor leakage current, which lowers the SRAM cell's overall leakage power consumption. To attain this low power consumption, the "Self-Controllable Voltage Level Technique," also known as the "SVL Technique," the "Improved SVL technique," also known as the "ISVL Technique," are employed, which further minimizes leakage power to optimize the system.

Figure 1 and 2 are the schematic and layouts for the Proposed 8T and 9T SRAM Cell Configurations using UL-SVL Method. Single n-MOS and p-MOS transistors coupled in series make up the Upper-SVL circuit connected on the top of the basic SRAM cell. Both N-MOS and P-MOS transistors accept an enable signal as input to their gates. P-MOS is activated, and N-MOS is deactivated when enable is low. In similar manner, Single n-MOS and p-MOS transistors coupled in series make up the Lower-SVL circuit connected towards the bottom of the basic SRAM cell.

Figure 3 and 4 depict the proposed 8T and 9T SRAM cell configurations employing Improved SVL technique (UL-ISVL).

3 Results and discussion

Various parameters like leakage power consumption in turns of static power consumption, and dynamic power consumption, Delay are analyzed and exhibited in the form of comparison tables. All schematics are drawn in Microwind DSCH (version 3.5), and all simulations are carried out using Microwind version 3.1 with 90 nm technology library at 1.2 V of Vdd. Transient

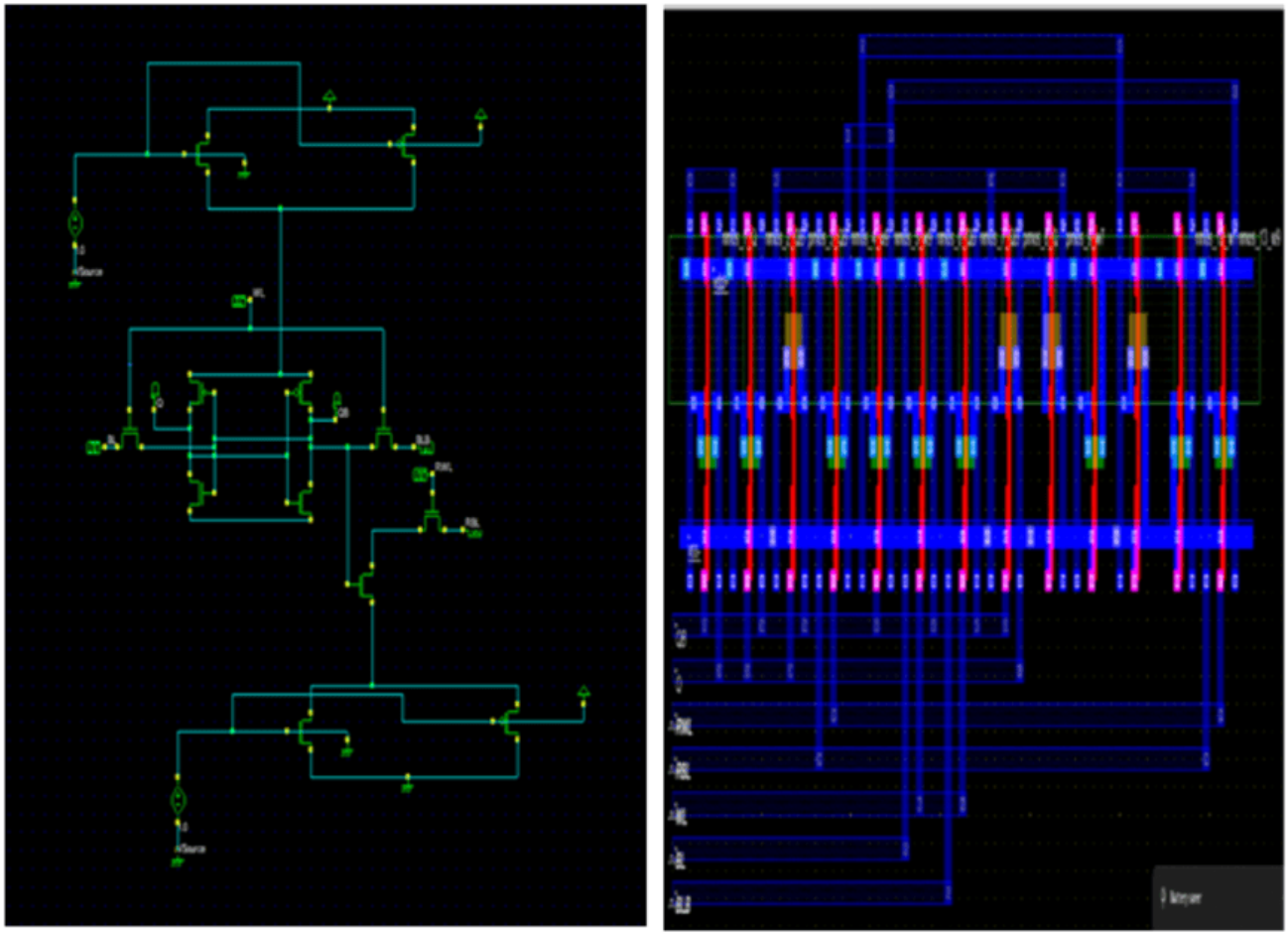

Fig 1. Proposed Schematic and Layout of 8T SRAM Cell configuration employing UL-SVL (SVL)

analysis is carried out for transient time of 100ns. In Microwind software, "Process Corners" refer to the different variations in manufacturing parameters that can affect the performance of a designed circuit, allowing users to simulate how their design will behave under different manufacturing conditions, including extreme variations in critical parameters like transistor threshold voltage and carrier mobility, essentially simulating the "best case" and "worst case" scenarios for the circuit's functionality.

Level 1: In VLSI (Very Large-Scale Integration) design, the terms VTO, UO, TOX, PHI, and GAMMA are model parameters used to describe the behavior of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). These parameters are primarily related to the transistor's operation and are critical for device modeling and circuit simulation. **Level 3:** A semi-empirical model that strikes a balance between computational efficiency and accuracy is the Level 3 model. These parameters enable the model to take into consideration body effect, velocity saturation, mobility degradation, and short-channel effects—all of which are crucial for the behavior of contemporary transistors. They help designers optimize circuits for speed, power, and dependability by predicting MOSFET behavior under various operating conditions using simulation tools**. BSIM 4:** The physical, electrical, and process properties of transistors are represented by these parameters in Berkeley Short-Channel IGFET Model 4, or BSIM4, a popular MOSFET model for circuit simulations. With its sophisticated characteristics, BSIM4 can accurately model current CMOS technologies, including mobility deterioration, short-channel effects, and others.

The power analysis is carried for static, dynamic and total power analysis using 90nm technology with different process corners like Level 1, Level 3 and BSIM 4 Models. The above said power analysis has been carried for Basic cells of 8T, 9T and SVL, ISVL Versions of 8T, 9T optimized SRAM cells. The detail power analysis has been exhibited for various transistor sizing using different process corner models of Level 1, Level 3 and BSIM 4.

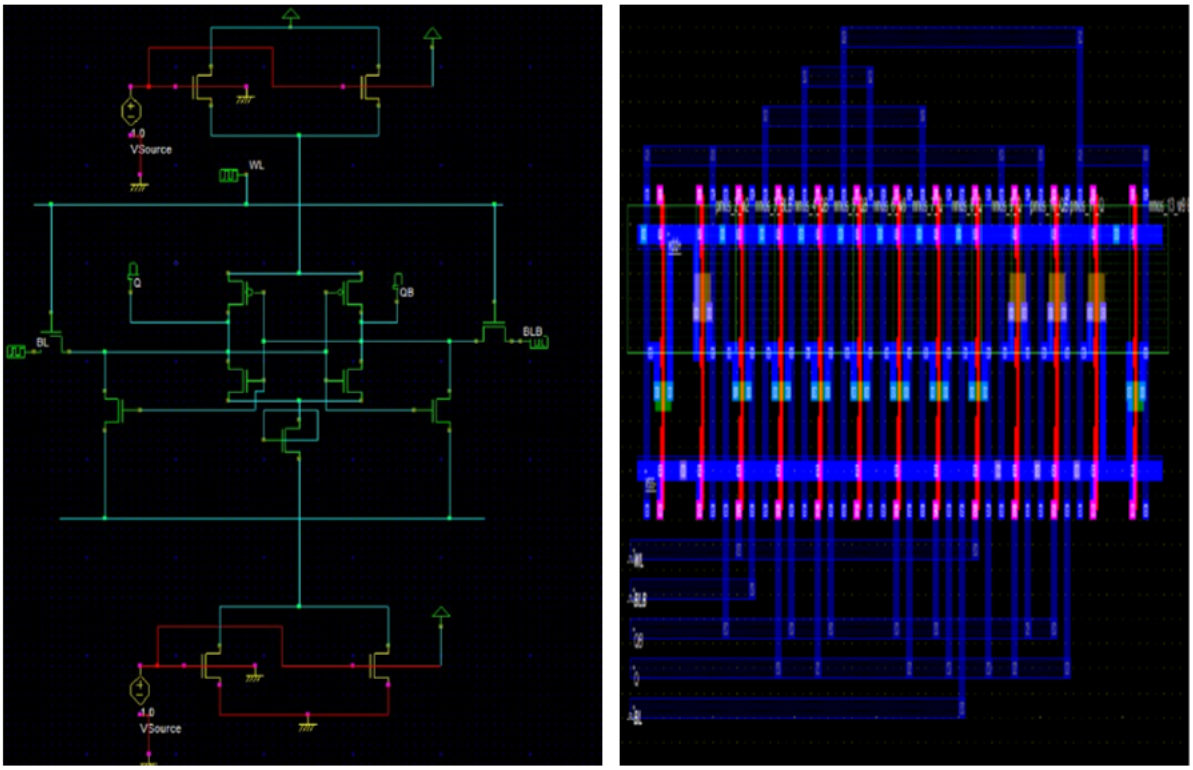

Fig 2. Proposed Schematic and Layout of 9T SRAM Cell configuration employing UL-SVL (SVL)

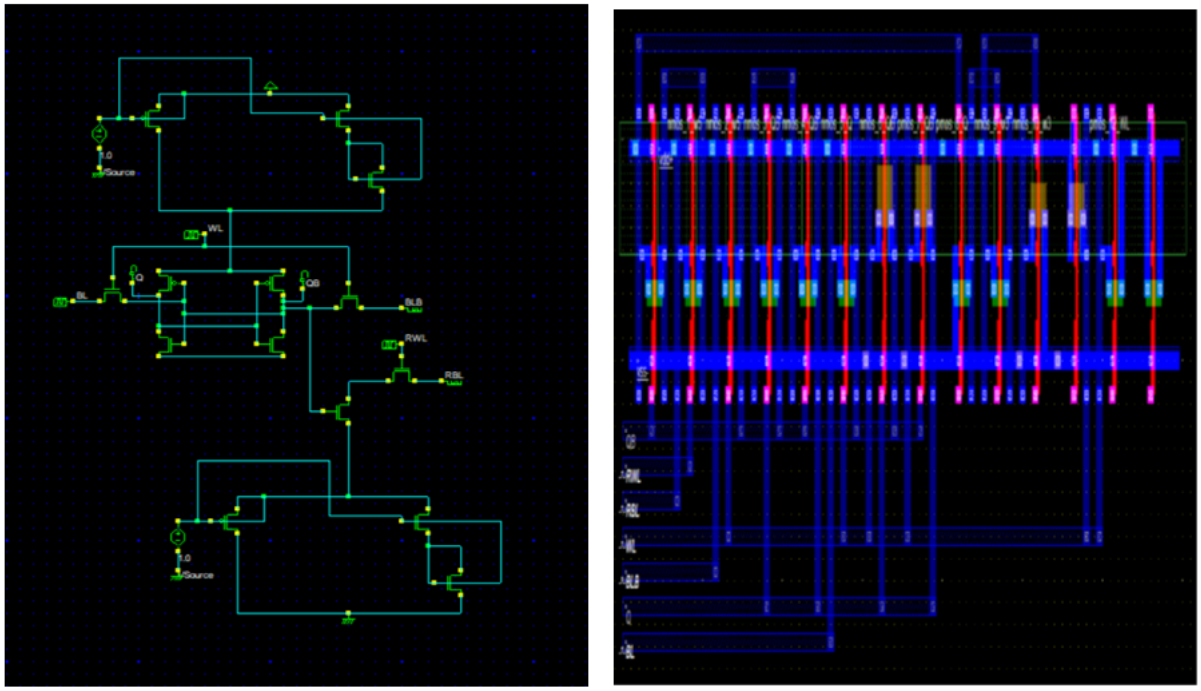

Fig 3. Proposed Schematic and Layout of 8T SRAM Cell configuration employing UL-ISVL (ISVL)

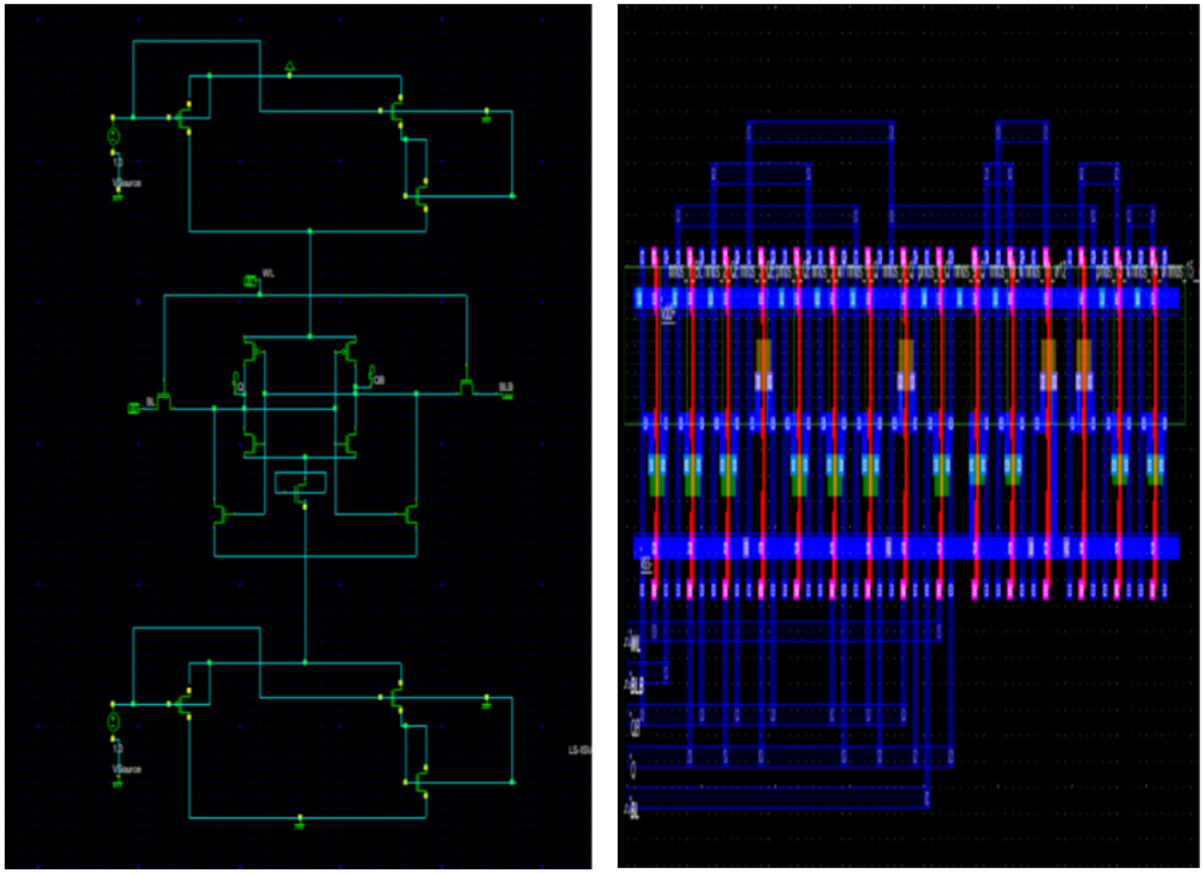

Fig 4. Proposed Schematic and Layout of 9T SRAM Cell configuration employing UL-ISVL (ISVL)

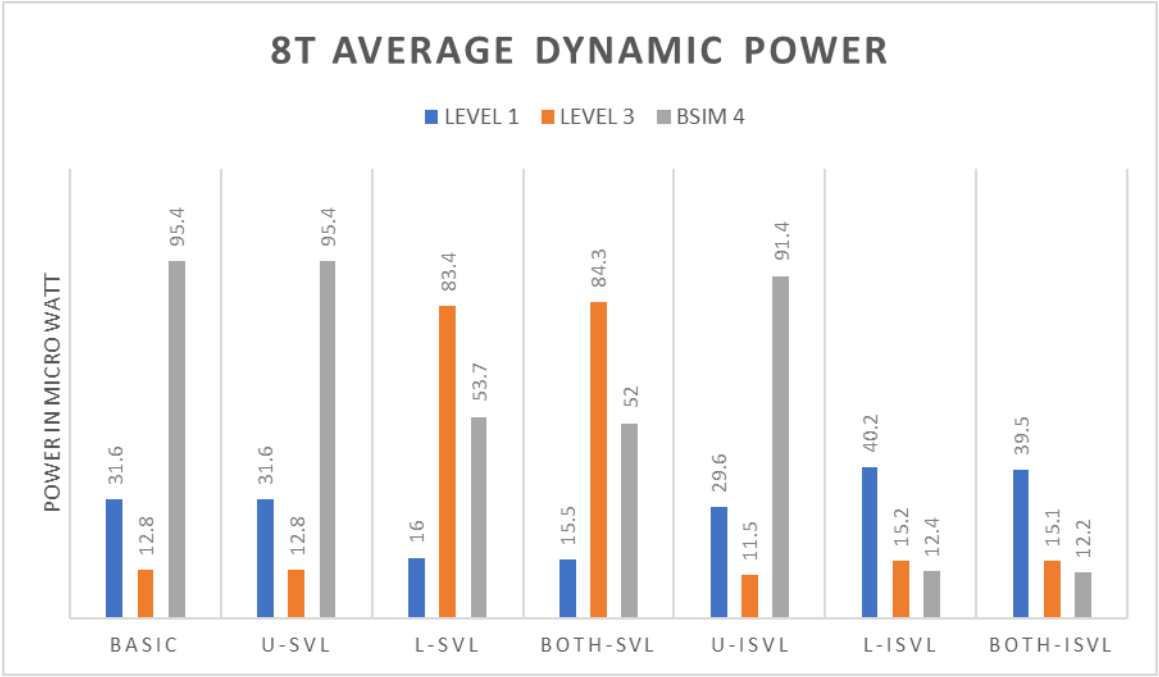

Fig 5. Comparative Dynamic power analysis of 8T SRAM cells using various Process Corner models

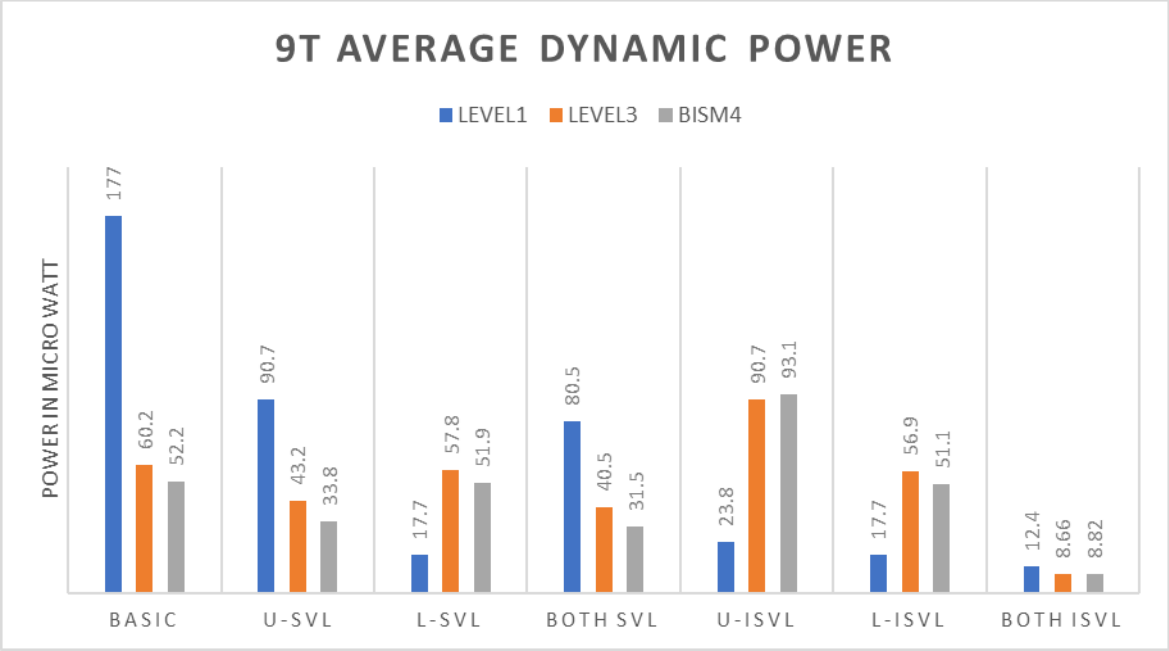

Fig 6. Comparative Dynamic power analysis of 9T SRAM cells using various Process Corner models

The average Dynamic power analysis results have been compared for different 8T SRAM Cells using SVL, ISVL for various Process corners and transistor sizing. Simulation was conducted across different Process Corners of Level1, Level3 and Bsim4. From the Implementation results, it clearly demonstrates that the least dynamic power has been resulted in I-SVL method in comparison to SVL and Basic 8T cell depicted in Figure 1. In addition, it can be noted that the least dynamic power has been resulted in BSIM 4 model with the value 12.2μw. The resulted value shows improvements of 18% and 69% in comparison with the Level 3 and Level 1 models respectively. The simulated values show much improvements using I-SVL method in comparison to SVL technique.

The average Dynamic power analysis results have been compared for different 9T SRAM Cells using SVL, ISVL for various Process corners and transistor sizing. Simulation was conducted across different Process Corners of Level1, Level3 and Bsim4. From the Implementation results, it clearly demonstrates that the least dynamic power has been resulted in I-SVL method in comparison to SVL and Basic 8T cell depicted in Figure 1.

In addition, it can be noted that the least dynamic power has been resulted in Level 3 model with the value 8.66μw. The resulted value shows improvements of 30% and 1.8% in comparison with the Level 1 and BSIM 4 models respectively. The simulated values show much improvements using I-SVL method in comparison to SVL technique.

The Total power consumption of 8T and 9T SRAM Cells with the Basic, SVL and I-SVL circuits has been simulated for various process corners of Level 1, Level 3 and BSIM4.The simulated results clearly demonstrated that the least power has been resulted in I-SVL in comparison to SVL and Basic configuration. In addition, least power has been resulted in BSIM4 model of both 8T and 9T I-SVL based configurations in comparison with the level 1 and Level 3 models.

Table 1. Comparison of Total Power between the existing literature and proposed cell

	Proposed 8T and 9T Cells	**Existing 8T and 9T cells Ref[6]**	**% of Improvements**
Power in micro watts	14.6	30.126	52
	And	And	And
	10.6	33.85	68

The total power analysis has been carried for 8T and 9T SRAM cells with different possible combinations of USVL, LSVL, UL-SVL, U-ISVL, L-ISVL, UL-ISVL configurations. The proposed 8T and 9T SRAM cells using I-SVL technique shows improvements in terms of total power with the existing 8T and 9T SRAM configurations. The comparative analysis of total power between existing and proposed 8T and 9T SRAM cells is depicted in the Figure 1. From Figure 1 it can be clearly noted

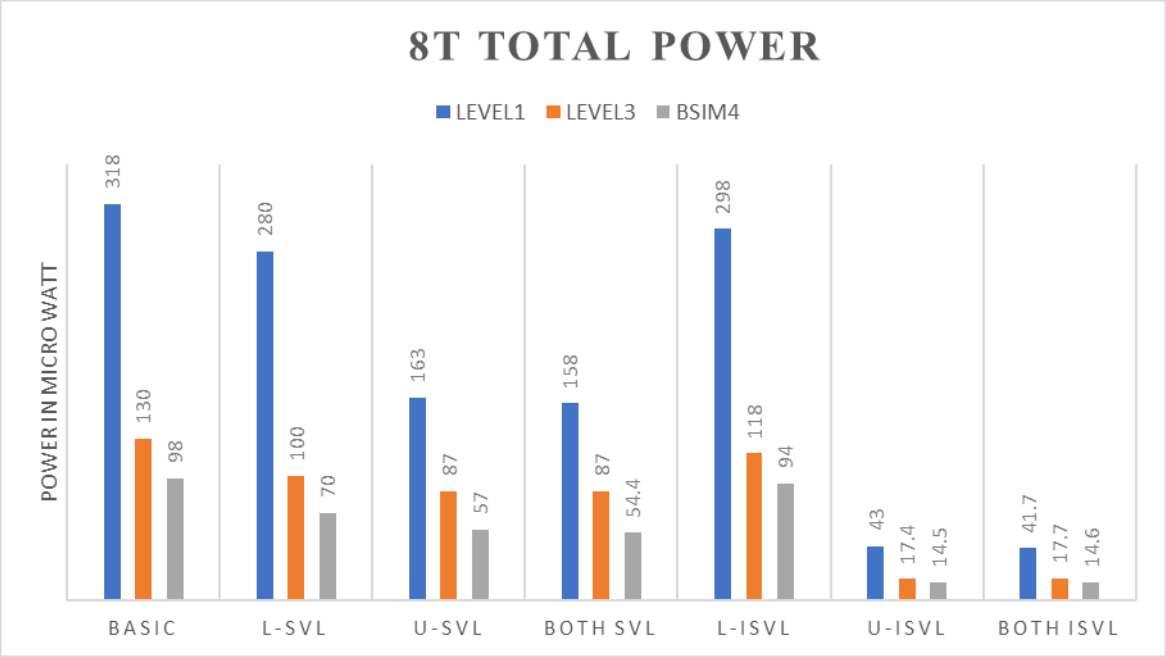

Fig 7. Comparative Total power analysis of 8T SRAM cells using various Process Corner models

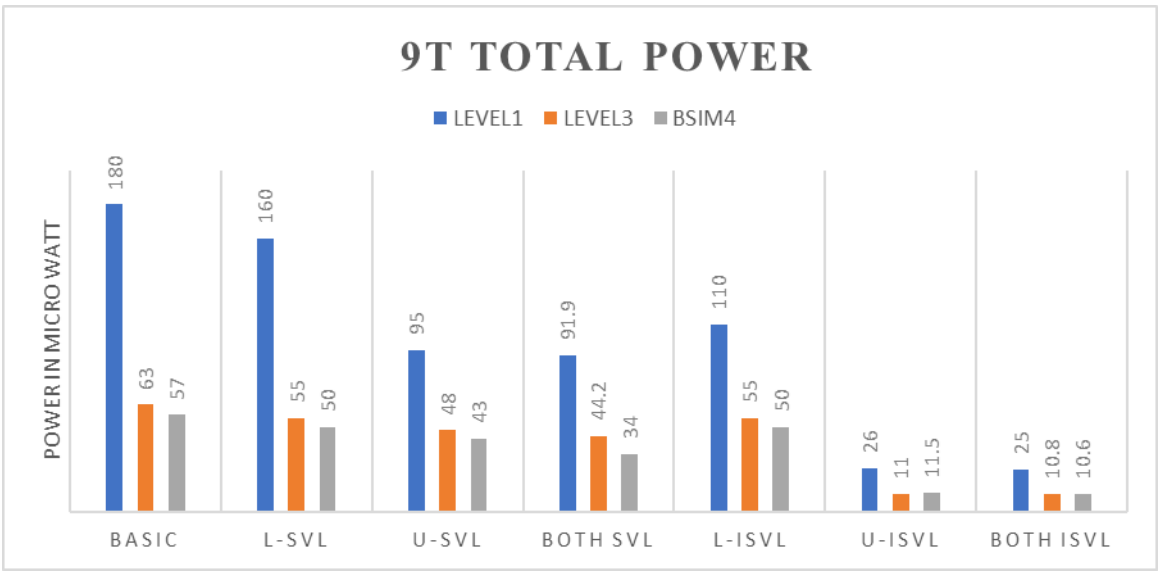

Fig 8. Comparative Total power analysis of 9T SRAM cells using various Process Corner models

that the proposed 8T and 9T SRAM cell shows 52% and 68% improvements in terms of total power comparatively with the work[6].

4 Conclusion

This study presents the designing and Implementation of Low power 8T and 9T SRAM cells. The implementation has been carried through the usage of SVL and I-SVL methods, which exhibits significant improvements in terms of power. The proposed 8T I-SVL based cells shows improvements in power by 18% and 69% using BSIM 4 in comparison with the Level 3 and Level 1 models respectively. The proposed 9T I-SVL based cells shows improvements in power by 30% and 1.8% using Level 3 in

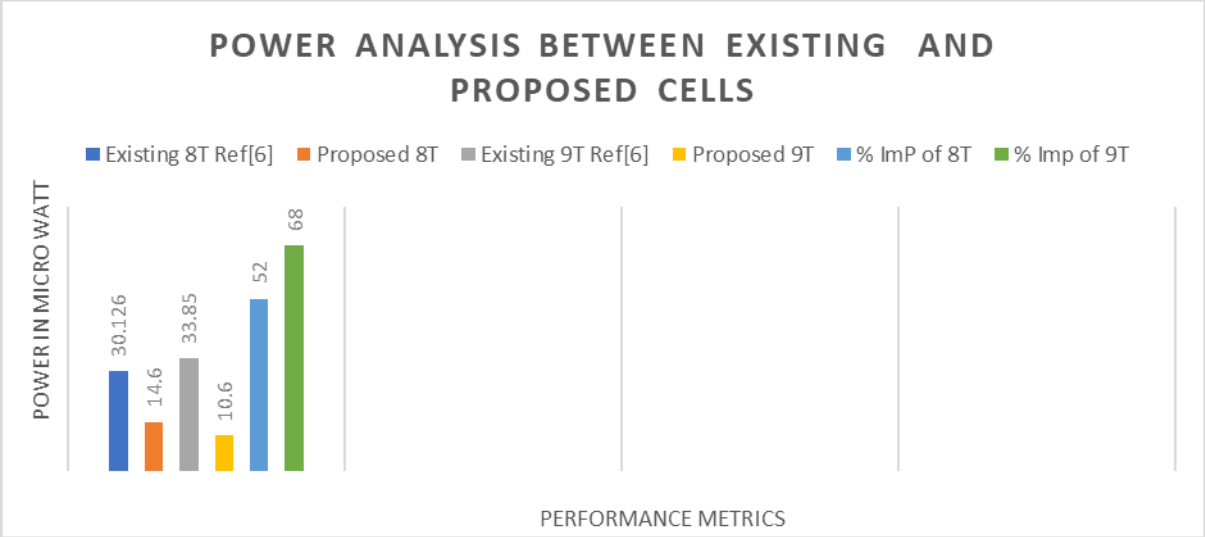

Fig 9. Comparative Total power analysis of Existing and Proposed 8T and 9T SRAM cells

comparison with the Level 1 and BSIM 4 models respectively. In addition, the proposed I-SVL 8T and 9T SRAM cell shows 52% and 68% improvements in terms of total power comparatively with the existing work[(6)]. The proposed work results clearly demonstrate the significance of SVL and I-SVL techniques with least power consumption in comparison to Conventional 8T and 9T configurations.

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