INDIAN JOURNAL OF SCIENCE AND TECHNOLOGY

RESEARCH ARTICLE

Issues and Challenges in Small-Signal Low-Power Amplifiers: A Review

Sachchidanand Shukla[1]*, Syed Shamroz Arshad[2], Kavita Thakur[3], Geetika Srivastava[4]

1 Professor, Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, Uttar Pradesh, India
2 Research Scholar, Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, Uttar Pradesh, India
3 Professor, Department of Electronics, Pt. Ravishankar Shukla University, Raipur, Chhattisgarh, India
4 Associate Professor, Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, Uttar Pradesh,, India

OPEN ACCESS

Received: 04-07-2024
Accepted: 27-08-2024
Published: 21-09-2024

Citation: Shukla S, Arshad SS, Thakur K, Srivastava G (2024) Issues and Challenges in Small-Signal Low-Power Amplifiers: A Review. Indian Journal of Science and Technology 17(36): 3787-3799. https://doi.org/10.17485/IJST/v17i36.2171

* **Corresponding author**.

sachida.shukla@gmail.com

Funding: Research and Development Scheme, Department of Higher Education, Government of Uttar Pradesh, India, ref. no. 44/2022/868/Sattar-4-2022/001-4-28-2021.

Competing Interests: None

Published By Indian Society for Education and Environment (iSee)

ISSN
Print: 0974-6846
Electronic: 0974-5645

Abstract

Background: Contemporary linear electronic circuit designs frequently include small-signal low-power amplifiers as a fundamental building block. These amplifiers are widely used as LNAs (Low Noise Amplifiers) in the pre-amplifier stages of both low-frequency and high-frequency featured electronic circuits. **Objectives**: To review the recent advances in the design of small-signal low-power amplifiers based on device configuration of BJTs, JFETs and MOSFETs for low ($\leq$1KHz) and high frequencies ($\geq$1MHz) at smaller input voltage (<1 Volt). **Methods**: The articles published between 2010 to 2024 are shortlisted from IEEE Xplore, Springer, Science Direct Elsevier, Google Scholar, and MDPI databases and the outcomes of the different techniques are compared on various parameters. **Findings**: It is found that four-stage CMOS amplifier at TSMC 40nm process technology emerges with highest 84.59dB gain, InP (Indium Phosphide) Distributed Amplifier Using 3-D Interdigital Capacitors carries widest bandwidth of 160 GHz, two stage darlington pair amplifier at 0.18μm under dual input and dual output topologies and four stage CMOS amplifier at 40nm technology realizes lower power consumption of 0.5mW and 0.00086 mW respectively. Small Signal Amplifier based on single stage BJT-JFET Sziklai pair operates at lowest frequency of 11.36 Hz, single stage LNA at 180nm CMOS technology using inductive degenerate topology works at very low supply voltage at +0.5V and, recently reported complementary sziklai based small signal amplifier under CC mode works at lowest -15V supply voltage. **Novelty**: The review proposed on 'Small Signal Low Power Amplifier' is first time reported in this paper. Moreover, it discusses low power small signal amplifiers at both low ($\leq$1KHz) and high ($\geq$MHz) frequencies considering gain enhancement technique, power dissipation reduction technique, and noise reduction technique whereas other review papers emphasize on the general discussion of different topologies only at high frequencies.

Keywords: Small-Signal Amplifiers; Low Power Amplifiers; BJTs; JFETs; MOSFETs

1 Introduction

Small-signal low power amplifiers, at low-frequencies, are widely used in pre-amplifier stages of sensor signal acquisition system for amplifying the low amplitude output signals (Refer Figure 1). Generally, output signals of the sensors are found in the μV range; therefore, these signals are usually amplified before feeding it to the signal processing unit for any practical application[(1)]. Similarly, at higher frequencies, these amplifiers are used as LNAs in wireless communication system in order to amplify RF signal received from antenna which is generally weak and noisy[(2)] (Refer Figure 2). Therefore, small-signal low power amplifier plays an important role in contemporary linear electronic circuit designs in both low as well as high-frequency domains.

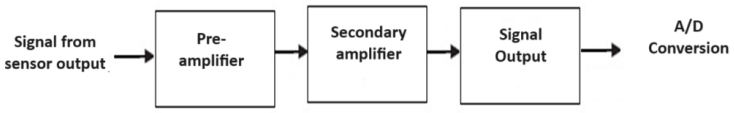

Fig 1. Sensor Signal Acquisition System

Over the years, many review papers have been proposed on the different topologies of Low Noise Amplifiers (LNAs)[(3)] [(4)] [(5)]In this reference, Kalra et al.[(3)] presented a review on LNA using distributed amplifier, source degeneration, common gate, common source with inductive and resistive load topologies along with their respective advantages and disadvantages. Priyanka et al.[(4)] proposed a review on LNAs topologies for global navigational satellite system (GNSS). Review on different topologies of LNAs is proposed by Agrawal et al.[(5)] and compared their respective parameters such as power consumption, gain, supply voltage, Noise figure, and input third order intercept point (IIP_3). Literatures shows that the existing review on low noise amplifiers (LNAs) focus on describing LNA topologies at high frequencies only. However, none of these review papers have described the operation of LNAs at low frequencies and respective bottlenecks in designing these amplifiers.

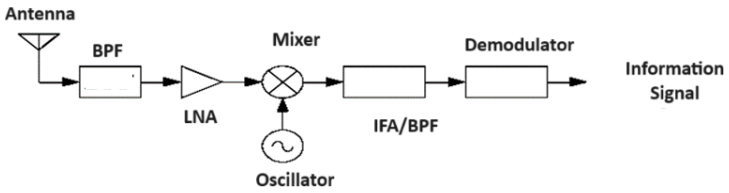

Fig 2. Broadband Communication System

This review paper, therefore, compensate the technical gap of the existing literature and provides the review outcome of 'Small Signal Low Power Amplifiers' based on device configuration of BJTs, JFETs and MOSFETs at both low ($\leq$1KHz) as well as high frequencies ($\geq$1MHz) at smaller input voltage (<1 Volt) in the form of tables and bar graphs including milestone works and break-through technologies, bottlenecks and prospective/emerging area for implementations/improvements. The research contributions, research gap, and research question of the proposed review are described as follows:

1.1. Research Contributions

The research contributions of the proposed review are discussed as follows:

- The review on 'Small Signal Low Power Amplifiers' based on BJTs, JFETs, and MOSFETs is the novel work and first time reported.
- In addition to the high frequencies, this review also provides a comprehensive summary of the available literature on Low Noise Amplifiers (LNAs) at low frequencies which is rarely available in the literature.
- This review provides discussion on key bottlenecks such as noises at low and high frequencies, high DC supply voltage problem, poor frequency response problem, and distortion problems along with their reliable solutions in the design of Small Signal Low Power Amplifiers.
- This review underscores the existing limitations in Small Signal LNAs and projects Sziklai pairs, due to the half base turn-on voltage and better linearity than Darlington pair, to find its exposure in linear electronic circuits, especially in the circuits of small-signal amplifiers.

1.2. Research Gap

Most of the available review on Low Noise Amplifiers (LNAs) are focused on describing different topologies at high frequencies, but literatures on the design and development of small signal low power amplifiers based on BJTs, JFETs, and MOSFETs at low frequencies are rarely available[3–5]. This manuscript, filling the technical void, provides an overview of the most recent advancements in the design of small-signal low power amplifiers using BJTs, JFETs, and MOSFETs device configurations at lower input voltages (<1 Volt), along with a description of the gain enhancement, power dissipation reduction, and noise reduction techniques used in these amplifiers for both low ($\leq$1KHz) and high ($\geq$1MHz) frequencies. All of the techniques have been compared in tables on various parameters, including bandwidth, voltage gain, power dissipation, supply voltage, die area, process, and their respective topologies and techniques.

1.3. Research Questions

The present literature review is mainly based to answer the following questions:

'What are the fundamentals in the development of small-signal amplifiers based on device configurations of BJTs, JFETs and MOSFETs at low and high frequencies, their issues and challenges, reported topologies of small-signal amplifiers at low input voltages, and emerging area for further improvements and implementations?'

The remainder of the review is organized as follows. Section 2 deals with the review methodology of the proposed work, result and discussion part are discussed in Section 3 which highlights analyses and findings of the proposed work in the form of tables and graphs, bottlenecks, and emerging area for improvements. Finally, conclusion is drawn in Section 4 which include a comprehensive summary encompassing the contributions, limitations, and future prospects of the review.

2 Methodology

This section accommodates the methodology adopted for review of the literatures relevant to 'small-signal low-power amplifier' at low ($\leq$1KHz) and high ($\geq$1MHz) frequencies. In the present section, a review methodology is performed to gather supplementary information which includes database consulted, keywords used, year of coverage, inclusion and exclusion criteria and parameters considered for concept development.

2.1. Selection of Study and Data Extraction

It is the initial level for preparation of the literature review. This consists of the keywords to search related papers from database libraries, period of coverage of selected research papers/articles and moreover the inclusion and exclusion criteria of research papers/articles.

2.1.1. Keywords

The following search strings are employed to find the research papers related to the aim of literature review:

- Small-signal Amplifiers based on BJTs, JFETs and MOSFETs OR
- Low input voltage small-signal amplifiers OR
- Issues and challenges in small-signal amplifiers OR

- Small-signal amplifiers at 45nm, 90nm and 180nm Technology OR
- Techniques for high gain, power dissipation reduction and noise reduction in small-signal amplifiers.

2.1.2. Research paper selection from databases libraries

Database libraries are searched using the mentioned keywords, precisely to identify the relevant research articles with a focus on recent work. Table 1 shows statistics of the research papers selected from the different databases libraries. The acquisition of the related research papers on small-signal amplifiers are done for period 2010-2024 using aforementioned databases libraries.

Table 1. Number of Papers and their Publishers

Publishers	URL	Number of Papers
IEEE Xplore	http://ieeexplore.ieee.org/	7
Google Scholar	http://scholar.google.com/	8
MDPI	http://www.mdpi.com/	4
Science-Direct Elsevier	http://www.elsevier.com/	1
Springer	http://www.springer.com/	3
Scopus	http://www.scopus.com/	2

2.1.3. Inclusion and Exclusion of research papers

The present literature review includes relevant research papers as per following criteria:

- The paper must come within the circumference of the selected field.
- Paper is easily accessible from databases library.
- The year of publication of the paper falls between 2010 and 2024.

Some research papers are excluded after the initial search as per following criteria:

- Thesis
- Patent
- Research papers for less than 2 citations.
- Research articles which do not lie within the selected duration (2010-2024).
- Research papers partially answer the research question.

2.2. Study Selection Process

At initial level, total 25 research papers are selected to participate in the process of literature review. However, considering aforementioned inclusion criteria, 9 research papers partially answer the research question; therefore, these research papers are filtered out from the process of review in different steps. Finally, 16 research papers, properly answering the research question, are brought forward to be the part of literature review. Entire selection process of the research papers is summarized in Figure 1.

2.3. Parameters Considered for Concept Development

The performance metrics[6], that are usually considered in the design of small-signal amplifiers, are summarized as follows.

- **Input impedance**: This must be high (ideally infinite) for small-signal amplifiers. High input impedance prevents input voltage from distortion and therefore provides a conducive environment for a proper utilization of the input current.
- **Output impedance**: This should be low (ideally zero) to receive maximum stuff of the output amplified current without any distortion.
- **Power dissipation**: This is the amount of power drawn from DC supply voltage by the small-signal amplifier. It is generally kept as low as possible by scaling down DC power supply voltage.
- **Bandwidth**: It is the range of frequencies at which the gain of the amplifier falls to 70.7% of its peak value (cut-off frequencies or -3dB frequencies). For an ideal small-signal amplifier, bandwidth should be infinite. The bandwidth of the amplifier is given by-

$B_W = f_H - f_L$, where f_H and f_L denotes higher and lower cut-off frequencies, respectively.

- **Slew rate**: It is the rate of change of output voltage with respect to time. For an ideal amplifier, slew rate must be infinite.It can be defined as –

$$Slew\ rate = \left|\frac{dV_o}{dt}\right|_{max} \left(\frac{Volt}{Sec}\right)$$

- **Gain**: It is defined as the ratio of output voltage or current to input voltage or current. It is usually defined on logarithmic scale in terms of decibel (dB). For an ideal amplifier, value of gain must be high. The usual expression for voltage gain is as follows -

$$A_{V(dB)} = 20Log_{10}\left(\frac{V_{out}}{V_{in}}\right)$$

- **Power gain**: It is the measure of the ratio of output signal power to the input signal power . It can be expressed as follows

$$A_{P(dB)} = 10Log_{10}\left(\frac{P_{out}}{P_{in}}\right)$$

Where Pout and Pin indicates output and input power respectively. Positive decibel value indicates power gain whereas negative decibel shows power loss.

- **Total Harmonic Distortion**: THD shows the variation of output signal waveform with respect to input signal waveform in terms of percentage. It is used to characterize the linearity of the amplifier. Total harmonic distortion of an amplifier is given by -

$$\%\ nth\ Harmonic\ distortion = \ \%\ D = \frac{|A_n|}{|A_1|} \times 100\%$$

Where A indicates the gain of the amplifier. Both, high as well as low distortion are useful as per the need of system design. For high-fidelity audio amplifiers, low distortion is needed whereas for guitar amplifiers, circuit with high level of distortion is the prime requirement.

Prominent performance metrics for small-signal amplifiers with respective ideal values are summarized in Table 2.

Table 2. Ideal values of parameters

Performance Metrics	Ideals Value
Input impedance	$\infty\Omega$
Output impedance	0Ω
Bandwidth	∞Hz
Slew Rate	$\infty Volt/sec$
Total Harmonic Distortion	Depends on requirement
Gain	High
Power Gain	High
Power Dissipation	Low

3 Results and Discussion

This section provides the review outcome in the form of tables and bar graphs including milestone works and break-through technologies, bottle-necks and prospective/emerging area for implementations/improvements.

3.1. Overview and Findings

3.1.1. Gain-Enhancement Techniques

BJT Common-Emitter amplifier based **Multi-Stage Technique** is presented by Dan-Abia et al.[7] in 2019. This topology is proposed for improving voltage gain of single-stage BJT amplifier for efficient processing of low frequency ($\leq$10 KHz) audio signal with high gain of 55. Under this toplogy, circuit consists of two BJT coupled by a coupling capacitor C_C. With the same technique, 20KHz bandwidth and 63.58 dB gain is received by Wardhana et al.[8], 123GHz bandwidthand and 55dB gain by Huang et al.[9], 23.903 KHz bandwidth and 61.27 dB gain is achieved by Soni et al.[10], and 0.161 GHz unity gain bandwidth and 84.59 dB gain is achieved by Gao et al.[11]. Major drawbacks of this topology is that the circuit occupy large area due to multi-stage configuration and suffers from high harmonic distortions at output port.

3.1.2. Power Dissipation Reduction Techniques

Dual-Input Dual Output Techniques was first given by Motlak et al.[12] in 2013. In this technique, Intermediate amplifier (IF) is discussed using 0.18 μm MIETEC technology channel length of MOSFET Darlington transistors. Resultant amplifier topology, with the help of PSpice software, produces 1.2 GHz wide bandwidth, 7.6 dB gain, 3.4 GHz gain-bandwidth product, 0.5 mW DC power consumption and 12 nV/sqrt(Hz) output noise at 1.2V supply voltage. Advantage of this topology is that it does not force us to use multi-stage amplifier configuration for widebandwidth operation. Drawbacks of this topology is that it consists of large numbers of active and passive devices, which collectively generates large noise at output.

3.1.3. Noise Reduction Techniques

Inductive Degenerate Technique was proposed by Janisha et al.[13] in 2016. This technique is applied on CMOS based LNA at 90nm and 180nm CMOS technology to reduce the noise and enhancement of the bandwidth. Under this technique, parallel inductor is used at the base and drain terminal of follower MOSFET. Broadband bandwidth of 1.047GHz and 1.157 GHz is received at 180nm and 90nm technologies, respectively at 0.5V. However, gain of 40 dB remains constant at both the technology.

Hybrid Combination Technique was used by Shukla et al in 2019 to announce small signal amplifier with BJT at driver position and JFET at follower position under Sziklai pair topology for effective processing of low frequency signals dedicated to biomedical applications, seismic operations and underwater communication systems[14]. This amplifier circuit receives 11.36 Hz bandwidth with 5.783 gain. In[15], MOSFET-BJT-MOSFET combination is used in Hybrid Combination Technique which yields 16.275 MHz bandwidth with 59.39 gain under PSpice user defined environment whereas under Cadence software at 180nm, 15.8865 GHz bandwidth with 14.8325 gain is received. Advantage of using this technique is that it successfully eliminates the poor frequency response problem of Darlington pair amplifier at higher frequency.

The 3D interdigital capacitors technique was used by Nguyen et al. in 2020 to design the wideband millimeter wave (mm-wave) MMIC based distributed amplifier using InP HBT (Indium Phosphide heterojunction bipolar transistor) technology[16] with the main focus to reduce the noise figure. Under this technique, nine gain unit cells were used in Distributed amplifier topology which significantly reduced the noise figure to 10.1 dB and enhanced the gain up to 10.5 dB and bandwidth to 160 GHz. However, power dissipation and chip area increases to 288 mW and 1.28 mm^2 respectively.

RC Coupled Amplifier Technique is frequently used to generate constant gain over moderate range of bandwidth, hence suitable for audio applications[17,18]. This technique is often used in single- or two-stage amplifier topologies. This technique is reported in designing complementary Sziklai pair amplifier at 180nm GPDK technology under CE (Common Emitter) and CC (Common Collector) configurations[17] with 1.64 MHz and 1.90 MHz bandwidth and 200.05 and 0.13 gain respectively. In similar manner, PNP Sziklai pair CC amplifier using PSpice user defined BJTs and BJTs available at 180nm GPDK technology is reported in[18] with 204.474 MHz and 35.4034 MHz bandwidth and 37.28 dB and 40.93 dB gain respectively. However, there are some limitations associated with this topology such as poor impedance matching, low voltage gain, and low power gain.

3.1.4. Milestone Works and Break-Through Technologies

Some other low-frequency amplifier, used especially for sensor amplification, are now-a-days designed using different active devices such as Operational Transconductance amplifiers, van der walls BJTs based on vertically stacked n^+-$MoS_2/WSe_2/MoS_2$ and field effect transistors (FETs) based on crystalline ionic liquid gated interface[19] [20] [21] [22].

Operational Transconductance amplifiers (OTAs) are widely used for low frequency applications. It carries low-frequency, extremely low-power consumption, with low input and output referred noise, therefore OTA based filters are being extensively used for portable devices and bio-medical applications. Research articles related to OTA filter designs referred in Table 3, shows that OTA based filter/amplifiers produces very low cut-off frequency with low power consumption and low Input Referred Noise and Output Referred Noise. In this context, Moradi et al.[19] reported second order continuous Gm-C low pass filter

which generates 390nW power consumption along with 100Hz cut-off frequency, and Oliveira et al.[20] proposed a fourth order digitally tuneable Gm-C low pass filter under four different modes which shows power consumption of 9.9 mW/ 11.52 mW/12.83 mW/ 13.10 mW with cut-off frequency of 1.90 MHz/3.56 MHz/6.07 MHz/8.15 MHz respectively.

Zezhang et al.[21] has proposed a New Technique in 2024 to develop van der walls BJTs based on **vertically stacked n^+-MoS_2/WSe_2/MoS_2** using controlled multistep dry transfer process. Proposed device under common source (CS) and common base (CB) mode generates large current gain (α=0.98 and β=225) with open emitter base collector breakdown voltage (BV_{CBO}) and open emitter base emitter breakdown voltage (BV_{CEO}) reaches at 52.9V and 40.3V respectively. This study has paved the way for implementation of 2D materials based on van der walls BJTs for achieving high current gains.

Table 3. Summary of the Reported Small-signal Amplifiers design, operational transconductance amplifiers design, and other breakthrough design based on Miscellanies Technique

Ref.	Year	Bandwidth	Voltage Gain (dB)	PDISSI. (mW)	VDD (Volt)	Die Area (mm^2)	Process	Topology	Technique
[7]	2019	< 10 KHz	55	—	+15	—	—	Two-stage CE amplifier	Multi-stage Amplifier
[8]	2022	100 Hz-20 KHz	63.58	65	+15	—	—	Three-stage CE Amplifier	Multi-stage Amplifier
[9]	2010	123 GHz	55	40.5	+2.5	1	50nm GaN-SiC	Two-stage CE Amplifier	Multi Stage Amplifier
[10]	2024	10 Hz-23.913 KHz	61.27	–	—	—	Pspice	Two Stage CE-CS Amplifier	Multi Stage Amplifier
[11]	2024	0.161 GHz UGB	84.59	0.00086	+0.5	—	TSMC 40nm	Four Stage CMOS with with Cross-Feedforward Positive Frequency Compensation (CFPFC)	Multi Stage Amplifier
[12]	2013	1.2 GHz	7.6	0.5	12	—	0.18 μm MIETEC technology	Two Stage Darlington pair	Dual Input Duall Output
[13]	2016	1.047 GHz	46.02	15	+0.5	—	180nm CMOS	Single Stage LNA using MOSFETs	Inductively de generate LNA
		1.157 GHz	46.02	15	+0.5	—	90nm CMOS		
[14]	2019	13.418 Hz-2.058 Hz	5.8 (mag)	12	+15	—	—	Single stage BJT-JFET amplifier	Hybrid Combination
[15]	2022	45.066 Hz-16.276 MHz	59.3998	71.6	+18	—	PSpice model of User defined MOSFETs and BJTs	Single Stage MOS-BJT-MOS Darlington amplifier	Hybrid Combination
	2022	17.9569 Hz-15.8867 GHz	14.8325	556.556	+18	0.000080	Cadence Model of MOSFETs and BJTs at GPDK 180nm		
[16]	2020	160 GHz	10.5	288	+4	1.28	InP HBT (Indium Phosphide heterojunction bipolar transistor)	MMIC based distributed amplifier	3D interdigital capacitors
[17]	2023	58.72 Hz-1.64 MHz	46.0228	13.60	-15	0.000158	Cadence Model of BJTs at GPDK 180nm	Signle Stage Complementary Sziklai CE amplifier	RC Coupled amplifier
		2.26 KHz-1.90 MHz	-17.721	10.63	-15	0.000141			

Continued on next page

Table 3 continued

[18]	2023	204.474 MHz	37.28	—	+18	—	PSpice User defined model of BJTs	Single Stage BJT CC amplifier	RC Coupled amplifier
		35.4034 MHz	40.9354	2.9 W	+18	(10.105 × 10.055) μm^2	Cadence model at 180nm technology		
[19]	2021	100 Hz	—	0.00036	+1	—	0.18-μm CMOS technology	Seond order Low Pass Filter	Continuous Gm-C
[20]	2024	1.90 MHz	—	9.90	+1.8	0.23	180nm CMOS	fourth-order Low Pass Filter	Digitally tuneable Gm-C filter
		3.56 MHz	—	11.52	+1.8	0.23	180nm CMOS		
		6.07 MHz	—	12.83	+1.8	0.23	180nm CMOS		
		8.15 MHz	—	13.10	+1.8	0.23	180nm CMOS		
[21]	2024	—	! =0.98 and =225	—	@BVCBO = 52.9V and BVCEO = 40.3V	—	Controlled multistep dry transfer	Van Der Walls BJTs	Vertically stacked n+-#MoS2/WSe2/MoS2
[22]	2024	—	On/off ratio=103 at 200K	—	Electron mobility = 345 $cm^2 V^{-1}s^{-1}$ hole mobility = 285 cm^2 V^{-1} s^{-1}	—	%BMIM-BF4 ILG encapsulation	$2H MoTe2 based FET	Crystalline ionic liquid gated interface

! α *and* βdenotes current gains.
@BVCBO and BVCEO denotes open emitter base collector breakdown voltage (BVCBO) and open emitter base emitter breakdown (BVCEO) voltage respectively.
#MoS2 and WSe2 denotes Molybdenum disulfide and Tungsten diselenide respectively.
$2H MoTe2 stands for Molybdenum ditelluride.
%BMIM-BF4 ILG is the abbreviation of 1-Butyl-3-methylimidazolium tetrafluoroborate.

Saidov et al.[22] has presented the fabrication technique of field effect transistors (FETs) based on **crystalline ionic liquid gated interface** which consists of few layers of molybdenum ditelluride (2H $MoTe_2$). The resulting device exhibits p-type behavior with high on/off ratio of 103 at 200K temperature and high electron and hole mobility of 345 $cm^2V^{-1}s^{-1}$ and 285 cm^2 V^{-1} s^{-1} respectively at 80K temperature. This topology demonstrates the possibility for the implementation of the proposed 2D insulator device in optoelectronic and post silicon applications.

Table 3 shows a brief comparison of the Small Signal amplifier designs, operational transconductance amplifiers design, and other breakthrough design based on Miscellanies Technique reported in the spanning duration of 2010-2024, in terms of their bandwidth, voltage gain, power dissipation, supply voltage, area, process, topology and technique.

Different techniques of small-signal low-power amplifiers enable to achieve high frequency- bandwidth upto160 GHz with high gain of 10.5 dB[16] and 123 GHz bandwidth and 55 dB gain[9] whereas low frequency-bandwidth up to 11.36 Hz with a gain of 5.738[14]. However, each techniques have their own advantages and limitations as well.

From the data in Table 3, one can observe that there are many approaches of designing small-signal low-power amplifier. One may first choose a basic topology, for example, common-base, common-emitter, common-collector, common-source, common-gate or cascade topology under two or three stages; and then select an appropriate gain-enhancement, power dissipation reduction or noise reduction technique as per the requirement.

A gross look of the variation of various topologies used to achieve high gain, low power dissipation, wide bandwidth, low supply voltage, ability to enjoy low frequency operational condition and their summarized comparative discussion is presented in form of bar graph in Figure 4.

It is evident by Figure 4 that four-stage CMOS amplifier at TSMC 40nm process technology emerges with highest 84.59dB gain[11], InP Distributed Amplifier Using 3-D Interdigital Capacitors carries widest 160 GHz bandwidth[16], Two Stage Darlington pair amplifier at 0.18μm MIETEC (MIcroElectronicsTEChnologies) under Dual input and Dual output

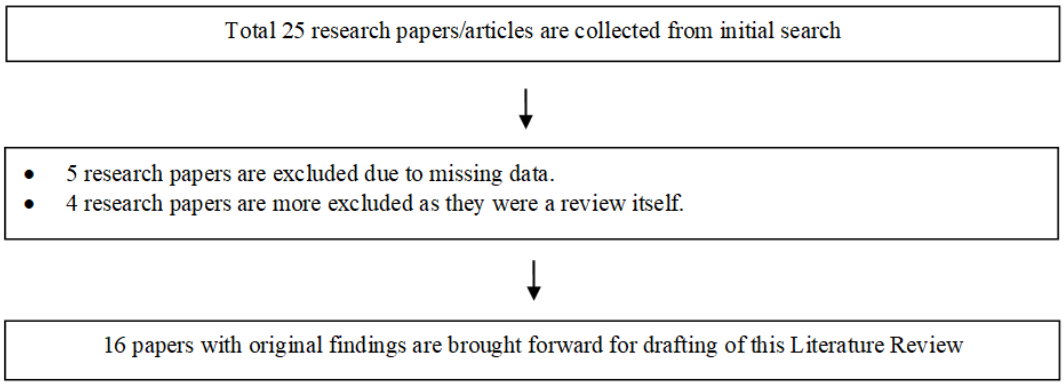

Fig 3. Study selection process for analysis/literature-review

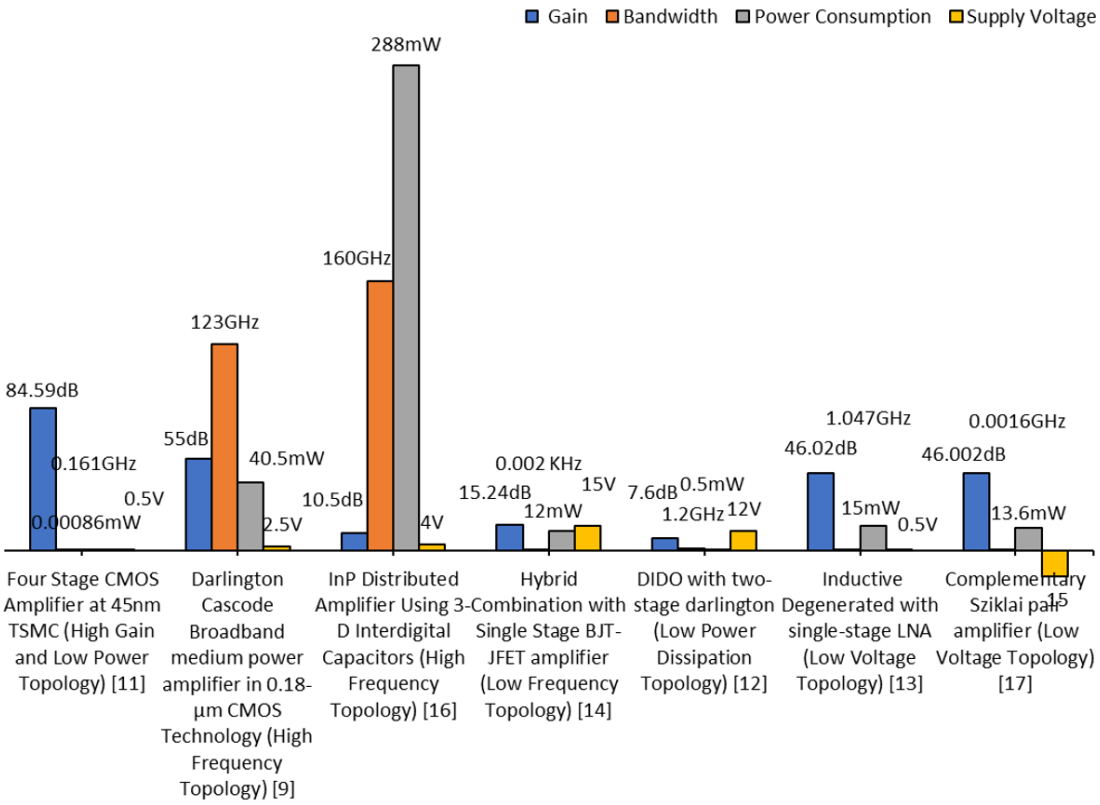

Fig 4. Comparative Chart

topologies[12] and four-stage CMOS amplifier at TSMC 40nm process technology[11] realizes lowest power consumption of 0.00086mW and 0.5mW respectively, Small Signal Amplifier based on single stage BJT-JFET Sziklai pair operates at lowest frequencies of 11.36 Hz[14], and Single Stage LNA at 180nm CMOS technology using inductive degenerate topology works at very low supply voltage at +0.5V[13]. However, recently reported Complementary Sziklai based Small Signal amplifier under CC mode also works at low -15V supply voltage[17].

3.2. Bottlenecks

Noise issue at low and high frequencies, high DC supply voltage problem, poor frequency response problem, and distortion problem are the key bottlenecks in the design of 'Small Signal low power amplifiers. This section covers the discussion on these bottlenecks and their reliable solutions.

3.2.1. Noise Issue

Noise energy always available whenever a circuit performs, and therefore plays important role as a liming factor for the operational signal levels in a circuit. It therefore becomes necessary to study and analyze the noise present in the circuit for a better performance, as it potentially affects the performance of the circuit as well as the quality of the output. This portion covers the noise issue related to BJT, JFET and MOSFET based small-signal amplifiers at low as well as high frequencies[1–5,19–22].

3.2.1.1. Noise at Low Frequency. The output signal from sensors or ECG is often too weak in amplitude (μV). Efficient processing of these weak amplitude signals is of vital importance for any practical usage. However, noise present in the circuit generally interrupt the usual behaviour of the amplifier, therefore noise must be supressed as low as possible[1,2].

Noise can be classified into two parts: (i) Internal noise and (ii) External noise. The internal noise is generated within the active devices (BJTs, JFETs and MOSFETs) whereas the external noises are appeared due to resistors and capacitors linked to the circuit[3].

The low frequency region is mainly dominated by the 1/f noise (flicker noise) and burst noise. The 1/f noise (flicker noise) exists due to the effect of lattice defects in semiconductors whereas burst noise is caused by the capture and emission of charge carriers within the semiconductors[4].

For smaller value of base-spreading resistance, BJTs are employed as an active device for low noise amplifier because it has 10 times lower input noise voltage than JFETs. Contrarily, JFETs are preferred choice for low noise amplifier at higher values of source resistance. However, MOSFETs should be avoided to use as an active element in low noise amplifier because it has high value of 1/f noise at low frequencies[5].

Capability of noise handling alone by BJTs, JFETs and MOSFETs are not efficient, moreover, they are independently not reliable and stable. Hence low noise amplifiers using Op-Amp, OTA and differential amplifiers are constructed to ensure the reliability and effective filtering of the noise[19–22].

3.2.1.2. Noise at High Frequency. At higher frequencies, researchers prefer to deal with noise power (instead of noise voltage or noise current) which is referred to as a small amount of voltage measured at the output even without the input[4,5].

Generally, Shot noise (or Schottky noise) dominate the semiconductor at higher frequency domain. This noise is caused by the random fluctuation of current flow in semiconductors through PN junction. Carriers in forward biased PN junction must have some thermal energy to overcome the potential barrier.This noise is associated with the individual carrier passing through the PN junction. This type of noise is generally found in BJTs not in JFETs[22]. Mean square value of the Shot noise current is given by

$$\bar{i_{SN}^2} = 2qI\triangle f$$

Where q is the electron charge, I is the forward junction current and $\triangle f$ is the frequency bandwidth.

3.2.2. High DC Supply Voltage Problem

DC supply voltage play a very crucial role in optimizing total power consumption of the circuit as well as creating large gain because it causes transistor to operate in saturation mode where it receives linear amplification[8].

One of the major problem associated with small-signal BJT amplifiers is that it operates at large DC supply voltage. Under this situation, even though the circuit receives higher gain but suffers from high collector current, high power consumption, optimization in bandwidth and inter-electrode capacitance effect at higher frequency at the same time[12].

This problem is resolved using small channel length MOSFET based amplifiers. Reducing channel length reduces the value of threshold voltage V_T of MOSFETs (i.e. gate voltage at which current start to flow from source to drain) and enables to use small value of supply voltage and supply current [13].

However, there is a certain limitation of CMOS supply voltage scaling by MOSFET threshold voltage [14]. For better performance of the MOSFET small-signal amplifiers, it is recommended that the supply voltage should be 2Volt or less which is governed by the empirical formula

$$\triangle T_{pd} \propto \frac{\triangle V_T}{(V_{CC} - V_T)^{2.5}}$$

Where $\triangle T_{pd}$ shows stage delay, V_T is theshold voltage and V_{CC} is the supply voltage.

3.2.3. Poor Frequency Response Problem

Higher frequency response of small-signal Darlington pair amplifiers are found to be very poor [9]. The reason is that the phase difference of output voltage of Darlington pair at high frequency is higher than a single BJT [10]. Additionally, due to the negative feedback, it becomes more unstable [12].

Efforts have been made in order to overcome the poor response problem at high frequency which includes addition of some extra biasing resistor at the emitter of the first transistor, using triple Darlington pair topology in cascade arrangement, using distributed amplifier topology and so on [15]. These modification still suffers, in one way or another, from reduction in gain and bandwidth shrinkage [23].

3.2.4. Distortion Problem

The distortion of output signal waveform has always been a problem in single stage BJT, Darlington and Sziklai pair small-signal amplifiers at higher frequencies. However, selection of appropriate values of the bypass capacitor C_E, load capacitor C_L, input capacitor C_1 and output capacitor C_2 plays a crucial role to optimize this problem [14].

It is also to be noted that higher level of THD is received when square wave is applied at the input terminal [15]. Additionally, BJT based CE amplifiers suffers from Miller effect at higher fequencies which increases the input capacitance and thereby decreases the higher cut-off frequency, thus it may also be accounted for the overall distortion [17].Moreover, in BJT based CB and CC amplifiers, distortion is very minimal at lower as well as higher frequency [18].

3.3. Emerging Area for Improvements/implementations

Small-signal voltage measurement is still a challenging task at both, low as well as high frequencies [6]. There aren't many published circuits of small-signal amplifiers with significant current gain at smaller input voltages. Due to their low current and voltage gain, existing amplifiers, based on single-stage semiconductor device, require the usage of multistage amplifiers [7]. Aside from taking up large areas, multistage amplifiers have significant harmonic distortion and poor noise immunity [8,9]. When Darlington pair is used in place of single active devices-based amplifiers or multistage amplifiers, large current gain at low frequency is received even at low input voltage with low noise and low harmonic distortions [10]. However, the frequency response of Darlington pair-based small signal amplifiers is poor at higher frequencies which is, consequently, resolved by the inclusion of additional biasing resistances [12]. Instead, Sziklai pair resolves the poor frequency response problem of Darlington pair at higher frequencies [14,15]. Over the years, Sziklai pair has received much attention due to its superior features over Darlington pair i.e., half base turn-on voltage ($\simeq$625mV) as compared to Darlington pair ($\simeq$1.36 Volts), better thermal stability due to lower heat dissipation and better linearity due to lower quiescent current (10mA-100mA) [17]. Consequently, many small-signal amplifiers based on Sziklai pair configuration are fabricated globally over the last one decade [18]. Subsequently, many small-signal amplifiers with different active devices combinations and different biasing conditions were assembled under Sziklai pair topology which not only receive wide applicability in removing poor-frequency response problem of Darlington pair small signal amplifier at higher frequency but also acts as an alternative of Darlington pair amplifier in audio range amplifiers [14,15,17,18].

Seeing its better performance in small-signal amplifiers, efforts have also been made in implementing Sziklai pair in switching circuits, power amplifiers, multivibrators and other linear electronic circuits [23] . Sziklai pair along with Darlington pair is also being used in Diode-triggered Silicon-Controlled-Rectifier (DTSCR) to enhance the current gain of the DTSCR [24] . With such modifications, current gain of DTSCR is enhanced by 80% and turn-ON speed is improved by 42%-93% for different current level. Moreover, Sziklai pair in the circuitry is also being used to boost the output current at a low input voltage and to generate high frequency (20KHz) voltage spikes to make the appearance of constantly illuminous LED lighting [25].

Most of the literature are equipped with the Darlington pair based small signal amplifiers but there are not much articles available on Sziklai pair small signal amplifiers. Therefore, due to more promising features, a sharp opportunity for further investigation with Sziklai pairs are available to find its exposure in linear electronic circuits, especially in the circuits of small-signal amplifiers.

4 Conclusion

The purpose of the present literature review is to give researchers and designers a quick and timely reference on "Small Signal Low Power Amplifiers."

The majority of reviews on Low Noise Amplifiers (LNAs) that are available in the literature concentrate on describing different topologies at only high frequencies. However, there are rarely available literatures on the design and development of small signal low power amplifiers operating at low frequencies that utilize BJTs, JFETs, and MOSFETs device configuration. This review paper describes gain enhancement technique, power dissipation reduction technique, and noise reduction technique used in small signal low power amplifiers for both ($\leq$1KHz) and high ($\geq$1MHz) frequencies and all the techniques have been compared in tables on different parameters such as bandwidth, voltage gain, power dissipation, supply voltage, die area, process, and their respective topologies and techniques and provides an overview of the latest developments in small-signal low power amplifier design, utilising BJT, JFET, and MOSFET device configurations at smaller input voltages (<1 Volt).

The comparison brought in Table 3 suggests that InP Distributed Amplifier Using 3-D Interdigital Capacitors[16] is very promising in small-signal amplifier designs at higher operating frequencies of 160 GHz whereas Small Signal Amplifier based on single stage BJT-JFET Sziklai pair operates at lowest frequencies of 11.36 Hz[14]. It is also observed by Figure 4 that four-stage CMOS amplifier at TSMC 40nm process technology emerges with highest 84.59dB gain[11], InP Distributed Amplifier Using 3-D Interdigital Capacitors carries widest bandwidth of 160 GHz[16], Two Stage Darlington pair amplifier at 0.18μm MIETEC (MIcroElectronicsTEChnologies) under Dual input and Dual output topologies[12] and four-stage CMOS amplifier at TSMC 40nm process technology[11] realizes 0.5mW and 0.00086 mW power consumption respectively, Small Signal Amplifier based on single stage BJT-JFET Sziklai pair operates at lowest frequencies of 11.36 Hz[14], and Single Stage LNA at 180nm CMOS technology using inductive degenerate topology works at very low supply voltage at +0.5V[13]. However, recently reported Complementary Sziklai based Small Signal amplifier under CC mode also works at low -15V supply voltage[17].

Authors have also observed that the investigation area for small signal amplifiers is still open to optimize the performance metrics like noise factor, gain, power consumption and linearity and therefore experiment with Sziklai pair in linear electronic circuits especially with the circuits of small signal amplifiers, due to its superior features over Darlington pair, would emerge as promising factor in the near future. Similar to the small signal amplifiers, the authors have noticed that it is difficult to find review papers on large signal amplifiers based on BJTs, JFETs, and MOSFETs device configurations; which is a topic of futher research and likely need to be investigated in the near future.

References

1) Sathya P. Design of a Low Noise Signal Amplifier for Sensor Signal Amplification. *Innovations in Power and Advanced Computing Technologies (i-PACT)*. 2021;p. 1–6. Available from: https://doi.org/10.1109/i-PACT52855.2021.9696986.
2) Hussein ZM, Motlak H. Low Power Low Noise CMOS RF Amplifiers for Wireless Applications: A Review. In: 2nd International Conference on Advances in Engineering Science and Technology (AEST). 2022;p. 560–566. Available from: https://doi.org/10.1109/AEST55805.2022.10412863.
3) Kalra D, Goyal V, Srivastava M. Low noise amplifier for high frequency applications: A review. *Materials Today: Proceedings* . 2023. Available from: https://doi.org/10.1016/j.matpr.2023.03.354.
4) Priyanka CH, Venkata RD, Santosh SKG. A Review on design of low noise amplifiers for global navigational satellite system. *AIMS Electronics and Electrical Engineering*. 2021;5(3):206–228. Available from: https://doi.org/10.3934/electreng.2021012.
5) Agrawal R. The Review Paper on Different Topologies of LNA. Smart Energy and Advancement in Power Technologies. *Lecture Notes in Electrical Engineering*. 2023;927:53–68. Available from: https://doi.org/10.1007/978-981-19-4975-3_5.
6) Dailey DJ. Small-signal and Low-power amplifiers. In: Electronics for Guitarists. 2022;p. 59–158. Available from: https://doi.org/10.1007/978-3-031-10758-0_3.
7) E DAD, Udofia OA, M K. Design and Analysis of a Multistage Common Emitter Amplifier for Low Frequency Applications. *European Journal of Engineering Research and Science*. 2019;4(10):87–92. Available from: https://doi.org/10.24018/ejers.2019.4.10.1431.
8) Wardhana AW, Ramadhani, Priswanto Y, P. Design and Simulation of Multistages Common-Emitter, Common-Collector, AC Voltage Amplifier. *Journal Nasional Teknik Elektro*. 2022;11(2):85–96. Available from: https://doi.org/10.25077/jnte.v11n2.1009.2022.
9) Huang PC, Lin KY, Wang H. A 4-17 GHz Darlington Cascode Broadband medium power amplifier in 0.18-μm CMOS Technology. *IEEE Microwave and Wireless Components Letters*. 2010;20(1):43–45. Available from: https://doi.org/10.1109/LMWC.2009.2035964.
10) Soni P, Srivastava G, Shukla SN, Arshad SS. Two Stage High Gain Small Signal Amplifier with Sziklai pair and Darlington pair. *International Journal of Engineering Research and Applications*. 2024;14(1):71–75. Available from: https://doi.org/10.9790/9622-14016570.
11) Gao F, Chan PK. A 0.5-V Four-Stage Amplifier Using Cross-Feedforward Positive Feedback Frequency Compensation. *Chips*;3:1–31. Available from: https://doi.org/10.3390/chips3010001.

12) Motlak H. Design of Low Voltage, Low Power (IF) Amplifier Based-On MOSFET Darlington Configuration. *Circuits and Systems*. 2013;4:269–275. Available from: https://doi.org/10.4236/cs.2013.43036.
13) Janisha F, Pankaj L. Design and Simulation of Low Noise Amplifiers at 180nm and 90nm Technologies. *International Journal of Engineering Research and Application*. 2016;6(11):43–47. Available from: https://www.ijera.com/papers/Vol6_issue11/Part-1/G061101043047.pdf.
14) Shukla SN, Srivastava G, Soni P, Mishra R. Development of a Small Signal Amplifier with Modeling of BJT-JFET Unit in Sziklai Pair Topology. *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*. 2019;8(5):1530–1538. Available from: https://doi.org/10.15662/IJAREEIE.2015.0804014.
15) Arshad SS, Shukla SN, Sharma A, Srivastava G. Darlington pair based Small-Signal amplifier under triple transistor topology. *Journal of International Academy of Physical Sciences*. 2022;26(4):427–442. Available from: http://www.iaps.org.in/journal/index.php/journaliaps/article/view/960/821.
16) Nguyen NKL, Nguyen DP, Stameroff AN, Pham A. A 1-160-GHz InP Distributed Amplifier Using 3-D Interdigital Capacitors. *IEEE microwave and wireless components letters*. 2020;30(5):492–495. Available from: https://doi.org/10.1109/LMWC.2020.2980280.
17) Shukla SN, Arshad SS, Srivastava G. Novel complementary Sziklai pair based high gain low noise small-signal amplifiers. *International Journal of Power Electronics and Drive Systems (IJPEDS)*. 2023;14(4):2283–2292. Available from: https://doi.org/10.11591/ijpeds.v14.i4.pp2283-2292.
18) Shukla SN, Arshad SS, Soni P, Sharma AK, Srivastava G. Design and Analysis of Wideband PNP Sziklai Common Collector Amplifier with High Current Gain. *Indian Journal of Science and Technology*. 2023;16(42):3743–3755. Available from: https://doi.org/10.17485/IJST/v16i42.689.
19) Moradi M, Dousti M, Torkzadeh P. Designing a Low-Power LNA and Filter for Portable EEG Acquisition Applications. *IEEE Access*. 2021;9:71968–71978. Available from: https://dx.doi.org/10.1109/access.2021.3076160.
20) Oliveira MS, Carvalho M, Müller C, Compassi-Severo L, De Aguirre P, Girardi AG. Design and Characterization of a Digitally Tunable Gm-C Filter for Multi-Standard Receivers. *Electronics*. 2024;13(14):2866. Available from: https://doi.org/10.3390/electronics13142866.
21) Yan Z, Xu N, Deng S. Realization of High Current Gain for Van der Waals MoS2/WSe2/MoS2 Bipolar Junction Transistor. *Nanomaterials*. 2024;14(8):718. Available from: https://dx.doi.org/10.3390/nano14080718.
22) Saidov K, Razzokov J, Parpiev O, Yüzbasi NS, Kovalska N, Blugan G, et al. Formation of Highly Conductive Interfaces in Crystalline Ionic Liquid-Gated Unipolar MoTe2/h-BN Field-Effect Transistor. *Nanomaterials*. 2023;13(18):2559–2559. Available from: https://dx.doi.org/10.3390/nano13182559.
23) Arshad SS, Srivastava G, Shukla SN. Sziklai pair and Darlington pair RTL inverters for high drive current application. *Journal of Rajasthan Academy of Physical Sciences*. 2023;22(1&2):22–40. Available from: http://raops.org.in.
24) Du F, et al. Augmented DTSCR With Fast Turn-On Speed for Nanoscale ESD Protection Applications. *IEEE Transactions on Electron Devices*. 2020;67(3):1353–1356. Available from: https://dx.doi.org/10.1109/ted.2020.2965092.
25) Truong SKM, Kim KH, Khan SU, Salvant J, Banerjee A, Looper R, et al. Demonstration of 155.1μW Wake-Up Gas Sensor Node Toward 8 Month Lifetime. *IEEE 33rd International Conference on Micro Electro Mechanical Systems (MEMS)*. 2020;p. 622–625. Available from: https://doi.org/10.1109/MEMS46641.2020.9056262.