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RESEARCH ARTICLE

Development of Improved Low-leakage Current H6 Single-Phase Full-Bridge Inverter Topology

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Abstract

Objective: To minimize leakage current in non-isolated photovoltaic grid connected inverters. **Methods:** The circuit design integrates extra switches and modifies the switch drive signals at the midpoint of the DC bus voltage, altering the common-mode current path. **Findings:** The proposed topology exhibits significant potential for widespread adoption, finding practical applications in diverse industrial settings as well as in residential use. **Novelty:** The suggested method implies that the topology presents distinctive or beneficial characteristics in contrast to current solutions, rendering it especially promising for a range of industrial and residential applications. This novelty may arise from enhancements in efficiency, cost-effectiveness, scalability, versatility, or other favorable attributes that distinguish it from traditional approaches. Moreover, Simulation outcomes distinctly demonstrate a noteworthy decrease in leakage current within the refined topology when contrasted with both the H5 topology and the High Efficient and Reliable Inverter Concept (HERIC) topology. This compelling evidence affirms the effectiveness of the proposed configuration in proficiently mitigating leakage current.

Keywords: Photovoltaic; Common Mode Voltage; Leakage Current; Grid Connected Inverter

1 Introduction

Grid-connected photovoltaic inverters are integral components of solar power systems, facilitating the conversion and transfer of solar-generated electricity to the electrical grid. Beyond their primary function of power transfer, these inverters are equipped with essential islanding protection capabilities, ensuring uninterrupted operation in the event of grid faults. Islanding protection involves the inverter's ability to detect irregularities in grid conditions, such as voltage or frequency fluctuations, and swiftly disconnect from the grid to prevent potentially dangerous islanded operation. This protective feature not only upholds the grid's integrity but also enhances the reliability and safety of the entire photovoltaic system. Consequently, grid-connected photovoltaic

inverters play a crucial role in seamlessly integrating solar energy into the existing electrical infrastructure, all while ensuring operational stability and security[1,2]. Compared to isolated grid-connected inverters, non-isolated grid-connected inverters do not have line-frequency transformers, which give them advantages such as high efficiency, low cost, and compact size[3]. The high frequency switching of power devices results in high-frequency common-mode voltage. In practical applications, a photovoltaic array consists of multiple photovoltaic modules connected in series and parallel, which introduces significant parasitic capacitance to ground. The high-frequency common-mode voltage acts on the ground parasitic capacitance of the photovoltaic modules, generating high-frequency common-mode current, known as leakage current[4].

High-frequency leakage current causes severe conduction and radiation interference in photovoltaic systems, increases harmonics in grid current, and leads to system losses[5]. In severe cases, it can pose a threat to personal safety. Suppressing leakage current in photovoltaic systems is one of the key issues in non-isolated photovoltaic inverter grid integration[6,7]. The most common method to suppress leakage current is by modifying the inverter topology and constructing a new freewheeling path. During the freewheeling stage of the inverter switching cycle, the output side of the photovoltaic cells and the grid side are decoupled to prevent the formation of a common-mode loop. The most representative topology structures for this purpose are the H5, H6, and HERIC topologies[8–10]. These topologies change the transmission path of the freewheeling path by increasing the number of switch devices, thereby suppressing leakage current.

This study proposes an improved non-isolated single-phase full-bridge inverter topology by adding two switch devices at the midpoint of the DC bus voltage and incorporating diode freewheeling paths on the AC side. This modification ensures that the voltage at the midpoint of the bridge arm is equal to half of the DC voltage, thereby maintaining a constant Common-Mode Voltage in the inverter system and eliminating leakage current. The working principle and operational states of the improved topology are analyzed in detail, and a comparison of losses is made with the existing efficient H5 and HERIC inverter topology. Finally, a simulation-based comparative analysis is performed between the proposed topology and the existing H5, HERIC topology to evaluate their performance in suppressing leakage current.

The remaining sections of the paper are organized as follows, in section 2 we are proposing the related work, in section 3 we are describing our model description along with various subtitles to justify the proposed work. In section 4, we did comparative analysis with current art of work; moreover, the simulation and conclusion have been carried in section 5 and 6 respectively.

2 Related work

The H5 topology adds a switch to the H4 Bridge. Its drawback is that the current must flow through the added switch during grid integration, leading to increased conduction losses. However, the H5 Bridge requires the least number of additional switches among other topology structures, has a simple control method, and lower cost.

The H6 Bridge has been extensively studied and improved by adding two switches; a freewheeling path is formed to maintain decoupling between the photovoltaic panels and the grid. The H6 topology has various forms, but the optimal switching sequence of the switches needs to be determined to achieve maximum efficiency. Further efficiency improvements are limited by the performance of MOSFETs and IGBTs.

The HERIC topology proposed by Sunway's company incorporates two additional switches between the output terminals, acting as large impedance in the common-mode loop and reducing the leakage current to a lower level. The advantages of the HERIC topology include high efficiency and maintaining low harmonic distortion of the unipolar modulation current. It does not introduce additional switch losses during grid-connected operation[11,12]. The HERIC topology can be seen as a change in the AC circuit, while the structures of the H5 and H6 bridges aim to suppress leakage current by modifying the DC circuit topology. In[13–16] the researchers suggested different approaches to reduce the harmonics, leakage current and conduction losses, however the designed circuit process is too complex to respond rapidly, hence might not be the optimum solution in real time applications. In[17] the authors proposed a model to minimize the leakage current, however the approach is too complex to respond in real time application and may not find optimum use in industrial applications. Yue et al[18] presented an approach to reduce leakage current for single phase. This paper aims to tackle the challenge of reducing leakage current in non-isolated photovoltaic grid connected inverters. Our proposed approach entails a unique circuit design integrating extra switches and adjusting switch drive signals at the midpoint of the DC bus voltage. This alteration effectively modifies the common-mode current path, resulting in the mitigation of leakage current within the system.

3 Methodology

3.1 Proposed Approach

The Proposed approach has various folds to explain the concept of the suggested design briefly and clearly.

3.2 Analysis of Leakage Current Generation

The analysis of leakage current in single-phase and three-phase systems follows a similar basic procedure. In this study, we take the non-isolated single-phase full-bridge grid-connected inverter as represented in Figure 1 **(a)** to explain the process of leakage current generation and its calculation formula. In the diagram, E represents the grid voltage, L_a and L_b denotes the grid interface inductances, C_{PV} represents the parasitic capacitance to ground of the photovoltaic array, C represents the parasitic capacitance between the output terminals of the single-phase bridge and ground, and L_g represents the ground inductance of the inverter and grid circuit.

Figure 1**(b)** visually portrays the single-phase system. Here, U_{cm_ab} represents the common mode voltage, and U_{dm_ab} represents the Differential-Mode Voltage. The calculation formulas are as follows:

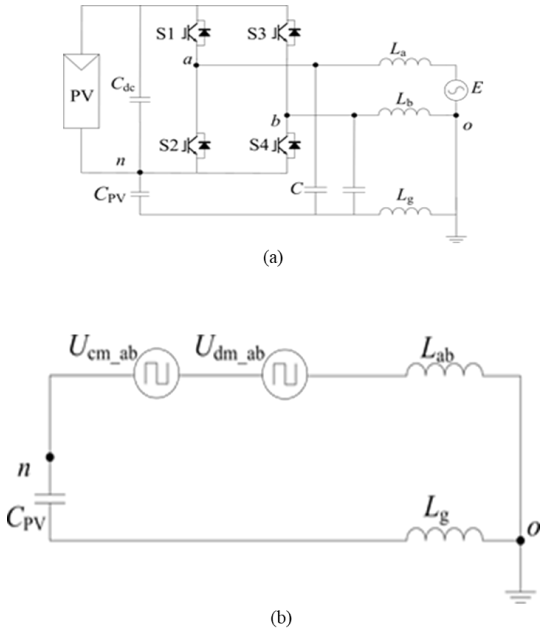

Fig 1. (a) Structure of non-isolated single-phase full bridge grid connected inverter, (b) Simplified common-mode model of single-phase system

$$U_{cm\_ab} = \frac{U_{an} + U_{bn}}{2} \tag{1}$$

$$U_{dm\_ab} = \frac{(U_{an} - U_{bn})(L_a - L_b)}{2(L_a + L_b)} \tag{2}$$

The total common-mode voltage of the system is:

$$U_{tcm} = U_{cm\_ab} + U_{dm\_ab} = \frac{U_{an} + U_{bn}}{2} + \frac{U_{ab}(L_a - L_b)}{2(L_a + L_b)} \tag{3}$$

As shown in Equation (3), when $L_a \neq L_b$ at that time, U_{dm_ab} directly affects the magnitude of the total common-mode voltage U_{tcm} in the system. However, in most cases, the grid interface inductances L_a and L_b have the same values, so Equation (3) can be represented as

$$U_{tcm} = U_{cm} = \frac{U_{an} + U_{bn}}{2} \tag{4}$$

The calculation formula for common-mode current is shown in Equation (5).

$$i_{cm} = C_{PV}\frac{dU_{tcm}}{dt} \tag{5}$$

When the value of U_{tcm} is constant, U_{tcm} can be considered as a DC source, the inductance is shorted, and the capacitor C_{PV} bears the voltage U_{tcm}. According to Equation (5), it can be concluded that the system's common-mode current is zero.

3.3 The composition and principle analysis of the improved topology

The composition and principle analysis of the improved topology are as follows:

The improved topology consists of a non-isolated single-phase full-bridge inverter with two additional switch devices added at the midpoint of the full-bridge DC voltage. Additionally, diode freewheeling paths are incorporated on the AC side. This modification ensures that the voltage at the midpoint of the bridge arm is equal to half of the DC voltage.

The working principle of the improved topology is based on maintaining a constant common-mode voltage in the inverter system to eliminate leakage current. When the common-mode voltage is constant, the common-mode voltage can be treated as a DC source, and the inductance is effectively shorted. The photovoltaic array's parasitic capacitance C_{PV} bears the voltage of the common-mode source. As a result, the system's common-mode current is eliminated, effectively suppressing leakage current.

By incorporating additional switch devices and modifying the topology, the improved topology alters the flow paths and voltage distribution in the inverter system, effectively reducing leakage current. The detailed analysis of the improved topology's working principles and operational states allows for a comparison of losses with existing high-efficiency topologies like the HERIC inverter topology. Through simulation-based comparative analysis, the performance of the improved topology in suppressing leakage current can be evaluated.

The proposed improved topology adds two switch devices and a full bridge consisting of four diodes to the foundation of the single-phase full-bridge topology, represented in Figure 2(**a**). In the diagram, E represents the grid voltage, L_a and L_b denotes the grid interface inductances, C_{PV} represents the parasitic capacitance to ground of the photovoltaic array, and L_g represents the ground inductance between the inverter and the grid. U_{an} and U_{bn} represent the potential differences between the midpoint of the bridge arm (a and b points) and the neutral point (n point).

3.4 Working Principle

Next, let us analyze the operation modes of the improved topology during one complete operating cycle. Figure 2 (**b**) illustrates the timing diagram of the switch driving signals in the improved circuit. During the positive half-cycle, switches S1 and S4 are turned on in high-frequency conduction, while the driving signals for switches S5 and S6 are complementary to those of S1 and S4. Switches S2 and S3 remain in the off state throughout the positive half-cycle. During the negative half-cycle, switches S2 and S3 are turned on in high-frequency conduction, while the driving signals for switches S5 and S6 are complementary to those of S2 and S3. Switches S1 and S4 remain in the off state throughout the negative half-cycle. When all the switches S1 to S4 are turned off, and the output voltage U_{ab} of the circuit is zero, it enters the freewheeling stage. Switches S5 and S6, along with diode bridge D1-D4, provide a freewheeling path for the inductive current.

Table 1 illustrates the switching states and voltage parameters of the six switch devices S1 to S6 during one complete operating cycle. From the table, it can be observed that the Common-Mode Voltage U_{cm} remains constant at $U_{PV}/2$, satisfying the theoretical condition for zero CommonMode Current. Figure 3 **(a) - (d)** represents the four operational modes of the improved circuit during one operating cycle, with the Common-Mode Voltage calculated using Equation (4) for each mode.

Table 1. Switch states and voltage parameters for improved topology S1 - S6

$S1$	$S2$	$S3$	$S4$	$S5$	$S6$	U_{an}/V	U_{bn}/V	U_{cm}/V	U_{ab}/V	
1	0	0	1	0	0	U_{PV}	0	$U_{PV}/2$	U_{PV}	P
0	0	0	0	0	1	$U_{PV}/2$	$U_{PV}/2$	$U_{PV}/2$	0	
0	1	1	0	0	0	0	U_{PV}	$U_{PV}/2$	$-U_{PV}$	N
0	0	0	0	1	0	$U_{PV}/2$	$U_{PV}/2$	$U_{PV}/2$	0	

Operational Mode 1: During the positive half-cycle, the circuit outputs positive voltage. Switches S1 and S4 are conducting, while the remaining switch devices are off. The photovoltaic modules transfer power to the grid, as shown in Figure 3 **(a)**.$U_{an} = U_{PV}, U_{bn} = 0, U_{ab} = U_{PV}$, The common-mode voltage is $0.5U_{PV}$.

Operational Mode 2: During the positive half-cycle, the circuit outputs zero voltage. Switches S1 to S4 are off, and switches S5 and S6 are conducting. S5, S6, and diode bridge D1-D4 provide a path for the inductive current, similar to Mode 1. Due to the connection of switches S5 and S6 to the midpoint of the two voltage-dividing capacitors in the DC link, the potential at the midpoint of the bridge arm is half of the photovoltaic output voltage U_{PV} i.e., $U_{an} = U_{bn} = 0.5U_{PV}, , U_{ab} = 0$. The common-mode voltage is $0.5U_{PV}$.

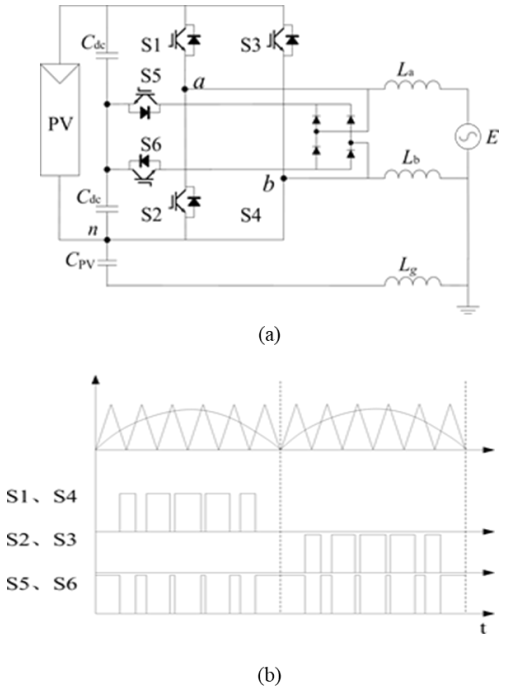

Fig 2. (a) Topology of improved single-phase inverter, (b) Driving signal of improved circuit

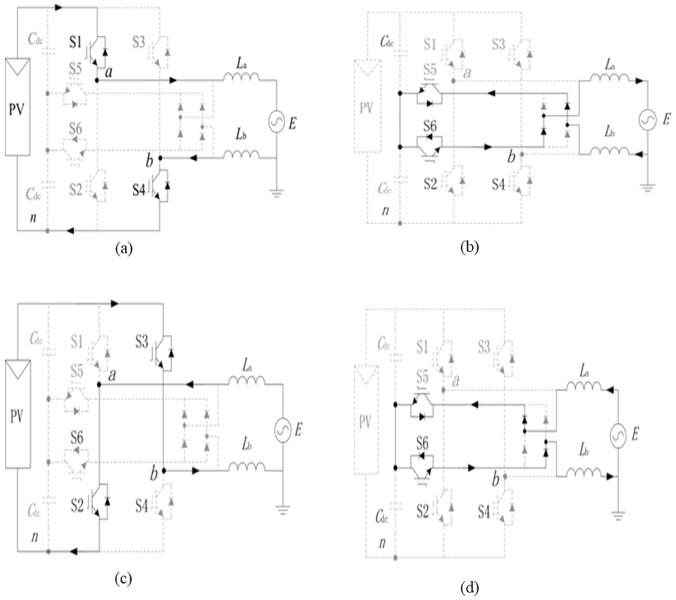

Fig 3. (a) Power exchange state in positive half-cycle, (b) Zero voltage state in positive half-cycle, (c) Power exchange state in negative half-cycle, (d) Zero voltage state in negative half-cycle

Operational Mode 3: During the negative half-cycle, with the output voltage being negative, $S2$ and S3 are conducting while the remaining switches are turned off. The photovoltaic module delivers power to the grid, as shown in Figure 3 **(c)**. $U_{an} = 0, U_{bn} = -U_{PV}$, $U_{ab} = 0$. The Common-Mode Voltage is 0.5 times U_{PV}.

Operational Mode 4: During the negative half-cycle when $U_{ab} = 0$, $S1 - S4$ are turned off, and S5 and S6 are conducting. Switches S5 and S6, together with diode bridge D1-D4, provide a path for inductive current, which flows in the same direction as in operating mode 3, as shown in Figure 3 **(d)**. The midpoint voltage of the bridge arm is half of the photovoltaic output voltage, $U_{an} = U_{bn} = 0.5U_{PV}$. The Common-Mode Voltage is 0.5 times U_{PV}.

The analysis of different working states within a complete operating cycle demonstrates that in the improved topology, during the freewheeling stage, due to the connection of S5 and S6 to the midpoint of the DC-side voltage division capacitor, the voltage difference between the midpoint and the n-point of the bridge arm (U_{an}) and (U_{bn}) is half of the photovoltaic module's output voltage. The Common-Mode Voltage remains constant throughout the entire operating cycle in all four working states, behaving like a stable constant current source, thereby suppressing Common-Mode Current and optimizing the topology's Common-Mode characteristics.

4 Comparative Analysis

4.1 Comparison with H5 topology

The H5 inverter and HERIC topologies are presented in Figure 4**(a)** and **(b)** respectively, and Figure 4 **(c)** represents the Signaling waveforms of the H5, the switch states and voltage parameters of its five switches S1-S5 are presented in Table 2 aiming to mitigate leakage currents in single-phase transformerless PV systems. The H5 converter topology, consisting of five switching elements, is created by adding a fifth switching element to the main full-bridge (H-bridge) inverter on the DC side. This added fifth switch is controlled at high frequencies to create zero-crossing transitions, thereby preventing reactive power flow between the DC input current capacity and the filter inductance at the inverter output. Furthermore, thanks to the fifth switch, the PV module is isolated from the circuit during zero-voltage transitions.

The H5 inverter topology has five switching elements (S1 - S5), where S1 and S3 are triggered at the grid frequency, while S2, S4, and S5 are subjected to high-frequency switching operations. The operational states of the H5 inverter topology are categorized under four headings. The operational state is referred to as the active state, where the S5 switch is controlled at a high frequency, and the S1 switch is triggered at the grid frequency. The current flows through the S5-S1 and S4 switches.

Table 2. Switching status and voltage parameters of H5 topology S1-S5

$S1$	$S2$	$S3$	$S4$	$S5$	U_{an}/V	U_{bn}/V	U_{cm}/V	U_{ab}/V	
1	0	0	1	1	U_{PV}	0	$U_{PV}/2$	U_{PV}	P
1	0	0	0	0	0	0	$U_{PV}/2$	0	
0	1	1	0	1	0	U_{PV}	$U_{PV}/2$	$-U_{PV}$	N
0	0	1	0	0	0	0	$U_{PV}/2$	0	

In this operational state, $U_{ab} = +U_{PV}$, and the common-mode output voltage value (U_{cm}) is calculated as in Equation (6):

$$U_{cm} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}(U_{PV} + 0) = \frac{1}{2}(U_{PV}) \tag{6}$$

The operational state indicated in Figure 3 is termed as the freewheeling state, where the current flows freely through the S1 switch and the D3 diode.

In this operational state, $U_{ab} = 0$, and the common-mode output voltage value (U_{CM}) is calculated as in Equation (7):

$$U_{CM} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}(U_{PV} + 0) = \frac{1}{2}\left(\frac{U_{PV}}{2} + \frac{U_{PV}}{2}\right) = \frac{U_{PV}}{2} \tag{7}$$

The operational state indicated in Figure 2**(b)** is referred to as the active state, where the S5 switch is controlled at a high frequency, and the S2 switch is triggered at the grid frequency. The current flows through the S5-S3 and S2 switches. In this operational state, $U_{ab} = -U_{PV}$, and the common-mode output voltage value (U_{cm}) can be calculated using Equation (8):

$$U_{cm} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}(0 + U_{PV}) = \frac{U_{PV}}{2} \tag{8}$$

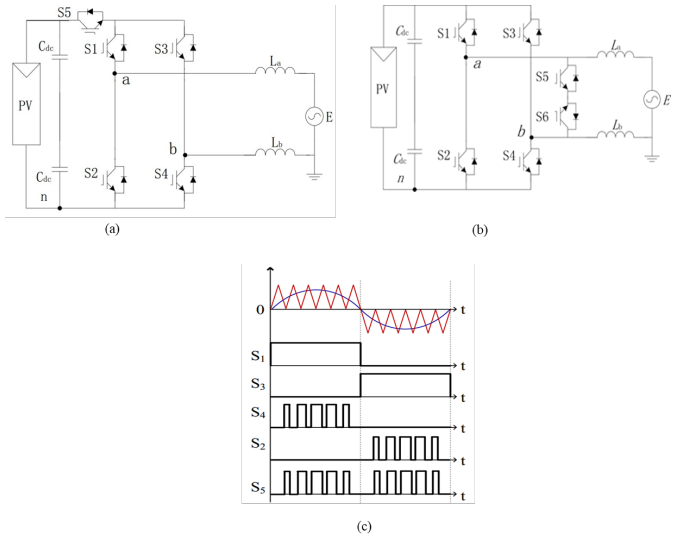

Fig 4. (a) H5 topology, (b) HERIC topology, (C) Signaling waveforms of the H5 inverter switching elements

The operational state indicated in Figure 3 is termed as the freewheeling state, where the current flows freely through the S3 switch and the S1 diode. In this operational state, $U_{ab} = 0$, and the common-mode output voltage value (U_{cm}) is calculated as in Equation (9):

$$U_{CM} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}\left(\frac{U_{pn}}{2} + \frac{U_{pn}}{2}\right) = \frac{U_{PV}}{2} \tag{9}$$

For the aforementioned switching states, it can be observed the U_{cm} (common-mode output voltage) remains constant at $\frac{U_{PV}}{2}$. Therefore, single-pole modulation technique can maintain the output voltage constant for the H_5 inverter. In Figure 4(**C**) the S1 and S3 switching elements are triggered at the grid frequency, S2, S4, and S5 are subjected to high frequency switching operations.

4.2 Comparison with HERIC topology

HERIC topology demonstrates high efficiency and outstanding ability to suppress leakage current, making it the most common non-isolated full-bridge inverter topology in practical applications. Therefore, we also compare the HERIC topology with the proposed improved topology in this paper. The HERIC topology is shown in Figure 4 (**b**), and the switch states and voltage parameters of its six switches S1-S6.

Each switch consists of an Insulated Gate Bipolar Transistor (IGBT) and an anti-parallel diode, so the conduction losses of the switches are composed of these two parts. When the switch turns on when the IGBT is closed, the on-state current I_C, flows through the IGBT, creating a saturated voltage drop $V_{CE(SAT)}$, the conduction loss is shown in Equation (10),

$$P_{CON\_IGBT} = V_{CE(SAT)} \times I_C \tag{10}$$

When the switch is turned off and the freewheeling diode conducts current I_F, the conduction loss of the diode is determined by the forward voltage drop V_F, as shown in Equation (11):

$$P_{CON\_D} = V_F \times I_F \tag{11}$$

Based on the analysis above, it can be concluded that both topologies have similar switch losses during power transmission. However, in the freewheeling state, the proposed topology in this paper has slightly higher losses compared to the HERIC topology.

Furthermore, it can be seen from Table 1 that when the improved topology transmits power to the power grid, there are two switching tubes in high-frequency action, and the IGBT generates conduction loss; in the freewheeling state, two IGBTs and two freewheeling diodes each generate conduction losses. It can be seen from Table 2 that when the HERIC topology

transmits power to the power grid side, there are also two switching transistors in high-frequency operation, and the IGBT generates conduction loss; in the freewheeling state, each has an IGBT and a freewheeling diode that produces conduction losses. From the above analysis, it can be seen that the switching loss of the two topologies is roughly the same when in the power transmission state; however, when in the freewheeling state, the topology loss proposed in this paper is slightly greater than that of the HERIC topology.

5 Simulation Results

To validate the feasibility of the proposed improved topology and modulation scheme, as well as its ability to effectively suppress leakage current, MATLAB/Simulink simulations were conducted for all the three, H5 topology, HERIC topology and the improved topology. The simulation step size was set to 0.1 μs, the switching frequency was 10 kHz, and the system parameters were as follows:

1. Input DC voltage: $U_{PV} = 350V$.
2. DC bypass capacitor: $C_{dc} = 250\mu F$.
3. Grid interface inductance: $L_a = 1.8mH$, $L_b = 1.8mH$.
4. Parasitic capacitance of the photovoltaic array: $C_{PV} = 100nF$.

Figure 5**(I) (a)**, Figure 5**(II) (a)** shows the simulated waveforms for the H_5 topology, HERIC topology, and Figure 5 **(II) (b)** shows the simulated waveforms for the proposed improved topology. Multiple voltage parameters waveforms (U_{an}, U_{bn}), and U_{cm}) for all the three topologies are presented.

From Figure 5**(I) (a)**, Figure 5**(II) (a)** it can be observed that the voltage difference between the midpoint of the H_5, HERIC topology bridge arms (U_{an} and U_{bn}) exhibits significant oscillations, deviating considerably from the theoretical values provided in Table 2 (around 150 V). The Common-Mode Voltage also fluctuates significantly, as shown in Figure 5**(I) (a)**, Figure 5 **(II) (a)**. On the other hand, Figure 6 **(a)** demonstrates that the proposed improved topology's midpoint voltages (U_{an}) and $U_{bn})$ match the calculated values from Table 1. U_{an} exhibits two amplitude values within the positive half-cycle (P): U_{PV} and $U_{PV}/2$, and two amplitude values within the negative half-cycle $(N) : 0$ and $U_{PV}/2$.

The amplitude of U_{bn} within a complete cycle also follows the values from Table 1, with the same analysis process as U_{an}. The Common-Mode Voltage fluctuation in the improved topology is minimal, remaining approximately constant at 175 V.

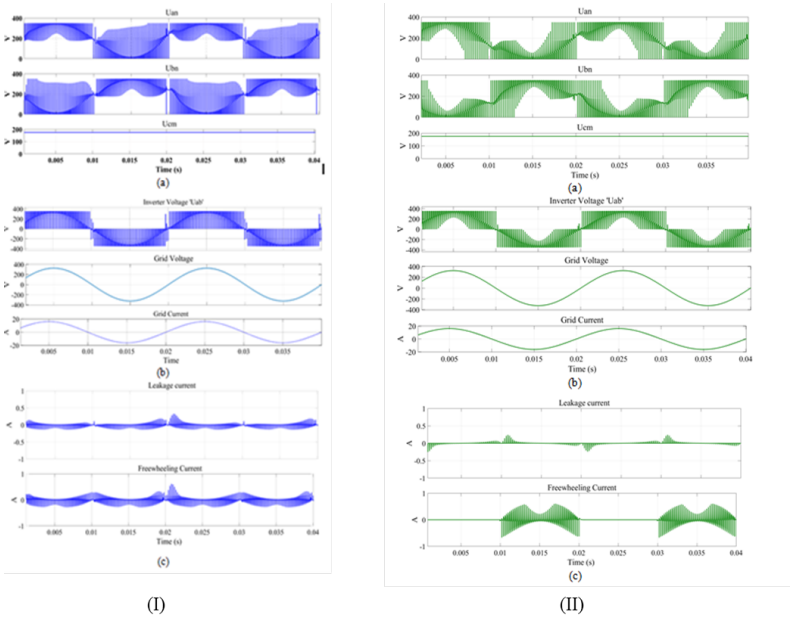

Fig 5. (I): Simulation results of $H5$ topology- (a) U_{an}, U_{bn}, and U_{cm} , (b) Inverter voltage, grid voltage & grid current, (c) earth leakage, freewheeling current. (II): Simulation results of HERIC topology- (a) U_{an}, U_{bn}, and U_{cm} , (b) Inverter voltage, grid voltage & grid current, (c) earth leakage, freewheeling current

Figure 5**(I) (c)**, Figure 5**(II) (c)**, and Figure 6 **(c)** depict the freewheeling current waveforms for the topologies. From figures, it can be observed that in the H5 and HERIC topologies, the freewheeling current magnitude is equal but with opposite directions in the positive and negative half-cycles.

Whereas Figure 6**(c)** demonstrates that in the improved topology, the freewheeling current direction remains the same throughout a complete operating cycle, consistent with the theoretical analysis in Figure 5. The minimum current is around 0.2 A, and the maximum current is approximately 11.71 A. Figure 5**(I) (b)**, Figure 5**(II) (b)**, and Figure 6 **(b)** show the inverter output voltage, grid voltage, and grid current waveforms for the topologies.

Moreover Figure 5**(I) (c)**, Figure 5**(II) (c)**, and Figure 6**(c)** show the leakage current waveforms for each of the three topologies. As can be seen from the leakage current waveform of the H5 topology, HERIC topology, the leakage current size is about 0.25 A, which is lower than the standards but not completely eliminated. From the leakage current waveform of the improved topology in Figure 6 **(c)**, it can be seen that although the leakage current is eliminated, the amplitude is small, about 0.04 A.

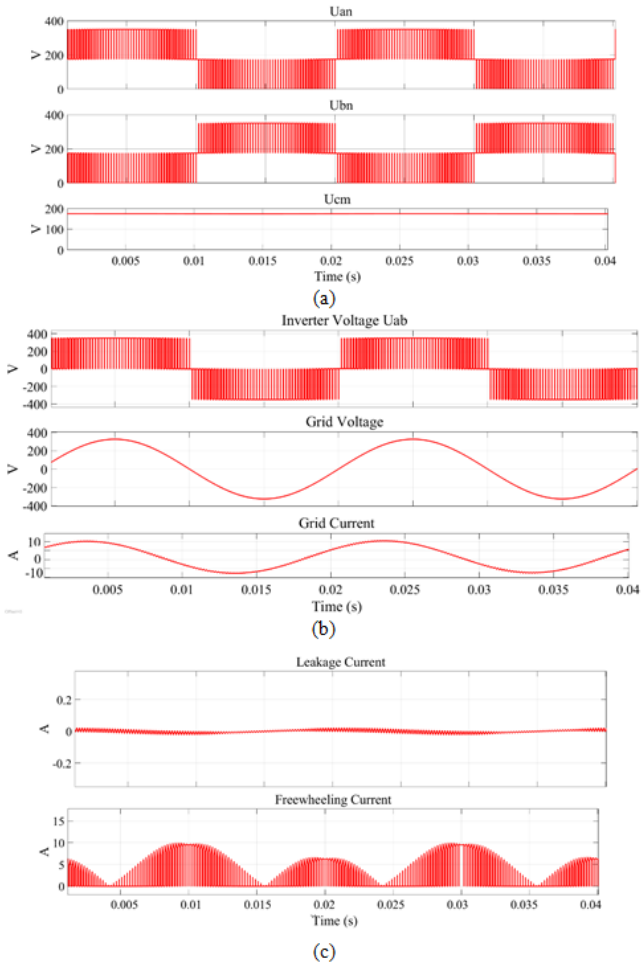

Fig 6. Simulation results of proposed topology- (a)U_{an}, U_{bn}, and U_{cm} , (b) Inverter voltage, grid voltage & grid current, (c) earth leakage, freewheeling current

To provide a more intuitive comparison, Fast Fourier transform (FFT) analysis was performed on the grid current waveforms for each topology. Figure 7 shows the FFT spectrum for the grid current, From the figure it can be seen that the total harmonic distortion (THD) of the grid current are 0.9%, 0.83% for the H5 and Heric topologies and 1.03% for the improved topology, all of the three meet the grid requirements, indicating good output voltage waveforms.

From Figure 8 it has been observed that the proposed method has better output response when compared to the current art of work, since it reduces the hardware and switching timing of devices employed. Furthermore, here the two commonly

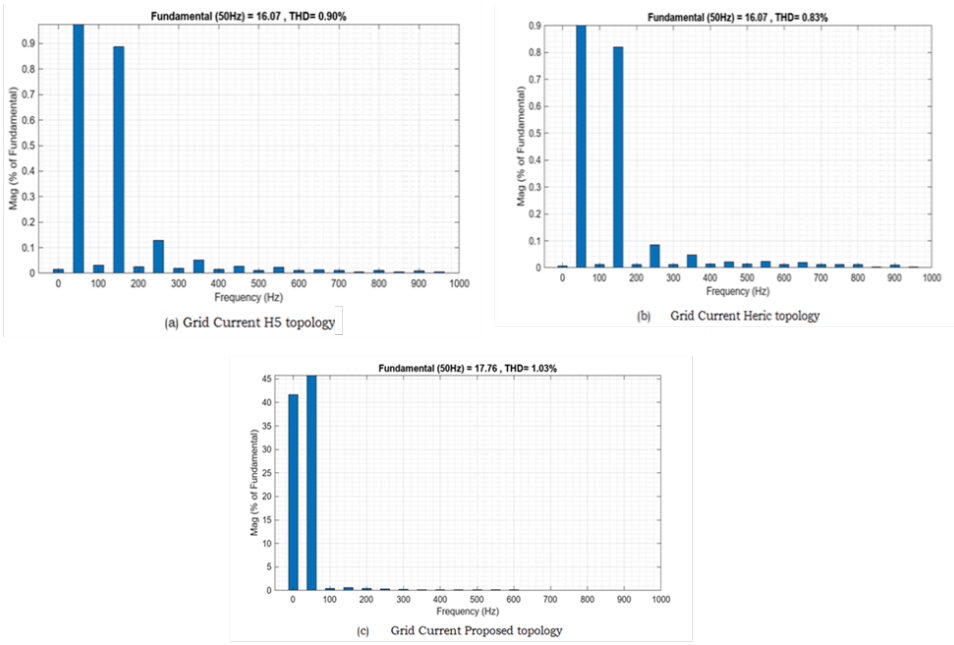

Fig 7. FFT spectrum of grid current

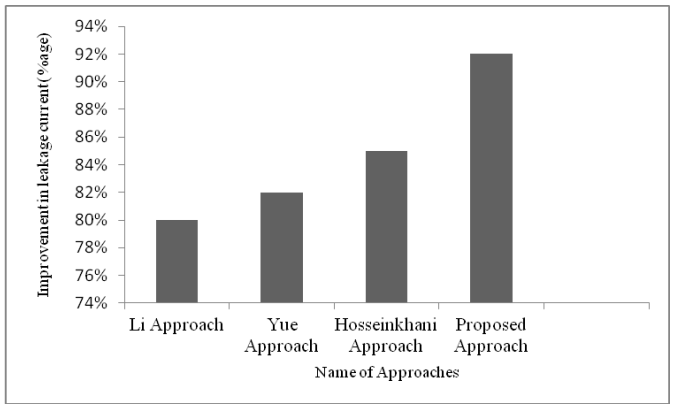

Fig 8. Comparative analysis of various approaches

used topologies that are employed to reduce the leakage current have discussed and compared in section 5. Furthermore, from section 5, it has been observed that the leakage current has minimized to an extent, which is tolerable to the desired circuit, and does not affect the performance of the chosen system design. Through comparison, it can be seen that the improved topology and modulation method proposed in this paper have high feasibility, can effectively suppress the peak of leakage current, and the safety margin of grid-connected inverter system operation has been greatly improved.

6 Conclusion

This research introduces a novel adaptation to the conventional configuration of a six-switch non-isolated single-phase full-bridge photovoltaic grid-connected inverter. The enhancement entails integrating two switching diodes and a diode bridge, each comprising four diodes, into the standard full-bridge inverter setup. Notably, these supplementary components are intricately linked to half of the voltage divider capacitance on the DC side. The innovation of this modification lies in its capacity to enhance the performance and efficiency of the inverter while preserving its structural integrity. Through the incorporation of additional diodes and a diode bridge into the circuit design, the proposed topology offers several distinct advantages.

Firstly, it improves the inverter's ability to manage voltage fluctuations and enhance overall stability during grid-connected operation. Secondly, it facilitates more efficient power conversion and transfer, thereby maximizing energy yield from the photovoltaic system. Additionally, the modification contributes to simplifying the system and reducing costs, rendering it a practical and economically viable solution for grid-connected solar applications In conclusion, the introduction of this modified topology signifies a significant advancement in the domain of photovoltaic grid-connected inverters. Its innovative integration of supplementary components and strategic placement within the circuitry enhances performance, efficiency, and cost-effectiveness, thus driving progress towards enhanced utilization of solar energy in residential and industrial applications.

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