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RESEARCH ARTICLE

Design, Implementation and Performance Analysis of Test Pattern Generator for Built-In Self-Test using m-GDI Technology

Y G Praveen Kumar[1]*, B S Kariyappa[2], M Z Kurian[3]

1 Assistant Professor, Department of Electronics & Communication Engineering, Sri Siddhartha Institute of Technology, SSAHE, Maraluru, 572105, Tumakuru
2 Professor & Head, Department of ECE, R V College of Engineering, Bengaluru, 560059, Karnataka
3 Professor & Head, Department of ECE, Sri Siddhartha Institute of Technology, SSAHE, Maraluru, 572105, Tumakuru

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* **Corresponding author**.

praviraj.star@gmail.com

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Abstract

Background: A Linear Feedback Shift Register (LFSR) is typically used for generating the test patterns in built-in self-test (BIST) as it produces pseudo-random patterns at every clock cycle. These pseudo-random patterns are used as test vectors for testing the VLSI circuits. **Objective:** The pseudo-random patterns generated by the LFSR exhibit low-correlation among the patterns, this increases the switching activity and power dissipation while testing the VLSI circuit. Thus, to reduce the testing power, modified gate diffusion input (m-GDI) logic based LFSR in 45nm technology is proposed in this paper. **Methods:** The circuits are developed on m-GDI technology using the Cadence virtuoso tool and a spectre simulator is used to carry out the simulation. **Findings:** Comparative analysis revealed that the delay and power are reduced significantly, for the proposed design when compared to the existing LFSRs in conventional CMOS, GDI and reversible logic. **Novelty and applications:** In conventional LFSR, an external source is necessary to load the seed value and it dissipates more power. But in the proposed design, the seed value is generated by the circuit itself. This reduces the power and critical path delay. Further a complete zero patterns is not possible in conventional LFSR design. But in proposed design, all zero pattern is plausible. The design obtained from this study can be applied in low-power, high-speed BIST circuits.

Keywords: LFSR; Seed Value; Test Patterns; Built-In-Self-Test; m-GDI

1 Introduction

BIST is more suitable for testing the digital circuits as it provides a wide range for low-power designs. A Linear Feedback Shift Register (LFSR) is generally used in BIST as a test vector generator for spawning the test vectors. During every clock cycle, LFSR generates a random sequence that can be used as test vectors for testing the Circuit-

Under-Test (CUT). Having carefully selected feedback polynomial, LFSR generates the random patterns which attain high fault coverage in a moderately small run of test patterns. Flip-Flops (FF) are the rudimentary component for realizing LFSR[1]. As the FFs have a deterministic operation, the stream of test patterns spawned by the LFSR is entirely governed by its present and preceding value. Furthermore, LFSR produces repeating patterns after it clocked through 2^n - 1 cycles where n represents the number of flip-flops used in LFSR[2,3]. The only input needed by the LFSR to produce the test vectors is the clock signal.

Different techniques and methodologies are proposed for implementing the test pattern generator that aims at reducing power, delay and area. Different logics like transmission gate logic, pass transistor (PT) logic, gate diffusion input (GDI) logic can be used to generate test patterns. PT and GDI technique-based test pattern generators perform better in terms of delay, power and area than the conventional CMOS design[4,5]. But these techniques are not compatible with the standard CMOS fabrication process and eventually increase the complexity in the fabrication. With slight modification in the architecture of LFSR, highly random patterns can be achieved[6–8]. But this increases the area and complexity with increased length. LFSR based on the bit swapping technique is presented in[9]. Bit swapping reduces the power but at the cost of area overhead. Thus, it is observed from the literature that, power, delay and area exhibit the trade-off.

To address these issues, in this research paper m-GDI based LFSR is proposed which reduces the power and delay when compared to conventional CMOS logic.

2 Basics of m-GDI

There are many methods to optimize the power. One such method is m-GDI technique. In this technique, a basic m-GDI cell is used to build all the circuit components. m-GDI technique allows us to apply more than one input (G, P and N) unlike CMOS logic where only one input can be applied. This reduces the number of transistors being used for the design and thereby power and area are reduced. The basic m-GDI cell is given in Figure 1.

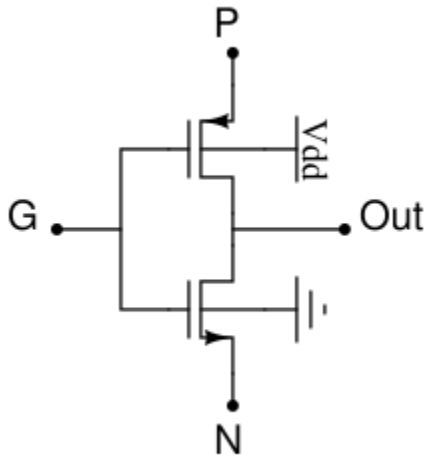

Fig 1. Basic m-GDI cell[10]

Modified GDI (m-GDI) cell contains two transistors i.e. NFET and PFET. Gates of NFET and PFET are shorted and it represents the 'G' terminal of the m-GDI cell. The source terminal of NFET and PFET represent the 'N 'and 'P' terminals of the m-GDI cell respectively. Also, the bulk of PFET is attached to V_{DD} and the bulk of NFET is attached to the ground. By applying different inputs and logic values to G, N and P terminals of m-GDI cell many functions can be realized.

Table 1 Illustrates the realization of different Boolean functions by applying different inputs to G, N and P terminals of the basic m-GDI cell. It also presents the transistor count for realizing different functions in CMOS logic and m-GDI logic. These functions entail around 6 -12 transistors in CMOS but in m-GDI, it is reduced to almost threefold.

Table 1. Function table [10–12]

N	P	G	OUT	Function	No. of Transistor	
					m - GDI	CMOS
'0'	B	A	$\overline{A}B$	Z_1	2	6
B	'1'	A	$\overline{A}+B$	Z_2	2	6
'1'	B	A	A + B	OR	2	6
B	'0'	A	A B	AND	2	6
C	B	A	$\overline{A}B+AC$	MUX	2	12
	B	A	$A \oplus B$	XOR	4	8

3 Proposed System Design and Implementation

LFSR should be loaded with an initial value (other than zero) which is referred to as seed value. Conventionally, the seed value is loaded into the LFSR through an external source and during every clock cycle, the output of LFSR will be shifted to the right by one position and the new value will be loaded into the first D-FF based on the characteristic polynomial. But in the proposed LFSR, a NOR gate is used to generate the seed value, thus no external circuit is required to load the seed value. During every clock cycle, the value stored in LFSR is shifted to the right and produces pseudo-random patterns based on the polynomial.

For implementing the proposed LFSR, basic gates such as Inverter, NAND, NOR and XOR gates are designed initially using m-GDI logic which uses less number of transistors and dissipates less power. This is followed by the design of master-slave D flip-flop (MSDFF) and proposed LFSR. All the designs are done in 45nm technology node with a supply of 1.2V.

3.1 Master-Slave D Flip-Flop (MSDFF)

DFF is the basic building block for designing the LFSR. Accordingly, m-GDI based DFF using 4 NAND gates and an inverter is developed and verified for its functionality. The transistor count for implementing m-GDI based DFF is 18(4 NAND gates utilize 16 transistors and an inverter uses 2 transistors).

m-GDI based DFF when used to implement LFSR results in an erroneous output because of the race around problem. And hence a master-slave DFF (MSDFF) is implemented using 2 m-GDI based DFF and 1 inverter. Thus the number of transistors entailed to realize MSDFF is 38(2*18 + 1*2). Schematic and the layout of m-GDI based MSDFF is shown in Figure 2 and Figure 3 respectively. The total net length used in the layout is 41.85μm and the chip area of the layout is 65.42 μm^2.

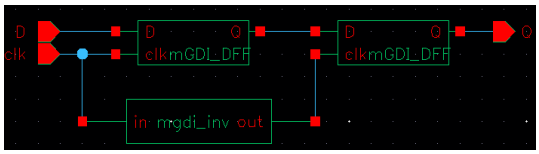

Fig 2. Schematic of m-GDI based MSDFF

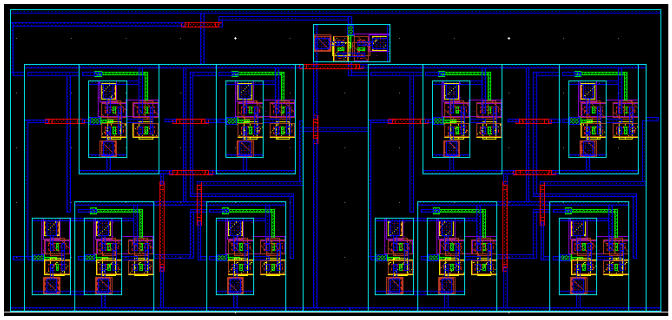

Fig 3. Layout of m-GDI based MSDFF

3.2 Proposed LFSR

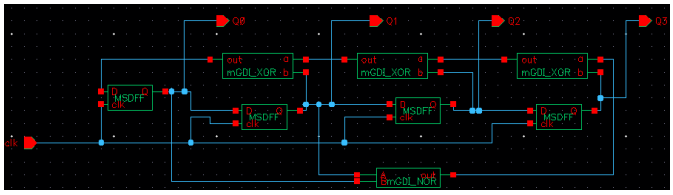

Fig 4. Schematic of Proposed LFSR

Figure 4 illustrates the circuit of 4-bit LFSR using a self-seeding scheme. It includes 4 MSDFF, 3 XOR gates and 1 NOR gate. Thus a total of 168 (4 *38 + 3 * 4 + 1 *4) transistors are entailed. The feedback polynomial chosen for implementing LFSR is $x^4 + x^3 + x^2 + 1$. The bit values that affect the subsequent state of LFSR are called the taps. The taps are XOR'd successively with the output value and then fed back to the first MSDFF as shown in Figure 4. It works on the falling edge of the clock viz. the value of the output bits is shifted to right at every negative edge of the clock and a new value is loaded into the first MSDFF which is determined by the output of NOR gate, 4^{th} ,3^{rd} and 2^{nd} MSDFFs. The input D_0 to the first MSDFF during every clock cycle can be expressed as Equation (1):

$$D_0(n) = Q_3(n-1) \text{ xor } Q_2(n-1) \text{ xor } Q_1(n-1) \text{ xor } \{Q_1(n-1) \text{ nor } Q_0(n-1)\} \quad (1)$$

Figure 5 illustrates the layout of the proposed 4-bit LFSR. The chip area of the layout is $645.63\mu m^2$ and the length of the wire used for developing the layout $362.21\mu m$. The layouts in Figure 3 and Figure 5 are optimized in area without violating any design rules.

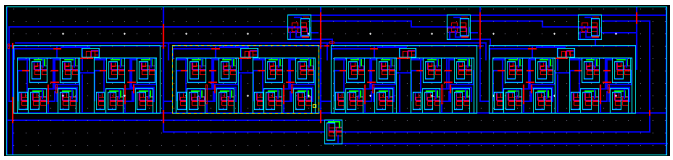

Fig 5. Layout of proposed LFSR

4 Results and Discussion

All the designs are done in 45nm Technology using Cadence virtuoso tool and functional verification is done using a spectre simulator at V_{DD} =1.2V.

Figure 6 represents the simulation waveform of 4-bit LFSR based on m-GDI technology. At every negative edge of the clock, the output bits (Q_0 to Q_3) of MSDFF are shifted to the right and the feedback mechanism loads the new value into the left-most MSDFF which represents the Q_0 bit. The last signal in Figure 6 (red colored signal) is the power signal from which peak power and total power is estimated.

Table 2. Performance metric of proposed LFSR

	Schematic	Layout
Delay(psec)	144.37	476.93
Peak Power(μw)	119.13	167.22
Dyn. Power(nW)	227.05	439.55
Static Power(nW)	4.147	4.147
Total Power(nW)	231.2	443.7

The performance metric of the proposed LFSR in schematic and layout is given in Table 2. From the table, it is evident that the delay and power values are slightly more in layout (AV Extracted view) than the schematic because of parasitic resistance and capacitance.

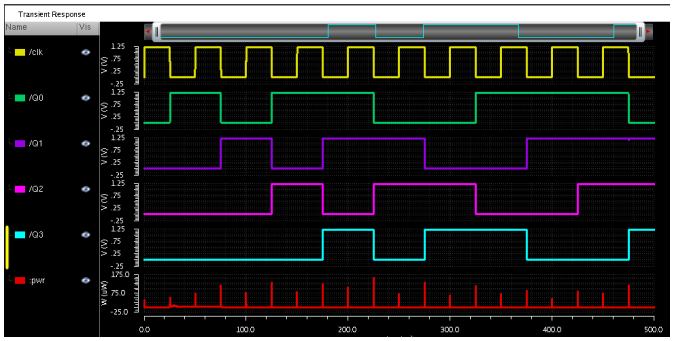

Fig 6. Simulation waveform of proposed LFSR

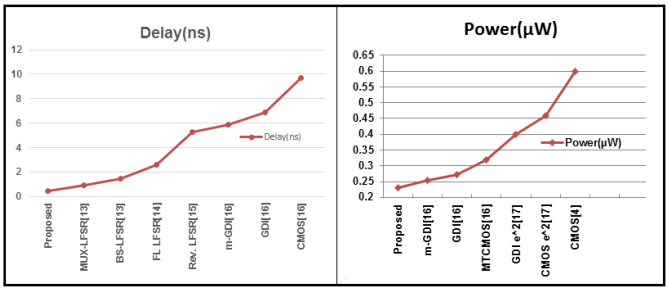

Fig 7. Delay and Power comparison of proposed LFSR with existing designs. *Footnote: FL-LFSR: Fuzzy Logic based LFSR, BS-LFSR: Bit Swapping LFSR, MUX- LFSR: MUX based LFSR, Rev- LFSR: Reversible Logic based LFSR, GDI-LFSR: GDI based LFSR.*

Figure 7 illustrates the delay and power analysis of the proposed design with existing literature. The critical delay in the proposed design is reduced by 67.56%, 81.75%, 90.94%, 91.87%, 93% and 95.06% when compared with LFSRs using bit-swapping technique[13], fuzzy logic[14], reversible logic[15], m-GDI logic[16], GDI logic[16] and conventional CMOS logic[16]. In the same way, power is also reduced by 9.8%, 43.9%, and 61.6% in proposed LFSR when compared to the m-GDI, GDI and CMOS based LFSRs presented in articles[16,17] and[4] respectively. Furthermore, the chip area in the proposed m-GDI based LFSR is reduced by 63% when compared with GDI based LFSR proposed in[17].

5 Conclusion

This study presents an implementation of 4-bit LFSR using m-GDI technology in 45nm technology. Conventionally initial value other than logic-0 needs to be loaded into the LFSR to generate pseudo-random patterns. But in the proposed LFSR, the seed value is generated by the LFSR itself. The results obtained have proved that the delay and power in the proposed design are reduced by 95.06% and 61.6% respectively when compared to the conventional CMOS based designs.

Thus, the proposed LFSR can be used to implement the BIST in high-speed and low-power applications, as m-GDI based design reduces the critical delay and dissipates less power than conventional CMOS logic. Also, it can be used to devise a parallel sequence generator in Cryptology applications.

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