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RESEARCH ARTICLE

12-Bit Clock Gated SAR-ADC for Bio-Medical Applications

Jyoti Sehgal[1]*, **Manoj Kumar**[2]

1 Research Scholar, UIET, MDU, Rohtak, Haryana, India
2 Assistant Professor, UIET, MDU, Rohtak, Haryana, India

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* **Corresponding author**.

jyotiece.rs.uiet@mdurohtak.ac.in

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Abstract

Background/Objectives: Power optimization is a critical design criterion in modern integrated circuits. The unwanted clock signals are neutralized and the reduction in power consumption is made presumable by using the clock gating technique. **Methods:** Analog-to-digital converters (ADCs) are important components in these systems. A widely used successive approximation register A/D converter includes an internal clock, reference, and high resolution. The number of redundant cycles is increased with improved resolutions but enhances the consumption of power. Thus, the clock gating strategy is used to substantially lower the circuit's dynamic power consumption. The clock gating technique is implemented with a reduced number of transistors to minimize the overhead with high switching activity. Also, demonstrate no imperfection on the clock duty cycle. **Findings:** A 12-bit clock gated SAR register using a D-flip flop with 1.8 V supply voltage is proposed in this study for efficient biomedical applications. SAR without a clock gating technique consumes 54 μW of power and SAR with a clock gating technique consumes a power of 22.68 μW. **Novelty:** The clock gating technique is stipulated to minimize power consumption of clock gated SAR-ADC and improves the battery life of the portable device.

Keywords: Clock gated technique; power consumption; resolution; SARADC; successive approximation register

1 Introduction

Because of the upsurge in chip complexity, reduced power and small size are major contradictions in modern integrated circuits. Multitudinous proposed techniques capitulate low-power operation with minimized signal switching activity. The clock system is one of most power swallowing submodules in VLSI circuits, thus the proposed clock gating technique is a useful approach to different hierarchical levels to reduce power consumption as well as diminish the number of transistors with reduced switching activity. An A/D converter plays a vital role in transferring analog signals to digital codes in Bio-Medical applications, VLSI systems, and wireless systems [1,2]. In comparison with other ADCs, successive approximation register (SAR) ADC is mostly used ADC in Bio-Medical applications like Bio-Medical sensors, medical imaging, data acquisition systems, and implanted biomedical devices like a pacemaker [3].

Low-frequency analog signal conversion demands ultra-low-power operation (e.g., in nW range). The binary search algorithm [4] is the basic principle on which successive approximation register ADC mainly works. Following [Figure 1] presents a process design model of SAR-ADC.

The four major blocks in [Figure 1] are the Sample and Hold circuit, comparator, DAC (Digital to Analog converter) capacitor logic, and SAR Control Logic. The conversion is completed in numerous clock cycles by SAR ADC, which uses the information from the last determined bit. Analog values are stored in the sample hold circuit. It gives a constant voltage to the comparator during conversion. The basic purpose of the comparator is to compare both the outputs from digital to analog converter V_{dac} and from the sample and hold circuit V_{hold}, and generates the output in the digital form of either '0' or '1' which is provided to SAR Logic. The binary search algorithm is implemented by the SAR logic. SAR logic gives the output in binary format which is further converted to the corresponding analog value using DAC and given to the comparator. All the devices utilized in SAR ADC consume a lot of power. Thus various techniques like clocking system, reducing the leakage, and logic reordering are used to resolve the challenge regarding consumption of the power. In this paper, a 12-bit clock gated SAR analog to digital converter is designed on 180nm CMOS technology at a 1.8V supply.

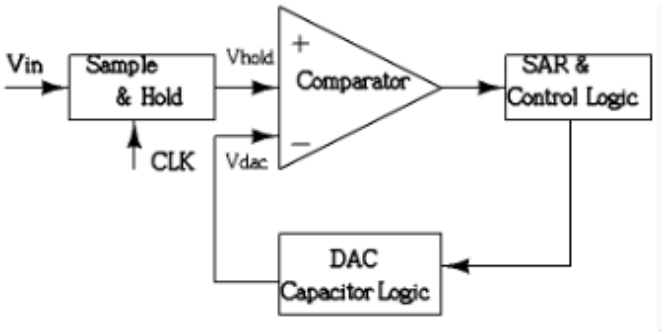

Fig 1. Model of Successive Approximation Register ADC

Erkan Alpman et al. [4] present a C-2C SAR ADC that culminates in high performance by using a small-area architecture and conquering a high device threshold. Shuo-Wei Michael Chen et al. [5] provide a high-speed (600-MS/s) and medium-resolution (6-bit) conversion using improved ADC. Zhiheng Cao et al. [6] present an ADC that achieves 6b performance without any digital post-processing. Mohamed O. Shanker et al. [7] proposed a clock gating SAR ADC. It can reduce the redundant clock by activating the clock gated signal (Clkg) with a change in the state of the flip flop. This will cause a decrease in the dissipation of power. Magdy A. Bayoumi et al. [8] the clock signal is implemented using a register with no data switching activity. It operates with fewer transistors and no redundant transitions which makes it suitable for low-power applications. Mohamed O. Shaker, and Magdy A. Bayoumi [9] proposed a novel low-power clock gated flip flop to reduce the gating overhead. T.O. Anderson et al. [10] have discussed two basic types of logic one for the sequencer and the other for the code register as two separately distinguished items. Auxillary control logic is also used for speeding up the conversion cycle. A. Rossi et al. [11] proposed a non-redundant SAR ADC with a multiple-input n-bit shift register. It is essential to provide a mechanism that brings the shift register into the initialization state. One method of loading the initialization is to use flip-flop with reset and set lines connected to a control signal which if active, sets the MSB flip-flop and resets all other bits. To stop the conversion we can use OR chain applying to the LSB a control signal which if active forces '1' in all signals. So SAR operates in the memorization mode. The stop signal is useful in a particular when the last step of the approximation sequence is reached and the result of the conversion process gets stored. The output of the LSB flip-flop can be used to signal the end of the conversion. The proposed non- redundant SAR ADC saved up to 50% of the total area. Strollo et al. [12] proposed two clock gating techniques. Double Gating is the first technique that is performed individually on the master and slave latches. As the switching activity of the input signal is very low, the power dissipation gets reduced. A second technique is NC^2MOS Gating or Sequential Gating, in which the entire flip-flop requires only one gate logic. The NC^2MOS gated flip-flop saves 74 percent of the power when the input is idle, however, the double-gated flip-flop retains 64 percent. Due to its lower complexity, the NC^2 MOS gated flip-flop performs better than the double-gated flip-flop [13]. The clock gating flip-flop in a 16-bit counter saves up to 52% of the power while the 8-bit audio sampler NC2MOS gated flip-flop saves 16% of the power. Manoj et al. [14] have designed the SAR register in 180nm technology using the clock gating technique. By using clock gating, power was reduced from 54μW to 736.1nW. Due to the existence of redundant clocks in a conventional SAR, during the entire conversion process, every flip-flop changes its state once or twice. Such difficulty can be solved by the means of the clock gated flip-flop. The transition in clk states depends on frequency. Nandita

Srinivasa et al.[15] have used the Spartan 3 FPGA family, power has been calculated using the clock gated benchmark circuits. Despite an area trade-off, it has been observed that the power shrinks. Wing-Kong Ng et al.[16] proposed flip-flop technology with two dynamic latches in parallel connection improve the race tolerace, energy efficiency, and circuit compactness.

2 Methodology

2.1 Conventional SAR

The conventional Successive approximation Register[11] contains many N-bit ring counters and also multiplexer is connected with the kth FF to choose one data input coming from:

1) Right shift [(k+1)th FF output]
2) Load data (comparator output)
3) Memorization (kth FF output itself)

The operation of the 12-bit successive approximation register is given as: Initially, SAR assumed all the bits are '0' except MSB. MSB is assumed '1'. At the first clock cycle, the comparator allocated MSB a true value (x11), and the second MSB becomes '1'. Until then all the true values are allocated to MSB, and this procedure will continue. Equation (1) is realized to stop the conversion procedure by adding OR logic gate chain:

a0 = Stop

$$a(k) = a(k-1) + Q(k-1) \quad (1)$$

Equation (1) is used at the last conversion of the last step and its result is stored in SAR. Here we notice that every FF requires 'n' clocks to finish the conversion process which indicates that we require n^2 clocks for the whole conversion process. During the whole conversion process, the state of every FF varies once or twice and because of this, a large no. of redundant clock pulses occurs which dissipates power without affecting the FF[8].

2.1.1 Various Clock Gating Techniques

2.1.1.1 AND gate logic-based Clock gating . A gating clock is a common way to minimize power consumption. Because of the simplicity AND gate is mostly used gate logic is for the clock gating technique[14]. When the enable signal is high 4 bit counter increases its value by 1 count. Mostly the AND logic gate is utilized for negative edge triggering because, in positive edge triggering, glitches occur because of the larger falling time.

2.1.1.2 NOR gate Logic-based Clock gating . NOR gate is another important logic gated that is used for the gating clock technique. For clock gating purposes, we consider 2 inputs NOR logic gate. The O/P of the NOR gate is '1' When both the inputs are '1' only then the output is '1', otherwise, it will be '0'. A NOR logic gate[17] is utilized for positive triggered circuits.

2.1.1.3 D-type flip flop-based Clock gating. [Figure 2] shows the D flip-flop clock gating for the negative latch[18]. In this architecture, we use the XNOR logic gate and OR logic gate. Inputs of the XNOR gate are provided by the input D and output Q. The output of the XNOR logic gate is given to one of the inputs of the OR logic gate. The transition occurs due to different input and output logic. This design provides a low switching feature.

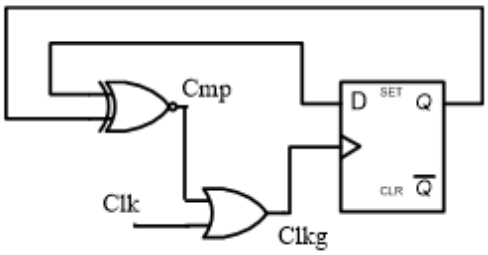

Fig 2. D-flip flop clock gating

2.2 Proposed Clock gated SAR methodology

The binary search algorithm is implemented by the SAR logic. Two different proposals are presented to design SAR control Logic. The first proposal is given by Anderson [11] in which a successive approximation Register consists of a shift register. This proposal is employed by '2N' flip-flops. The next proposal which comprises some combinational logic and 'N' no of flip-flops are presented by A. Rossi [11]. SAR Control logic works sequentially and produces output based on the resulting output of the comparator. Initially, MSB is set to '1' and DAC converts this digital value to the analog value and then the comparator compares this value with the sampled value [19]. Then it is the comparator's choice whether MSB remains the same or it changes to '0'. The same conversion process is repeated throughout the whole process. Here we notice that two clocks are active during each conversion.

2.2.1 The Transmission Gate Based D Flip Flop

D flip-flop is the fundamental unit of the Successive approximation register. For low power requirements, a D flip flop-based transmission gate is used [20]. To boost power efficiency, minimum size transistors are more efficient [21]. In the critical path, transistors whose threshold voltage is low are used and in the noncritical path, transistors whose threshold voltage is high are used to decrease the leakage power. High efficiency is thus given by this dual-threshold strategy.

2.2.2 Sequence and Code Register architecture

Successive approximation Register block diagram is shown in [Figure 3]. Two sets of registers used in this architecture are sequence registers or Sequencer and Code registers [22].

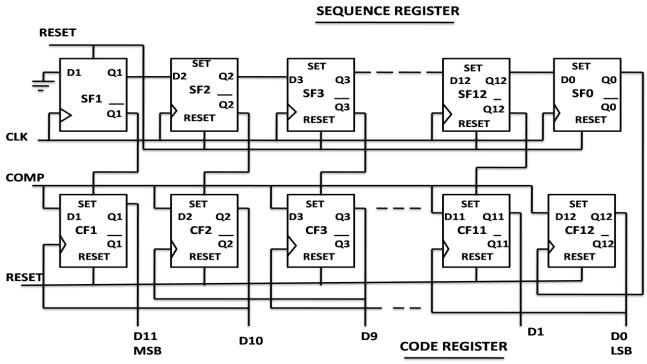

Fig 3. Block Diagram Successive Approximation Register

The sequence register is used for bit sequencing, while the code register retains bit values [23]. The Q bar output of the shift register is used to set the FFs of the code registers. Initially, the reset of the first FF of the sequence register is attached to the reset of the remaining FFs of the sequencer, and the set input of the 1st FF and reset of all the FFs of the code register [24]. Firstly, 0V supply voltage is provided to the reset input. O/Ps of the non-inverted and inverted are '0' and '1' respectively. The non-inverted output also determines the set input of CF1 and its output becomes 1 [25]. The MSB is stored in it and the weight for the full-scale range is 0.5Vref. Here we note that all sequence registers are reset, and all code registers except CF1 are set. Now, DAC generates its equivalent analog value. When the 1st clock pulse is triggered, reset goes high and output Q of the 1st FF becomes '0' as D input to the first flip is grounded and the output of SF2 is '1' [15]. Thus, the transition occurs from low to high. SF2 triggers CF1 and stores comparator output. When another clock pulse is applied, the FF of the code register retains the set value as SF2 output becomes '0'. This process is repeated for each flip-flop until the sequence register's FF outputs high logic after N clock cycles.

The traditional SAR possesses several redundant clock pulses. This happens because the state of every FF varies once or twice throughout the whole conversion process. The redundant clock pulses are reduced by the use of Clock gated FF.

The FF input gets the logic output and leaves the CLK signal isolated. In a particular period, the condition of the CLK signal is changed based on its frequency. As a result, many extra pulses occur that consume power. By using Clock gating FF, this issue can be solved as shown in [Figure 4]. The output Q is connected to the input D. By doing this, the Clkg signal is active if the FF decides to vary its state. The Clkg signal is inactive if the FF retains its condition. The n-FF Clock gated Successive

approximation register has (n+1)/3 controllers. [Figure 5] shows the proposed clock gated SAR register block diagram. Clkg signal is generated by the controllers to control a set of FFs. Each FF output is linked with the corresponding controller. Each FF output is connected for toggling operation to the FF input terminal. Each FF at the positive edge of its Clkg is triggered. Controller 1 and controller 2 are mostly similar to each other. Only one difference is that the transistor M10 is driven by Cin, whereas in controller 1 the transistor M8 is driven by Clk. In the controller, an additional transistor M9 is used which is driven by Qi.

Every controller has a gating overhead circuit. The gating overhead circuits contain pass transistors which are used for the propagation of the clock signal. The MSB loads the true value of the data, modifying its state. They often change their state as other bits load their real value or collect the data coming from the neighboring FF (shift right).

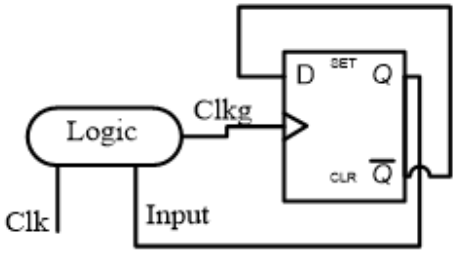

Fig 4. Clock Gated Flip Flop

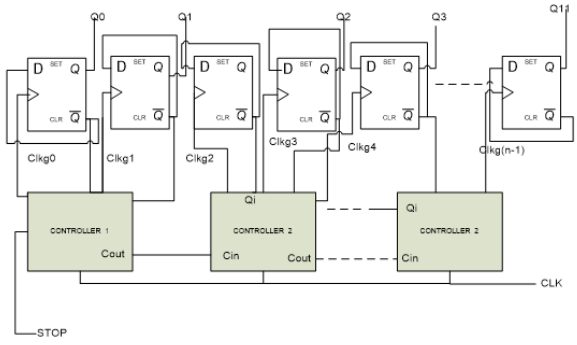

Fig 5. Proposed clock gated SAR Register block diagram

3 Result and Discussion

The performance of clock gated SAR are compared with double gated and NC^{2}MOS gated SAR. The simulated result of the SAR Logic is deployed at 180 nm CMOS technology at 1.8V supply at 0.5 KS/s. As compared to conventional SAR, the proposed clock gated SAR saves 58% and by comparing to the double gated SAR, it saves 35.7% of the power as shown in [Figure 6]. As compared to conventional SAR, the proposed clock gated SAR saves 81.4% and by comparing it to the NC^{2}MOS gated SAR, it saves 38.4% of the power as shown in [Figure 7]. [Figure 8] shows the power consumption of proposed clock gated SAR and conventional without clock gating. The power consumption without clock gating is 54μW and with clock, gating is 22.68μW. As in the proposed SAR register, no transistor count is raised, but total power consumption is decreased by 58 percent. [Table 1] shows the comparison of conventional SAR, other reported SAR, and proposed clock gated SAR based on the various parameters like the technology used, supply voltage, resolution, number of transistors required, and consumption of power. From Table 1, the consumption of the power in SAR Register without clock gating technique is more than the SAR Register with clock gating technique. But the number of transistors is increased in the clock gated SAR.

Table 1. Comparison of Conventional SAR, other reported SAR, and proposed clock gated SAR

Parameters	(17)	Conventional SAR with clock gated	Proposed clock gated SAR
Technology (nm)	180	180	180
Resolution (bits)	8	12	12
Supply Voltage (V)	1.8	1.8	1.8
Sampling Rate	35MS/s	0.5KS/s	0.5KS/s
Power consumption	65μW	54μW	22.68μw

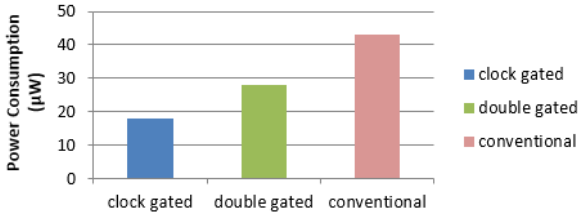

Fig 6. Analysis of power consumption with double gated SAR

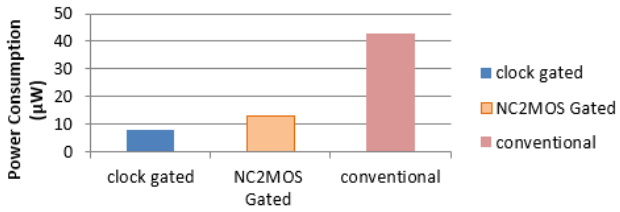

Fig 7. Analysis of power consumption with NC2MOS gated SAR

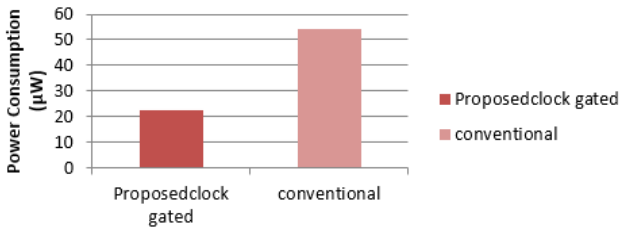

Fig 8. Power consumption of proposed clock gated and conventional SAR

4 Conclusion

A 12-bit SAR has been implemented to minimize the repeated cycles of the clock signal for Bio-Medical applications. The proposed NC^{2}MOS gated SAR saves more power percentage as compared to double-gated SAR. The proposed system does not demand any constraint on the clock duty cycle. In 180nm CMOS technology, the SAR with a clock gated system with double gated SAR and NC^{2}MOS gated SAR have been introduced using a 1.8V power supply. In the future, this technique will be used to design a biopotential system with improved battery life.

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