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RESEARCH ARTICLE

Analysis of 7T SRAM Cell Based on MTCMOS, SVL and I-SVL Technique

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Abstract

Objective: To design and propose an optimized Volatile 7T based SRAM cell in terms of leakage currents and dynamic power. **Methods:** The methodology involved is Multi threshold Voltage CMOS (MTCMOS), Self Controllable Voltage Level (SVL) and Improved Self Controllable Voltage Level (I-SVL). **Findings:** The proposed work demonstrates that 7T based SRAM cell using I-SVL method is efficient in terms of leakage currents and dynamic power. Also, Comparative Leakage current and dynamic power analyses are done between MTCMOS, SVL, and I-SVL methods The Proposed work based on I-SVL is significant than the MTCMOS and SVL Technique. All the circuits are developed using the Cadence virtuoso tool and spectre simulator is used to carry out the simulation. **Novelty:** The paper proposes Low power Volatile Memory cell based on 7T with improvements in leakage and dynamic power values in comparison with the earlier literatures. The proposed I-SVL based cell is 89% and 85% efficient in terms of dynamic power in comparison with the earlier references.

Keywords: Improved – Self Controllable Voltage Level (I-SVL); Improved Lower SVL (I-LSVL); Improved Upper SVL (I-USVL); Multi threshold Voltage CMOS(MTCMOS); Self Controllable Voltage Level (SVL); SRAM

1 Introduction

Memories are of two kinds such as Volatile and Non Volatile. Generally Volatile memories are faster and suitable for applications in higher speed Memories of PC as cache. Random Access Memory (RAM) chips are widely used as a memory for high speed operations. Hence, energy efficient hardware architecture is necessary for smooth operation. The present technology is scaling day by day, due to which the leakage power is enormous. Leakage power in terms of gate and sub-threshold is the major source for power consumption. The power of SRAM array architecture within the cache memory depends on the individual cell, hence the challenging part is to reduce leakage power in terms of SRAM cells. Thereby results in the power savings of the cache memory. Normally the total power consumption of an SRAM Cell is based on Idle and Working condition. When it is in idle state there will be some power loss termed as Static power in terms of gate and sub threshold leakage. During working condition the power dissipation is designated through dynamic power. The total power is the sum of static and dynamic power.

The standard 6T based SRAM cell is largely adopted in cache because of simplicity nature.6T based SRAM cell lags instability and hence 7T configured SRAM cell.7T based SRAM cell requires one additional transistor at the lower portion of 6T SRAM cell to improve stability during operation. In the present work 7T based SRAM cells using MTCMOS, SVL, and I-SVL have been designed and analyzed. The performance analysis is carried in terms of gate, sub threshold leakage, and dynamic power.

6T based SRAM cell and array designing is discussed using Low power reducing techniques such as gated VDD and MTCMOS [1]. Design of 6T, 8T, and 9T based SRAM is carried using MTCMOS technique in [2] . MTCMOS Schmitt trigger based Nonvolatile SRAM cell design is done in [3]. Triple threshold voltage CMOS technology design is carried on 6T, 7T & 8T based cells in [4].7T based SRAM cell designing based on SVL and I-SVL is done in [5] [6]. A high speed and Low leakage 6T SRAM cell is proposed by adopting MTCMOS method [7,8].A comparative survey on SRAM has been carried using distinct Low Power techniques [9]. A New 7T based SRAM Memory cell has been proposed with improved performance during read operation [10]. Memristor based Non-volatile 7T SRAM cell has been designed with improved stability [11,12]. The author presented the performance investigation of CNTFET SRAM cells by using low power techniques [13] with the lacuna in cell area and leakage currents. Volatile and Non Volatile 7T based SRAM cells were proposed with performance analysis in [14]. The author proposes optimized 10T based SRAM cell using PNP inverters with the increased area and leakage penalty [15].9T based SRAM cell using MT-SVL method is implemented in work [16] with the penalty in area and dynamic power.7T based SRAM cell using Power Gated Vdd method is implemented in work [17] with penalty in dynamic power.

The above presented literatures lags in leakage and dynamic power. The same issue is addressed by proposing an optimized Volatile 7T based SRAM Cell in terms of leakage and Dynamic power.

2 Methodology

2.1 MTCMOS

MTCMOS technique is one of the important techniques to decrease leakage power. In this method, the leakage power is minimized by disconnecting the power supply using switches (SW's) having very high threshold voltage. This technique generally consists of transistors with more no of variable threshold voltages which results in optimized delay and power without introducing penalties. All transistors in the 7T SRAM Cell are modeled at Lower Vt except sleeping transistors are modeled at Higher Vt to results in reduced leakage power. The implementation through the MTCMOS technique involves in leakage power reduction via using transistors which are in sleep mode. These associated transistors are enabled in ON mode and disabled in OFF (Sleepy) mode through clock signal. A Transistor in Sleepy mode reduces static leakage current by larger amount during off condition of SRAM Cell [1]. The Proposed 7T based SRAM cell designed using Multi Threshold CMOS Technique is indicated in Figure 1.

During the OFF condition of sleep transistors, automatically VDD & ground get disconnected from the SRAM cell and data bits 0 & 1 are available on either side of the SRAM cell to form virtual power rails.

2.2 Self Controllable Voltage level (SVL and Improved Self Controllable Voltage Level(I-SVL

The handy portable electronic devices that are operated on batteries need an efficient design for low leakage power. To achieve power reduction many significant methods are used, those are Multi Threshold Voltage CMOS (MTCMOS), Self Controllable Voltage Level (SVL), and Improved Self Controllable Voltage Level (I-SVL).The above discussed MTCMOS is very sensitive as High Threshold MOSFET switches are needed and it cannot retain data for a longer time. Hence SVL and I-SVL methods are proposed for lower leakage power in standby mode [3]. The Proposed 7T SRAM Cell based on Self Controllable Voltage technique (SVL) is depicted in Figure 2.

An SVL technique is significantly employed as the load to provide full Vdd voltage during the ON mode and reduced Vdd voltage during OFF condition for decreasing gate leakage current. Therefore during the stand-by mode, a mechanism is used to provide slightly lesser supply voltage and higher supply voltage to the load circuit using enabled switch, so that Vds of inactive condition MOS transistors decreases Vsub. This enhances Vth and consequently sub- threshold current decreases [4]. The design of the proposed Improved Self Controllable Voltage (I-SVL) technique based 7T SRAM cell is indicated in Figure 3.

In the period of SRAM operation during active mode, I-SVL enabled switch is used in providing higher supply and a lower ground Vss voltage to the SRAM cell, so it can operate quickly. Over the period of standby mode of operation, I-SVL provides slightly lesser Vdd voltage and larger ground Vss voltage. Thereby I-SVL switches are involved in decreasing gate leakage currents at a stand-by mode of Operation [18].

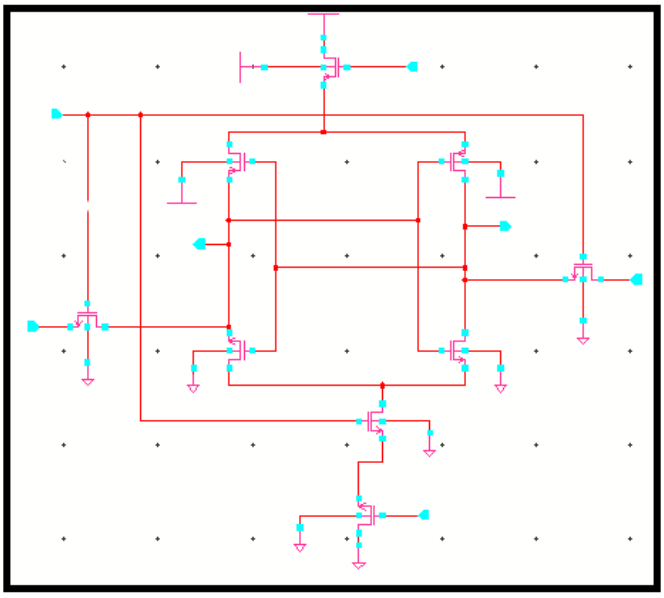

Fig 1. 7T SRAM Cell Schematic based on MTCMOS Technique

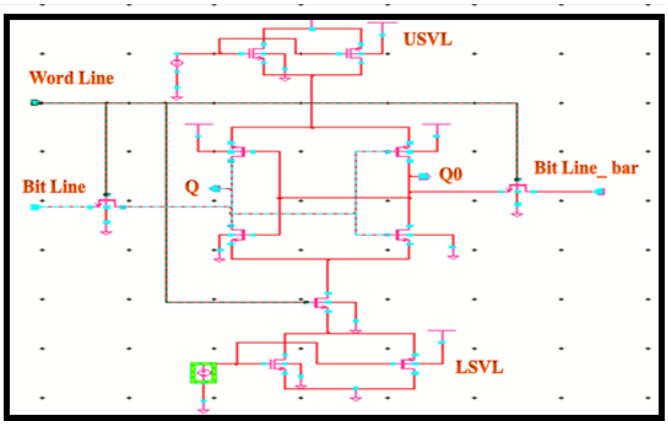

Fig 2. 7T SRAM Cell Schematic based on SVL Technique

3 Simulation Results and Discussions

The design and simulation of 7T SRAM cells using MTCMOS, SVL and ISVL technique is proposed by employing Cadence Virtuoso Spectre Tool using standard CMOS technology. As CMOS technology marches down to scaling the usage of process variation is a bit challenging.

Corner analysis helps in measuring the circuit performance while simulating the circuit with a set of parameter values which represent the extreme variation in a manufacturing process. Also, it accounts for deviations in the semiconductor fabrication process. Normally variation in process parameters will be in terms of gate oxide thickness, impurity concentration, and diffusion depths. CMOS technology normally supports the following process corners. a) NN: normal NMOS, normal PMOS b) FF: fast NMOS, fast PMOS c) SS: slow NMOS, slow PMOS d) FS: fast NMOS, slow PMOS.

ndicates the environmental corners for a 1.8V commercial process and illustrates that circuits are fastest at high voltage and low temperature. Circuits are intended to fail most likely at the corners of design space, hence nonstandard circuits to be simulated at all corners to ensure for stable operation.

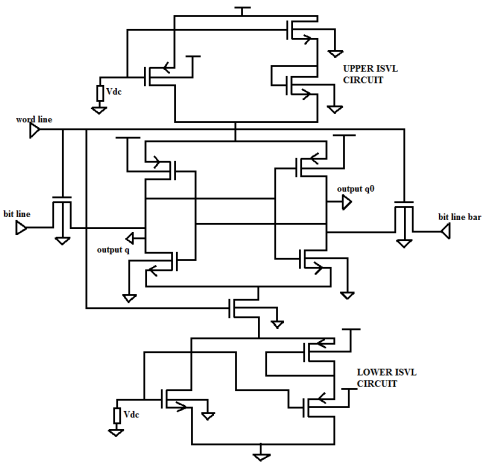

Fig 3. 7T SRAM Cell based on I-SVL Technique

Table 1. Environmental Corners

NMOS	PMOS	VDD	Temperature
Normal	Normal	1.62	125^{o}C
Slow	Slow	1.62	125^{o}C
Fast	Fast	1.98	0^{o}C
Slow	Fast	1.98	0^{o}C
Fast	Slow	1.98	0^{o}C

3.1 Results of Leakage Analysis

The proposed work of I-SVL based 7T SRAM cell is superior in terms of Low gate and sub-threshold leakage in comparison with the other power reduction techniques like, MTCMOS and SVL methods. The same is depicted in the analysis of leakage results and dynamic power values with the comparison of earlier literatures.

The leakage analysis is carried for the proposed 7T based SRAM cells using MTCMOS, SVL, and I-SVL techniques. Generally, Leakage analysis is carried when the device is in 'OFF 'condition, without applying any input. The analysis is carried for gate, sub threshold, and total leakage. The evaluation of leakage analysis is carried for different process variation employing MTCMOS, SVL and I-SVL techniques. The adopted process variations are FF, FS, SS and NN at 45nm technology with supply voltage of a 1.8V. Total leakage current of SRAM cell is given by $I_{Leak} = I_{gate} + I_{sub}$ (1)

Leakage current analysis outputs evaluated using MTCMOS, SVL and I-SVL are tabulated (Tables 2, 3 and 4)

Tables 2, 3 and 4 are the values of gate, sub threshold, and total leakage in nA for different process variations. The values indicated in Tables 2, 3 and 4 clearly demonstrate that the I-SVL method is significant in comparison with the MTCMOS and SVL techniques. For different process variations like FF, SS, NN, and FS the obtained leakage is very less in I-SVL in comparison with SVL and MTCMOS technique. Among the different process variations, SS process results in the least gate, sub threshold, and total leakage. The comparison chart of different leakage currents for MTCMOS, SVL and I-SVL (SS process variation) is plotted and indicated in Figure 5.

Table 2. Leakage Currents Obtained for Different Process Variations Using MTCMOS Technique

Process variation	Gate leakage	Sub Threshold leakage	Total Leakage
FF	-24nA	77nA	53nA
FS	-31nA	98nA	67nA
NN	-6nA	88nA	82nA
SS	-14nA	69nA	55nA

Table 3. Leakage Currents Obtained for Different Process Variations Using SVL Technique

Process variation	Gate leakage	Sub Threshold leakage	Total Leakage
FF	-13nA	55nA	42nA
FS	-14nA	48nA	34nA
NN	-12nA	44nA	32nA
SS	-9nA	30nA	21nA

Table 4. Leakage Currents Obtained for Different Process Variations Using I-SVL Technique

Process variation	Gate leakage	Sub Threshold leakage	Total Leakage
FF	-8nA	23nA	15nA
FS	-8nA	24nA	16nA
NN	-3nA	21nA	18nA
SS	-0.8nA	6nA	5.2nA

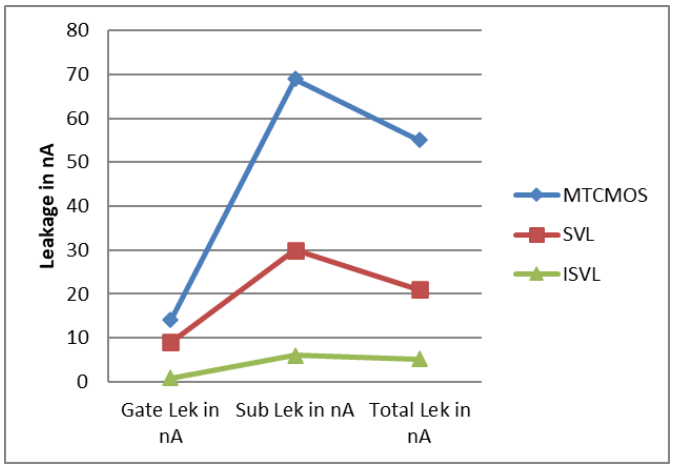

Fig 4. Leakage currents comparison of MTCMOS, SVL and I-SVL Techniques

3.2 Results of Dynamic Power Analysis

The dynamic power analysis is carried when the device is in 'ON 'condition. The analysis is carried by applying different inputs like Word, BL, and BLB to check for the functionality of the SRAM cell in terms of Read and Write operation. The write and read phases are enabled based on the input line Word. During the write operation word input is '1' and if BL input is '1' then writing'1' operation takes place. Else if BL input is '0' then writing '0' operation takes place. For Read operation Word input is '0' and BL should be '1'(Precharge) to perform the read operation based on the previously stored values of '1' and '0'. Read and Write operations for 7T SRAM cells based on MTCMOS, SVL and I-SVL are depicted in respectively.

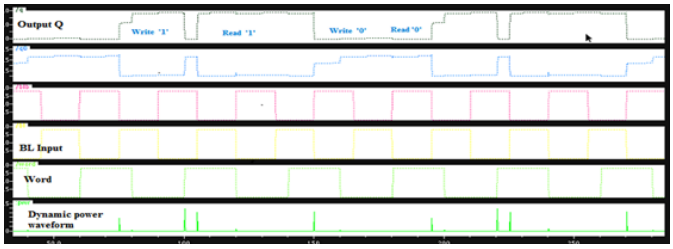

Fig 5. Read and write operations in proposed 7T SRAM cell based on MTCMOS technique.

The Tables 5, 6 and 7 are the values of dynamic power evaluated for write and read operations of the Proposed 7T based SRAM cell using MTCMOS, SVL and I-SVL techniques. Also, the tabulated results demonstrate that the I-SVL method has

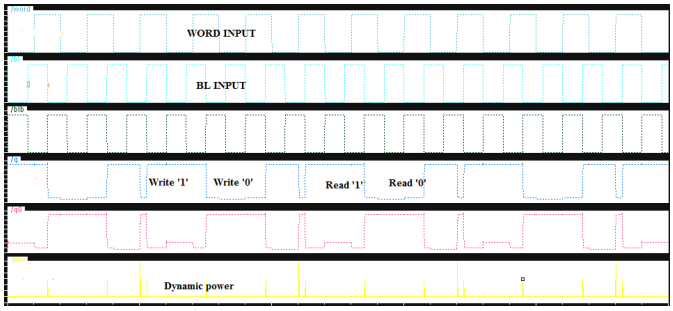

Fig 6. Read and write operations in proposed 7T SRAM cell based on SVL technique

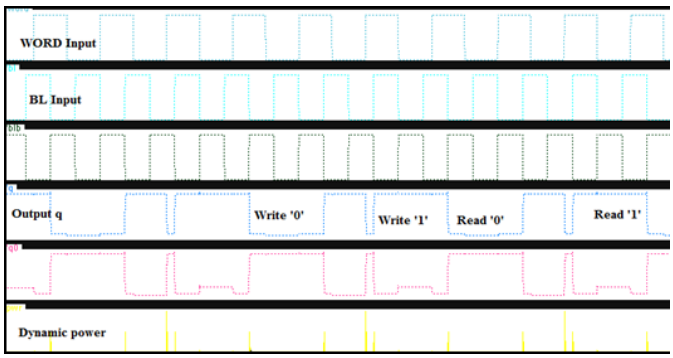

Fig 7. Read and write operations in proposed 7T SRAM cell based on I-SVL technique.

Table 5. Dynamic Power Values Obtained for Different Process Variations Using MTCMOS Technique

Operation	SS	NN	FS
Write 1	2μw	1.9 μw	1.8 μw
Write 0	2μw	1.9 μw	1.8 μw
Read 1	2μw	1.9 μw	1.8 μw
Read 0	2μw	1.9 μw	1.8 μw

Table 6. Dynamic Power Values Obtained for Different Process Variations Using SVL Technique

Operation	SS	NN	FS
Write 1	970nw	969nw	871nw
Write 0	970nw	969nw	871nw
Read 1	970nw	969nw	871nw
Read 0	970nw	969nw	871nw

Table 7. Dynamic Power Values Obtained for Different Process Variations Using I-SVL Technique

Operation	SS	NN	FS
Write 1	613nw	583nw	617nw
Write 0	613nw	583nw	617nw
Read 1	613nw	583nw	617nw
Read 0	613nw	583nw	617nw

least Dynamic power value in comparison with SVL and MTCMOS method. Among the different process variation like SS, NN and FS, SS process is significant by consuming least dynamic power value. The Comparison chart of dynamic power in terms of different process variation using MTCMOS, SVL and I-SVL is depicted in Figure 9.

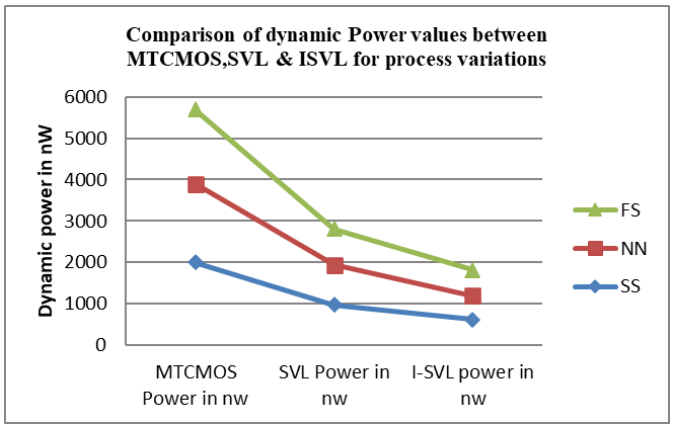

Fig 8. Comparison of Dynamic power for different process variations using proposed 7T SRAM cellbased on MTCMOS, SVL and I-SVL

Table 8. Dynamic Power Values of Proposed Cells and Work in References [2], [16] and [17]

Proposed Cells and Earlier work	Dynamic power
7T based on MTCMOS	1.8μW
7T based on SVL	871nW
7T based on I-SVL	617nW
Ref[16] SRAM cell based on MTCMOS	5.876μW
Ref[15] SRAM cell based on MTSVL(9T)	4μW
Ref[17]0 SRAM cell based on Power Gated VDD Technology	63μW

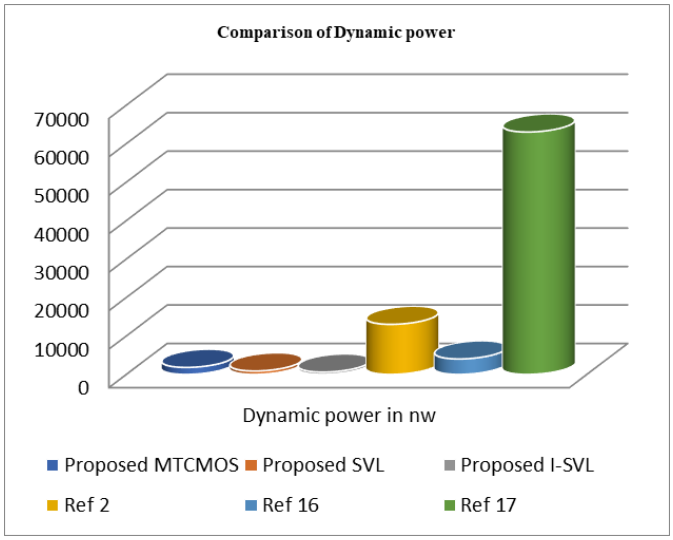

Fig 9. Dynamic power values representation of proposed 7T based SRAM cells and Earlier Literatures

From the comparative analysis presented in the above chart it is clear that I-SVL method is significant in terms of low power in comparison with the work carried in [2] [16] and [17]. The proposed I-SVL method requires 89% and 85% lesser power in

comparison with the work done in [2] and [16]. Also proposed SVL Technique requires 85% and 78% lesser amount of power in comparison with the work proposed in [2] and [16]. The chart of dynamic power values between the proposed 7T based SRAM cells and work in ref [2] [16] and [17] are indicated in Figure 9. Also it is clear that the proposed work of I-SVL is very efficient in dynamic power with the ref [17].

4 Conclusion

The current trend designing of memory cell prefers low power reduction techniques like MTCMOS, SVL, and I-SVL. In the present work, Leakage and dynamic power analysis is carried for different process variations using the cadence virtuoso spectre tool. The proposed work clearly demonstrates that the I-SVL method is significant in terms of low power in comparison with MTCMOS and SVL Technique. The analysis indicates that Proposed I-SVL requires 70% and 56% lesser dynamic power in comparison with the proposed MTCMOS and SVL Methods. Also, it reflects that the Proposed I-SVL method is 89% and 85% efficient in dynamic power in comparison with the work carried in ref [2] and [16] using MTCMOS based SRAM Cell. Also, the comparative total leakage analysis clearly demonstrates that the proposed I-SVL based 7T cell is 90% and 74% efficient in terms of gate and sub threshold leakage with the proposed 7T based cell using the MTCMOS and SVL method. Hence I-SVL method is significant in terms of low power designing of SRAM Cells.

5 Acknowledgement

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References

1) Shivkumar SA, Geetha S. Design and Analysis of Low power MTCMOS using SRAM Cell. *International Journal of Management*. 2019;IX(III). Available from: https://doi.org/16.10089.IJMTE.2019.V9I3.19.27426.
2) Das SM. A Novel Low Power Energy Efficient SRAM Cell With Reduced Power Consumption using MTCMOS Techniquen. *IOSR Journal of VLSI Signal Process*. 2015;5(1):42–49. Available from: https://doi.org/10.9790/4200-05114249.
3) Nikitha L, Bhargavi NS, Kariyappa BS. Design and Development of Non-volatile Multi-threshold Schmitt Trigger SRAM Cell. *International conference on Emerging Research in Electronics*. 2019;p. 978–981. Available from: https://doi.org/10.1007/978-981-13-5802-9.
4) Kumar CSH, Kariyappa BS. Analysis of low power 7T SRAM cell employing improved SVL (ISVL) technique. *2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT)*. 2017;p. 478–482. Available from: https://doi.org/10.1109/ICEECCOT.2017.8284551.
5) Sreekala K, Kumar SK. Leakage Estimation of SRAM cell based on Node Voltage and Current Characterization. *International Journal of Pure and Applied Mathematics*. 2018;p. 13143395–13143395. Available from: https://doi.org/https://acadpubl.eu/jsi/2018-118-7-9/articles/7/13.
6) Kumar H, S C, B K. 7T Based SRAM Topologies with Low Power and Higher SNM. *International Journal of Innovative Technology and Exploring Engineering*. 2019;8(11):2779–2783. Available from: https://doi.org/10.1109/RTEICT42901.2018.9012414.
7) Tripathi T, Chauhan DS, Singh SK. A Novel Approach to Design SRAM Cells for Low Leakage and Improved Stability. *Journal of Low Power Electronics and Applications*. 2018;8(4):41–41. Available from: https://doi.org/10.3390/jlpea8040041.
8) Agrawal R, Tomar VK. Analysis of Cache (SRAM) Memory for Core iTM 7 Processor, 2018. *9th Int Conf Comput Commun Netw Technol*. 2018;p. 1–8. Available from: https://doi.org/10.1109/ICCCNT.2018.8494063.
9) Leela M, Rooban S, Joshitha C. Comparative analysis on low power SRAMs. *Materials Today: Proceedings*. 2020. Available from: https://doi.org/10.1016/j.matpr.2020.11.140.
10) Kazi F, Sharif R, Islam. A New Model of High Speed 7T SRAM Cell, International conference on computer, Communication and Electronic Engineering (IC4ME2),IEEE 2018. Available from: https://doi.org/10.1109/IC4ME2.2018.8465611.
11) Singh J, Raj B. Design and Investigation of 7T2M-NVSRAM With Enhanced Stability and Temperature Impact on Store/Restore Energy. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2019;27(6):1322–1328. Available from: https://doi.org10.1109/TVLSI.2019.290103.
12) Louis VJ, Pandey AJG. A Novel Design of SRAM Using Memristors at 45 nm Technology, VDAT 2019, CCIS 1066. 2019. Available from: https://doi.org/10.1007/978-981-32-9767-8_48.
13) Kumar H, Srivastava S, Khosla PK, Singh B. High Stable and Energy Efficient Emerging Nanoscale CNTFET SRAM Cells using Circuit Level Low Power Techniques. *Silicon*. 2022. Available from: https://doi.org/10.1007/s12633-021-01581-8.
14) Kumar CSH, Kariyappa BS. Node Voltage and KCL Model-Based Low Leakage Volatile and Non-Volatile 7T SRAM Cells. *IETE Journal of Research*. 2022;p. 1–17. doi:10.1080/03772063.2022.2027279.
15) Chauhan RA. Low Power PPN inverter based 10T SRAM Cell. *Indian Journal of Science and Technology*. 2021;14(20):1699–1710. Available from: https://doi.org/10.17485/IJST/v14i20.400.
16) Jyothi K. SRAM cell with MT-SVL Technique for Leakage Power reduction. *IT in Industry Journal*. 2021;9(2). Available from: https://doi.org/838-1-10-20210413.
17) Valluri A, Jayabalan M. Reduction of Power in SRAM cell with Gated Vdd Technology. *IJRTE*. 2019;7. Available from: https://doi.org/E10800275S419/19@BEIESP.
18) Kumar CS, Kariyappa BS. Design and Power Analysis of 16×16 SRAM Array Employing 7T I-LSVL. In: 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT). 2018;p. 319–322. Available from: https://doi.org/10.1109/RTEICT42901.2018.9012414.