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REVEIW ARTICLE

Comprehensive Review of Optimal Utilization of Clock and Power Resources in Multi Bit Flip Flop Techniques

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Abstract

Objective: To analyze High-speed digital Integrated Circuit (IC) designing techniques and to identify the power dissipation rate in a different configuration of network switches. **Methods:** the complexity of a large-scale switching network is reduced using 2-bit Multi Bits Flip Flops (MBFF). The throughput and reliability are increased using a multibit flip-flop and have to be operated in parallel. The clock cycle required for 64-bit logical operation is analyzed using Xilinx software. The resources utilized during the execution process in various methods have been identified and analyzed **Findings:** Based on the survey, the proposed system will be built to identify characteristics of multi-bit flip flop based on switching speed (ps) concerning temperature (c), load capacity (fF), supply voltage (v), power consumption (mW) with respect to operating voltage (v) and many gates with respect to nanometer (nm) **Novelty:** Chip size and total power consumption rate by optimal chip reconfigurable network has been reduced to micrometer (mm) to nanometer (nm) and 0.3mW to 0.04mW respectively. Performance of parallel different applications operations in effective utilization of MBFF has been increased to 64 bits/s to 128 bits/s. The switching speed is increased with respect to clock frequency without any hazards and jitters using reconfigurable MBFF methods

Keywords: System on Chip; Multibit flipflop; multibit register; breadthfirst search; Register transfer level; Verylargescale integration

1 Introduction

The power consumption in an integrated circuit is one of the main parameters of Very Large-Scale Integration (VLSI) design. Today reduction power consumption using advanced technology is the great interest in IC design and it's a need of many portable devices. With this concern minimization of switching rate in a clock network in very essential to reduce the power consumption of a System on Chip (SOC), because it

contributes on a chip of 50% of dynamic power[1]. In SOC design the dynamic power consumption is dominated and 75% of power is contributed to the total power of the design[2]. Recent researches have introduced many approaches to reduce to switching rate in the clock network such as register placement optimization, buffer sizing [[3–5]], register banks[6], multi-bit flip-flops (MBFFs), or applying multi-bit registers[7–15]. The concept of making a flip-flop of 2 bit from merging -bit flip-flops of two 1 bit is shown in Figure. 1. In each flip-flop contain pair of inverters, which produces the clock signal in the opposite phase. As they advance in the process technology beyond 65nm it helps to minimize inverter/buffer in the design[16]. The number of inverters in the design can be reduced with the help of one multi-bit flip-flop (MBFF). This process reduces the area and power consumption of the design to great extent.

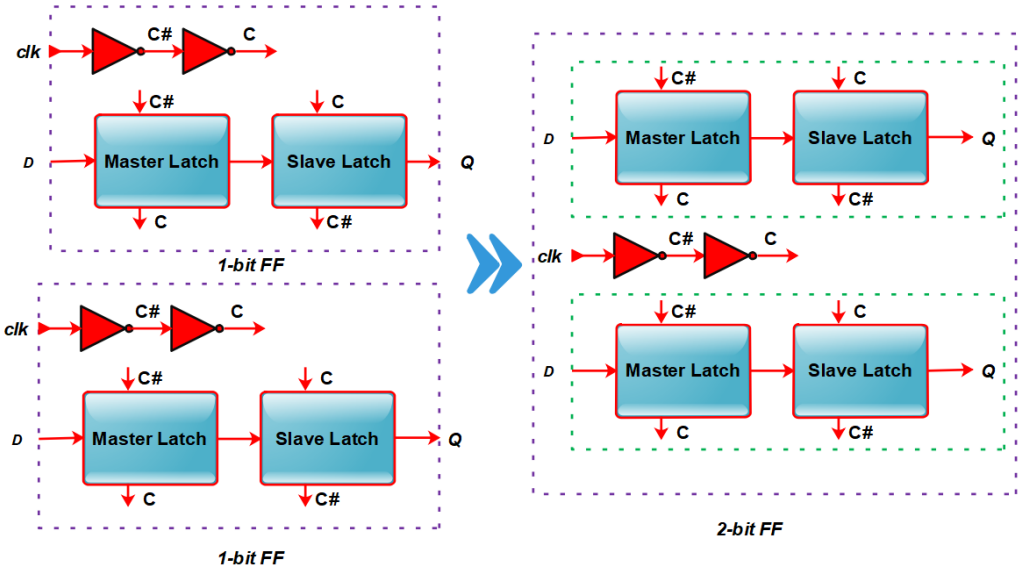

Fig 1. Reconfigurable process of 1-bit flip-flop into 2-bit flip-flop.

The following advantages offer by MBFFs along with a reduction in power and area.

- The smaller capacitive load and fewer clock sink on the clock network as shown in Figure. 2, makes the smaller power and delay of the clock network.
- The common clock in the design reduced the depth of a clock tree and controllable clock skew.
- Utilization of resources with improved routing for any design for testability (DFT).

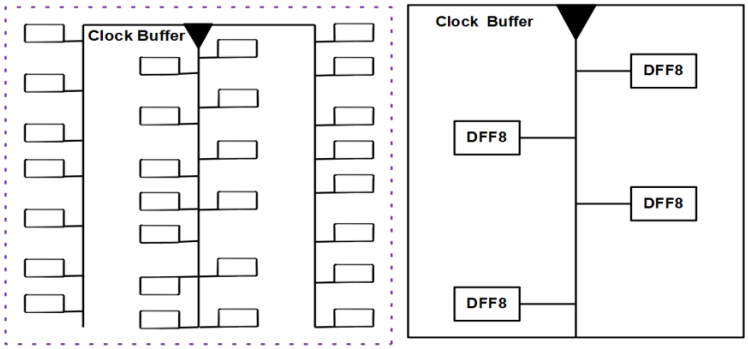

Fig 2. 2: a)Clock network 28 1-bit flip flops b) Clock network of one 4-bit and three 8-bit flip-flops

In [17] the idea of using MBFFs was first introduced. Further Hou et al. [18] have presented pipelined design by applying register banks. The common integrated clock gating block is associated with all flip-flops is placed between two-dimensional arrays. The example of a cell with integrated clock gating and 32 flip-flop cells register bank is shown in Figure. 3. The cell structure presented in [18], contains 2, 4, and 8 single-bit flip-flops, but the structure of the register bank presented in [19] have flip-flops in large number ranging from 16 to 128.

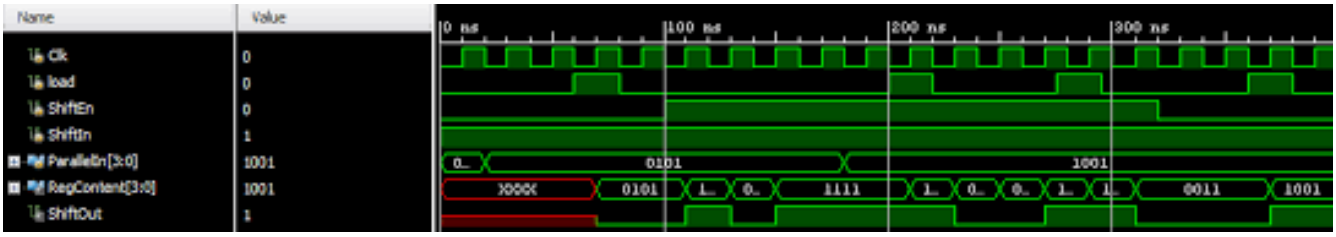

Fig 3. 3. Structure of register bank containsone integrated clock gating and 32 flip-flop cells

To make use of MBFFs by replacing single-bit flip-flops to save the power consumption is further investigated to the optimization methods for design. The existing MBFFs flow and design optimization methods are summarized in Table 1.

Table 1. List of MBFFs flow, design optimization methods, and related work

Related Works	Optimization Method/Flow
[7], [10]	MBFFs Logic optimization
[9]	MBFFs Pre-placement optimization
[8]	Register bank placement optimization
[11], [12], [13]	MBFFs post-placement optimization

The rest of the paper's content is organized as flows: MBFFs logic optimization is presented in section II, MBFFs optimization methods or register banks, and various physical synthesis flows is presented in section III. Directions for future research are presented in section IV, and finally, the conclusion is presented in section V.

2 MBFFs Logic Optimization

The feasibility of using MBFFs by inputting an RTL design during synthesis is presented by K. S. Manu et al [20], and M. P. Lin,. [21] Design constraints, MBFF cells library, and the logic synthesis tool available is illustrated in Figure. 4.

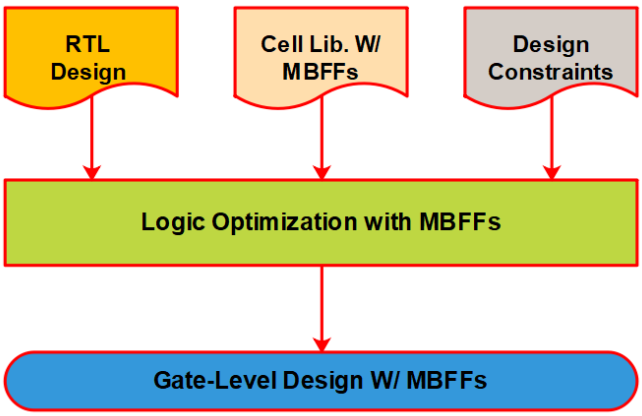

Fig 4. MBFF cells Logic optimization using Synopsys

L. Cherif, M [22], was introduced an advanced design method for creating the cell library with multi-bit registers models, which can be inferred by Design Compiler. In this approach, RTL design can be directly mapped to gate level based on the multi-

bit register cells. Further options and inference commands provided by Design Compiler are reported by S. Gautam et al.[23]. In their work 2-bit, flip-flop cells have been designed using their cell library to implement it on ASIC designs. The experimental results show that the total power consumption of the clock network is 22-40% and a reduction in power consumption is achieved around 10-11 %.

3 MBFFs Physical Optimization

Most of the recent work shows that[24], the available logic synthesis tools are supported to perform the MBFFs logic optimization. During physical synthesis, authors have tried and succeeded in developing the physical design flow for MBFFs. The developed works are divided into three different categories: 1) MBFFs pre-placement optimization[25], 2) In-placement register banks optimization[26], 3) MBFFs post-placement optimization[27].

3.1 MBFFs pre-placement optimization

The physical design flow is shown in Figure. 5 presented by Wu, H et al,[28]. In this design breadth-first search (BFS) algorithm has been used grouped at the gate level as single bit flip flops design starting from the clock root. Based on the design requirements the number of single-bit flip-flips is grouped and corresponding MBFF is generated. This process makes it easy to control clock skew during placement optimization. This procedure of flow design reduces the number of flip-flop cells and reduces the resource required.

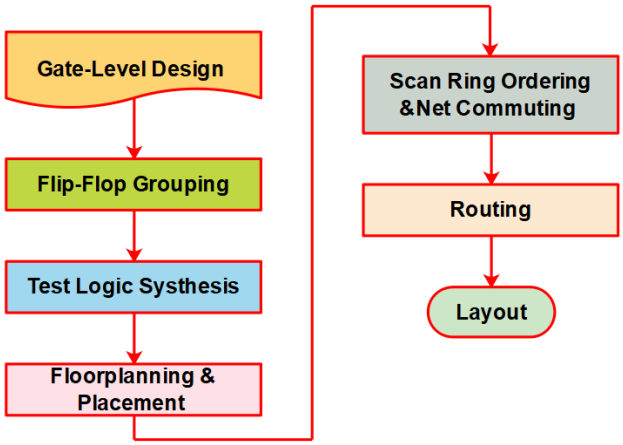

Fig 5. The process of MBFFs pre-placement optimization

3.2 In-placement register banks optimization

Figure. 6 shows the physical design flow presented by Chundi Pavan Kumar,[29] for register bank generation with proper timing and profitability. The initial placement is started by generating register banks for single-bit flip-flops gate-level design. During the generation of register bank, the number of the register which is in the same pipeline is merged into a single register bank with the help of heuristic criteria. For example, at the register-transfer level (RTL) if the register belongs to the same vector group and has the same integrated clock then they are grouped into a common register bank. The dimension and location of the register bank are calculated by reducing the register cells' total displacement.

MBFFs post-placement optimization

Instead of following the heuristic criteria to generate register banks in large size and disassembling the banks for incremental placement in recent works[30], it's better to adopt different problem formulation in the post-placement stage to generate MBFFs with the satisfaction of placement and timing constraints. Figure. 7 (a) shows the problem formulation-based post-placement MBFF generation physical synthesis flow. This process has two major steps: 1) Placement of MBFF and 2) Clustering of flip-flops as shown in Figure.7 (b). Each step design objectives are further compared in Table II with related works.

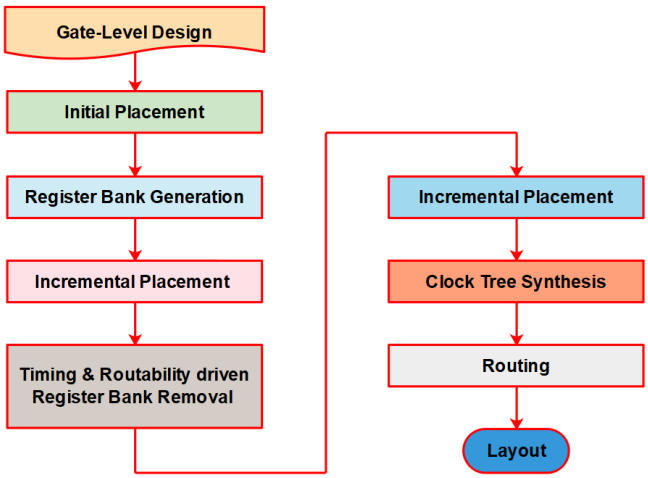

Fig 6. The process of in-placement register banks optimization.

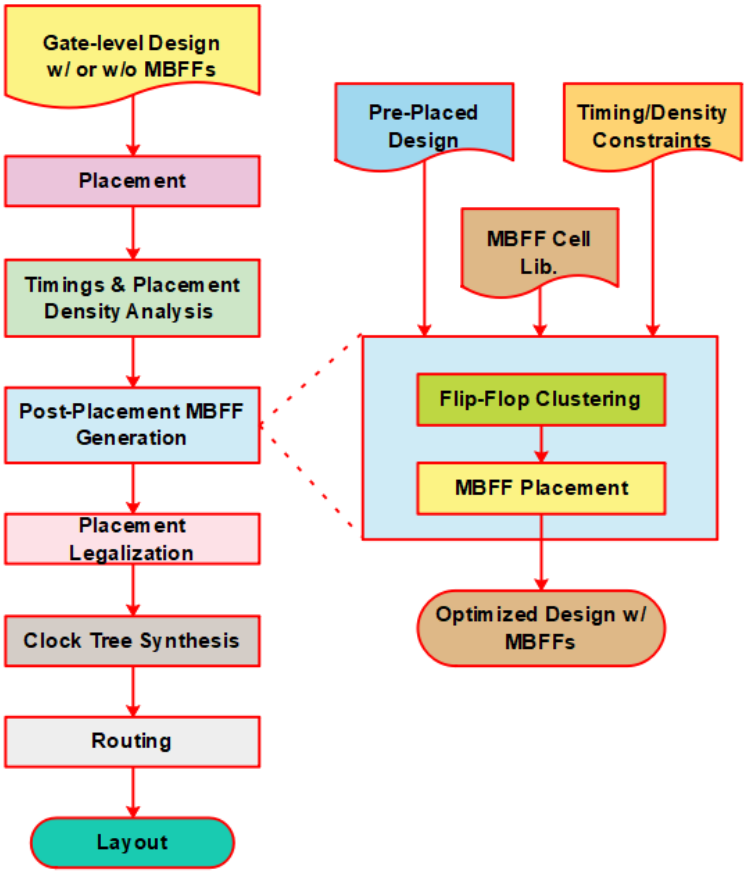

Fig 7. (a) Post-placement MBFF generation- physical synthesis flow (b) Flip-flop clustering generation flow

Table 2. Comparison of Flip-Flop Merging Design Objectives and Placements of MBFF.

Method	MBFF Placement objective	Flip-Flop Clustering objective
(24)	N/A	The total minimum power of the flip-flop
(25)	Maximum rout ability	The total minimum power of the flip-flop
[27]	Minimum total wire length	The total minimum power of the flip-flop and wire length
(27)	Minimum total net switching power	Net switching power and total minimum number of clock sinks
(28)	Minimum total wire length	Total minimum flip-flop power

3.4 Placement of MBFF

The design procedure of previous works has been referred to place the newly generated MBFFs with different objectives are shown in Table II. MBFF placement algorithm presented by Chen and Dake Liu (31), which integrates signal rerouting and capacity-constrained to maximize the profitability. In another work Mallikarjunaswamy, S (32) and I. H. Jiang, C et al. (33) have proposed a method to place MBFF in the median coordinates to reduce the wire length. The weighted total wire length is minimized using weighted median intervals was presented by Mahendra HN, (34) and this method reduces the total switching power.

3.4.1 Clustering of Flip-Flop

Many researchers have focused on reducing the power consumption of the flip-flop during flip-flop clustering (34). The different design objective was given by Thazeen, S et al (35) to reduce the number of clocks sinks ad switching power. The first one is the number of flip-flops in the design is equal to the total clock sinks in the design and the second is the switching power of the design is derived as per the switching rates.

Figure. 8. (a)Flip-flop feasible region (b) Intersection graph of the flip-flop.

A group of the flip-flop is merged into a single MBFF to satisfy the timing constraint only if they have the feasible common placement region. Figure. 8 (A) shows the intersection of flip flops with allowable distances to connected pins. Researchers (36) were proposed their algorithms based on an intersection graph to generate the clusters of flip-flops as shown in Figure. 8(b). J. H. Edmondson et al (37) (38) have used iteratively extracting process instead of using intersection graph while grouping flip flops to propose their algorithms.

4 Directions towards Future Research

The MBFFs clock network development and future research directions are presented in this section.

4.1 MBFF Optimization Design Flow Exploration

Although the in the prior art had investigated the optimization of MBFF at different design stages. But optimization using two different design stages is not reported. Therefore, it's necessary to develop the best design flow for MBFF optimization to physical design from electronic system-level (ESL).

4.2 Register Banks and Bit Numbers of MBFFs

In the previous works, many researchers are reported MBFF bit number ranges from 2 to 8 (39) and ranges of registered banks from 16 to 128 (40). But no work reported on the effective use of the bit number of a registered bank or MBFF. Therefore its worth comparing best out of between the bit number and other design constraints

4.3 Register Banks and Legalization of MBFFs

From the design procedure, we understand the size of register banks and MBFF cells is much higher than the single-bit flip-flops size. Also, it occupies multiple rows, but detailed placement algorithms is not used. Therefore, it's required to study and develop effective algorithms for placements of registered banks and MBFFs.

4.4 Performance Analysis of various MBFF Protocols

Figure 9 shows the power consumption analysis of between various MBFF techniques such as PowerPC, Static D-Flip Flop (SDFF), Hybrid Latch flip-flop (HLFF), Cross Charge Control flip-flop (XCFF), Condition Pass Logic Static DFF (CPLSDFF), Dynamic DFF (DDFF), Clocked CMOS (C2MOS), Condition Pass Logic Dynamic DFF (CPLDFF) on its parameters as shown in table .3 and with respect to operating voltage (V) as shown in Table .4 and comparison analysis as shown in figure.10

Table 3. Power comparison of various Flip-flop architectures.

MBFF techniques	Data Power (mW)	Clock Power (mW)	Internet Power (mW)	Total Power (mW)
PowerPC	0.9	0.9	5.3	7.1
SDFF	0.3	0.4	3.8	5.9
HLFF	0.2	0.2	4.8	4.9
XCFF	–	–	3.1	3.8
DDFF	0.3	0.1	3.5	3.9
C2MOS	–	–	0.9	1.8
CPLSDFF	0.3	0.2	0.25	1.3
CPLDDFF	0.9	0.1	0.5	1.2

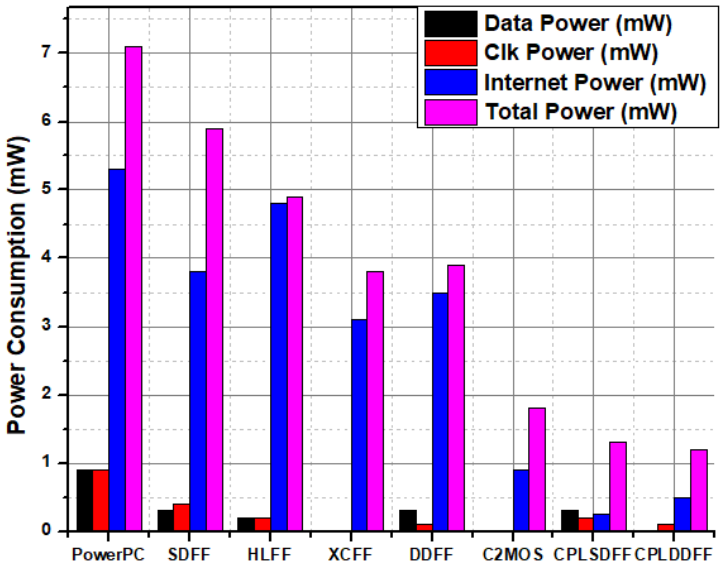

Fig 8. Power comparison of various Flip-flop architectures

Table 4. V Flip Flop power consumption with respect to operating Voltage.

Operating Voltage	PowerPC (mW)	SDFF (mW)	HLFF (mW)	XCFF (mW)	DDFF (mW)
1	5.6	4.5	3.9	3.5	3.2
1.5	5	4.39	3.7	0.5	0.85
2	4.5	4.3	3.6	0.75	0.75
2.5	4	4.2	3.45	0.85	0.6
3	2.9	3.9	2.5	0.865	0.2

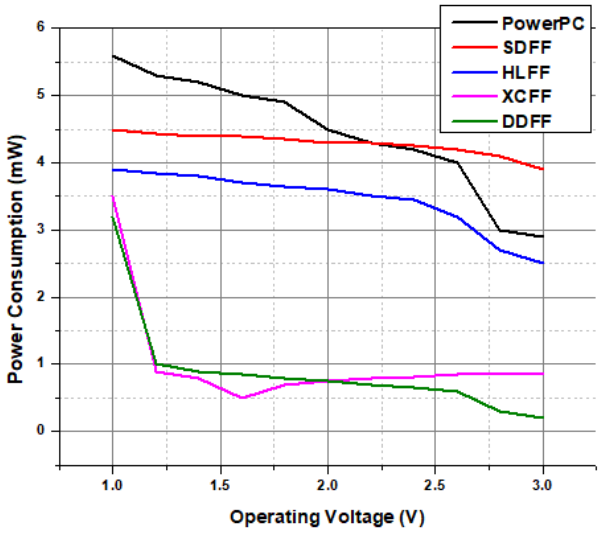

Fig 9. Flip flop power consumption with respect to operating Voltage

5 Conclusions

A large-scale survey has been done on reconfigurable register bank and minimization of clock cycle required in-network and clock power in MBFFs logical circuits. In addition to analysis, the various designing procedure and their constraints have been discussed in this study. Based on the analysis of the study, the proposed work on reconfigurable multi-bit flip-flops design and implementation will be carried out with respect to the reduction of chip size from the micrometer (mm) to nanometer (nm) and total power consumption rate from .3mW to 0.04 mW respectively. Due to the proposed optimal multipath and parallel switching operations, the designed throughput efficiency increases from 64 bits/s to 128 bits/s.

6 Future scopes

5G and 6G Technologies which have highly complex bit encryption and decryption process will require high-speed switching operations. So better accuracy and reliability can be obtained. The multi-bit flip flop techniques will improve its capability to handle these types of data without loss of information and optimal power consumption.

7 Limitations

The multi-bit flip-flop may produce hazards with the increase in data speed and parallel switching operations due to operating in different switching networks like circuit switching, packet switching, message switching, etc in 5G and 6G operating speeds.

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