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RESEARCH ARTICLE

Experimental assessment of Single Phase Grid assisted system using Second Order Generalized Integrator–Frequency Locked Loop

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Abstract

Objectives: To design and develop a simple, robust, and novel SOGI based frequency lock loop approach with DC-offset elimination capability for extracting precise phase angle of the grid voltage. As the additional objective of the work is to utilize the unused capacity of the PV system for providing reactive power support to the grid. **Method:** The second-order generalized integrator (SOGI)-Frequency Look loop (FLL) is implemented to achieve precise phase-angle for the control system, filtering capability for the adaptive frequency tuning as well as an orthogonal signal generation. The DC blocker is designed to eliminate the dc-offset generated during analog to digital conversion without compromising the dynamics of the system. To achieve the second objective, the virtual two-axis current control is simulated and experimented on in a single-phase grid-assisted system. Synchronous-frame current controllers are designed to inject active power to the grid and also ensure the unity power factor by providing reactive power support to the grid. The developed system is simulated using MATLAB /Simulink and implemented on the experimental step-up. **Findings:** The precise phase-angle is extracted from the grid voltage during the abnormal grid conditions like frequency shift, distorted by harmonics, and dc-offset. The DC-offset can be eliminated without adopting high-order FLLs by choosing the appropriate control parameter and DC cancellation block (DBC). **Novelty:** This study presents simple, efficient, novel SOGI based control that provides assurance of power quality as well as injection of active power injection into the grid using the virtual two-axis reference frame power control. The experimental and simulation results confirm that the presented control approach provides fast and accurate phase angle extraction in the grid synchronization with DC-offset cancellation.

Keywords: Grid synchronization; STM32F407VG microcontroller; WAIJUNG Blockset; phase detection; Phase Locked Loop (PLL); virtual two axis reference frame power control

1 Introduction

To fulfill the increasing demand for electricity as well as environmental regulation, solar photovoltaic systems (PV) become a clean and inexhaustible source of energy[1]. Nowadays, the distributed generation units are designed in such a way to utilize the additional capacity of an inverter to provide reactive support for the power factor correction or voltage regulation at the common coupling point[2]. The current control technique and grid synchronization technique of the PV system plays a crucial role to meet the interface standard with the utility[3]. The single-phase/ three-phase grid assisted systems are interfaced with grid either double-stage topology or single-stage topology. In a double-stage topology[4], a power electronics inverter is used for active/reactive power exchange while a DC-DC converter is used to extract maximum power from the PV panel using an MPPT controller[5]. On other-side[6,7], the power electronic converter is capable to extract maximum power as well as active/reactive power exchange in a single-stage topology. Stationary frame PLLs[8] are suitable as well as efficient in single-phase grid assisted PV converter due to the only one voltage signal to synchronize as well as an increase in the speed of synchronization in comparison with other methods. The Phase detector of stationary frame PLLs is having an inherent drawback of producing twice the fundament frequency ripple components (2ω) in the error of phase-detector (ε_{pd}) which further proliferates through the Loop Filter[8]. It can be minimized by adding another low-pass filter in a loop that encounters this 2ω term at the cost of reduction in bandwidth and/or phase-margin, slower transient response, and decrease in overall speed of synchronization[8]. Synchronous frame (DQ) PLLs can be adopted to compute frequency and phase angle as well as transform the grid voltage into DC signals. However, DQ PLL requires two signals i.e. a direct signal and an orthogonal signal (quadrature signal) for the computation of frequency and phase angle[9]. Therefore, an orthogonal signal is derived from the sensed grid voltage for the synchronous frame transformation by using different methods such as phase delay filters, differentiation of the input signal, Inverse Park's transform, Hilbert transform,and the second-order generalized integrator (SOGI)[10]. However, phase delay filters can cause inaccuracies to arise because of slow varying characteristics of the grid within tolerable range whereas differentiation of the input voltage signal is having an issue of noise amplification during the generation of the orthogonal signal[8,9]. The orthogonal signal generation using a Second Order Generalized Integrator (SOGI) offers band-pass filtering to eliminate the 2ω ripple without using LPFs. In a SOGI-PLL[10], SOGI is used to create direct/orthogonal for the synchronous frame while PLL is used to estimate the frequency and phase angle of the grid voltage. However, SOGI-PLL increases computation burden for estimating frequency and phase as well as increases settling time of dynamic performance due to the two-feedback path in the SOGI PLL structure. Moreover, due to inherent resonate characteristics; the SOGI employs to auto-tune the center frequency of the grid voltage with a single feedback loop by extending the SOGI structure with Frequency Locked Loop (FLL)[11]. The SOGI structure was modified with Frequency Locked Loop (FLL) to enhance the auto-tuning capability, which is a simple and robust extension of SOGI structure. However, SOGI-FLL is not capable to eliminate dc-offset generated due to the analog to digital conversion (ADCs) of sensed voltages. In the research paper[12], the modified SOGI (MSOGI) was proposed with the modification in standard SOGI by adding a forward gain path to get the benefit of double degree freedom for the rejection of dc-offset. However, the MSOGI with FLL becomes a third-order system as well three-control parameter to be a tune for the precise phase-angle detection and dc-offset rejection, which makes complexity in the implementation. Moreover, the research paper[12] also presented parallelism of the SOGI structure for harmonics elimination, but it will create more complexity for implantation as well as slow down the dynamic performance of the control system in the grid-connected application. Hence, researchers have put effort into high-ordered PLLs and FLLs[13] to achieve superior performance and dc-offset rejection by paying the cost of complexity in the implementation. To encounter the issue, Second Order Generalized Integrator (SOGI)-Frequency Locked Loop (FLL) method along with the dc-offset cancellation block are implemented to obtain superior performance without compromising the dynamics of the system as well as dc-offset rejection capability. Therefore, it can also eliminate the 2ω ripple without using LPFs and decreases computation time; subsequently, increase inherent synchronization speed as well as bandwidth as compared with convention PLL. In addition to the above work, this paper also an insight into active-power generation and reactive power compensation. The power factor deterioration[13–18] can be avoided by the presented control approach during the active/reactive power operation. The single-phase grid-assisted PV system is designed to inject power in the low voltage distribution network without exceeding voltage and harmonics limits as defined EN50160 and IEEE 1547 standards.

This paper mainly focuses on robust control of active and reactive power in the grid-assisted PV system using the SOGI based current control techniques and the SOGI-FLL as a grid synchronization technique. This paper is presented in five sections. Sections 2 describes the control strategy of grid-assisted PV systems including all key blocks like grid synchronization, dc-offset cancellation, voltage controller, and current controller. It also gives insight into the active/ reactive power control through a power electronic converter. Section 3 shows the experimental results of the grid-assisted PV system. The comparative study is discussed in section 4. The conclusive remark is written in section 5.

2 Control strategy of grid assisted PV system

Figure 1 illustrates the schematic of grid assisted PV system. The grid assisted PV system performs conversion of DC power of PV panel to AC power, which is finally dumped into the grid. The control system of grid assisted PV system consists of (i) MPPT based outer voltage controller for the active power injection into the grid,(ii) reactive power control outer-loop (iii) grid synchronization using the SOGI-FLL, (iv) the SOGI based current controller, and(v) synchronous frame transformation and the SPWM block.

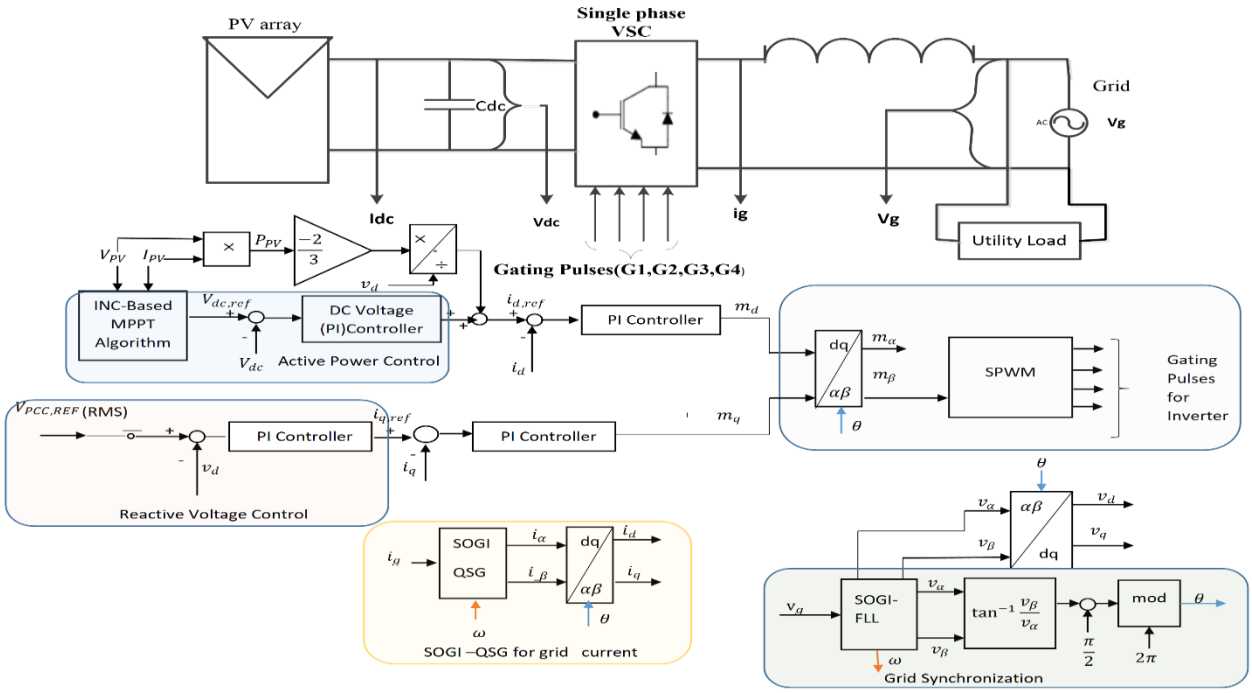

Fig 1. Schematic diagram of the control system of grid assisted PV inverter

The virtual two-axis synchronous reference frame current control techniques provide reactive power support to the grid for unity power factor at the common coupling, as shown in Figure 1. The perturb and observe (P&O) algorithm is an iterative method to extract maximum power from PV panel and is used here[13]. It is simple and well-known and presented in many research articles. However, this algorithm never reaches MPP but oscillates around it. It can be minimized by reducing the perturbation step size at the cost of slower MPPT. Many articles have been published on the modelling of the PV panels and MPPT algorithm. Hence, they are briefly discussed in this paper.

2.1 Structure of Second-Order Generalized Integrator (SOGI)

The structure of SOGI, as shown in Figure 2, and their transfer functions in equations (1) & (2) are indicating that two imaginary complex conjugated poles placed at $\pm j\omega_0$ that behaved like a resonator oscillating at an angular frequency ω_0. This feature offers infinite gain at resonator oscillating at the angular frequency, ω_0 as observed from the bode plot of SOGI in Figure 1(b) that can be useful in the implementation of voltage controlled oscillator (VCO) block in PLL. The transfer functions of SOGI are given as:

$$\frac{Y(s)}{v_{in}(s)} = \frac{\frac{\omega_0}{s}}{1+\frac{\omega_0}{s}\frac{\omega_0}{s}} = \frac{s\,\omega_0}{s^2+\omega_0^2} \tag{1}$$

$$\frac{Y'(s)}{v_{in}(s)} = \frac{Y'(s)}{Y(s)} * \frac{Y(s)}{v_{in}(s)} = \frac{\omega_0}{s} * \frac{s\,\omega_0}{s^2+\omega_0^2} = \frac{{\omega_0}^2}{s^2+\omega_0^2} \tag{2}$$

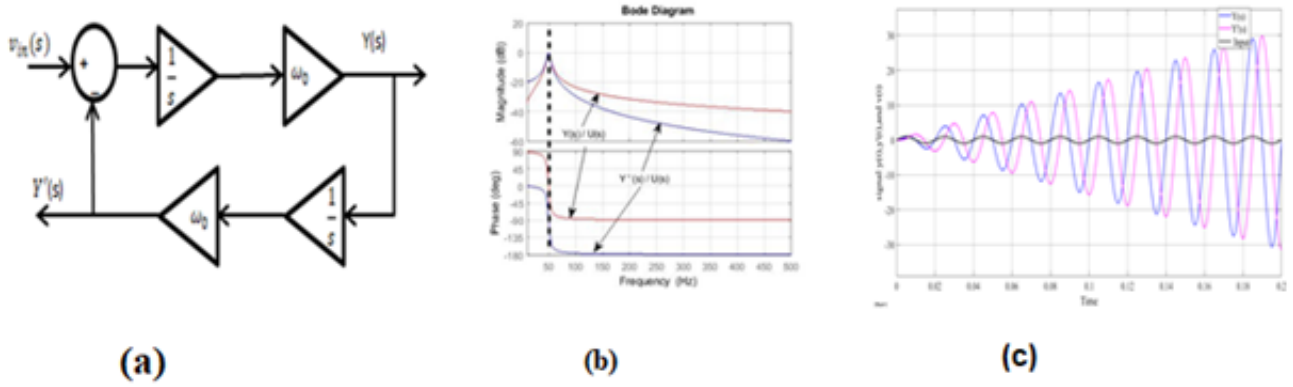

Fig 2. (a) Basic structure of Second-order generalized integrator [10], (b) Bode diagram of transfer function (Y(s) / Vin (s))and (Y'(s) / Vin (s))of SOGI , and (c) Step response of SOGI

$$y(t) = L^{-1}[Y(s)] = L^{-1}\left[\frac{s\omega_0}{s^2+\omega_0^2} * v_{in}(s)\right] = L^{-1}\left[\frac{s\omega_0}{s^2+\omega_0^2} * \frac{\omega_0}{s^2+\omega_0^2}\right] = \frac{1}{2}[t\omega_0 \sin\omega_0 t] \tag{3}$$

$$y'(t) = L^{-1}[Y'(s)] = \frac{1}{2}[\sin\omega_0 t t\omega_0 \cos\omega_0 t] \tag{4}$$

Figure 2 (c) shows the step time response of a SOGI structure as per the equation. (3) & equation. (4) with $\omega_0 = 2\pi.50$ rad/s, respectively, that increase the amplitude of output signals which cause an unstable system, when a unitary step is applied as input. To prevent the system to be unstable, the input to the SOGI structure is modified as weighted k of (where k is the gain parameter of the SOGI) the difference of input signal which is nothing but grid voltage $v_{in}(s)$and unity feedback of output signal Y(s) to the input as shown inFigure 3.

The transfer functions $D_v(s)$ and $Q_v(s)$ are rewritten as:

$$D_v(s) = \frac{Y(s)}{v_{in}(s)} = \frac{k\ s\ \omega_0}{s^2 + k\omega_0 s + \ \omega_0{}^2} \tag{5}$$

$$Q_v(s) = \frac{Y'(s)}{v_{in}(s)} = \frac{k\ s\ \omega_0}{s^2 + k\omega_0 s + \ \omega_0{}^2} \tag{6}$$

Bode Diagrams describe band-pass compatible nature of the output Y(s) (Figure 3 (b)) and nature of the output Y'(s) as low-pass compatible, while phase responses of curves at frequency 50Hz are observed at 0° and 90° respectively which indicates that Y(s) is having 90° phase lead to Y'(s) (Figure 3 (c)). Moreover, the magnitude responses of Bode are maintaining 0 dB at the 50Hz fundamental frequency and attenuating amplitude at 5th and 7th harmonics frequency i.e.250Hz and 350Hz. It is seen from Figure 3 that the transfer function Y(s) and Y'(s) can extract only fundamental components of grid voltage while eliminating harmonics components of grid voltage as a second-order band-pass filter.

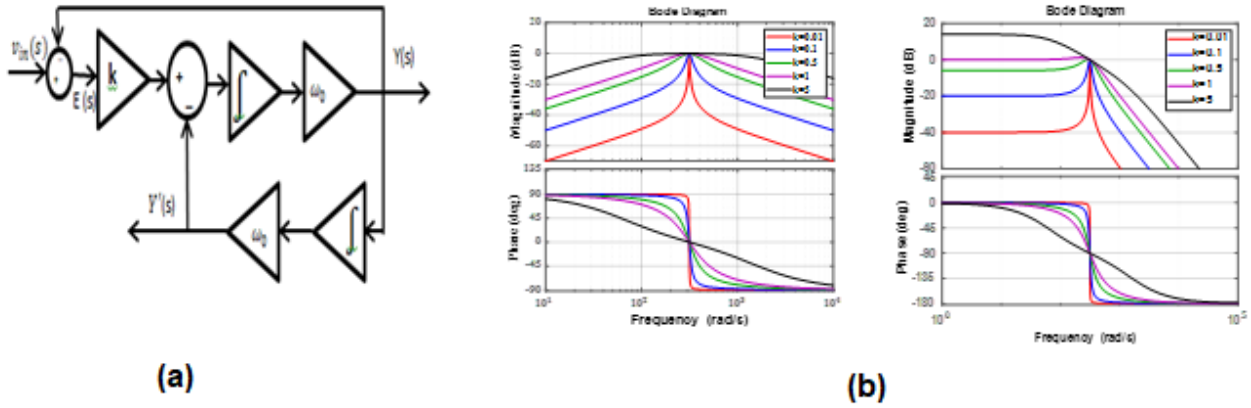

Fig 3. (a) Block diagram of SOGI-OSG, and (b) Bode Diagram of (a) $D_v(s)$, and (b) $Q_v(s)$with a different value of k

2.2 Frequency locked loop

However, SOGI has an inherent resonate character that can use as a voltage-controlled oscillator, which emphasizes to design a simple and robust single feedback control loop for an auto-adapting center frequency of the SOGI resonator as per the input grid frequency. Frequency Locked Loop, FLL is nothing but the simple and robust extension of the SOGI structure as shown in Figure 4 (a). In order to make auto- tunable SOGI-QSG, it should pay attention to the voltage error signal $E_v\ (s)$, which is nothing but the difference between the input $v_{in}\ (s)$ and output Y(s) and behave as a notch filter with zero gain and180^o phase-angle jump at a center frequency as observed from the bode diagram in Figure 4(b), is described in term of the transfer function by

$$E_v\ (s) = \frac{\varepsilon_{v(s)}}{v_{in(s)}} = \frac{s^2 + \omega_0{}^2}{s^2 + k\omega_0 s + \omega_0{}^2} \tag{7}$$

Figure 4 (b) presents the dc blocker for eliminating the dc-offset generated due to the analog to digital conversion (ADCs). The transfer function of $E_v\ (s)$ and $Q_v\ (s)$ gives worthy information for an auto-tunable frequency control system by taking a common bode diagram of the transfer function $E_v\ (s)$ and $Q_v\ (s)$, as depicted in Figure 4(c). The Bode diagram of transfer functions, $E_v\ (s)$ and$Q_v\ (s)$, reveal that the phase of signals $E_v\ (s)$ and $Q_v\ (s)$ are in a phase when input frequency (ω) lower than the SOGI resonance frequency ($\omega^{'}$) i.e. $\omega < \omega^{'}$ and out of a phase (180^o phase difference) when $\omega > \omega^{'}$, as indicated in Figure 4 (c).

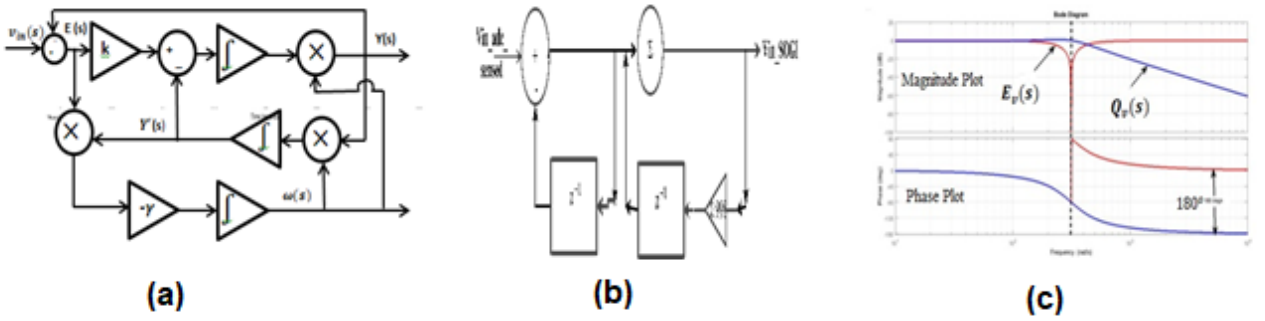

Fig 4. (a).The basic structure of SOGI based Frequency lock loop,(b) dc-offset cancellation block, and(c) Bode Diagram of the $E_v(s)$ and $Q_v(s)$in a SOGI- QSG

Hence, a frequency error variable ε_f is derived from the product of $E_v(s)$ and $Q_v(s)$, which remain positive when input frequency (ω) is lower than the SOGI resonance frequency (ω'), zero when $\omega = \omega'$, and remain negative $\omega > \omega'$ in the SOGI-FLL. Moreover, the frequency-locking loop (FLL) can be designed by using frequency error variable, ε_f , and a negative value of frequency loop controller gain,$-\gamma$ as shown in Figure 4 (a). The frequency loop controller gain ($-\gamma$) is used to achieving DC component of the frequency error variable ε_f equal to zero by changing SOGI resonance frequency, ω', until equal to the input frequency, ω. A feed-forward variable, ω_c i.e. nominal value of grid frequency is provided in the frequency locking loop(FLL) to speed up the initial synchronization process. The SOGI-OSG and Frequency locking loop combined a structure diagram known as SOGI-FLL for a single-phase grid synchronization system, as shown in Figure 4. The transient and steady-state behavior of the SOGI –FLL mainly depends on a suitable value chosen for control parameters γ and k in order to obtain the desired response in the estimation of the frequency and amplitude of the input signal.

2.3 DC-offset cancellation block

The dc-offset presents due to the analog to digital conversion(ADCs) and signal conditioning and the SOGI structure is inefficient to eliminate the dc offset as observed from the bode diagram, shown in Figure 3 (b). The Bode diagram of the SOGI presents the inability to attenuate low-frequency components especially the dc signal from the grid voltage. It is very well common that integration of DC value yields steps signal, further integration produces a ramp signal. The presence of a DC-offset in the sensed grid voltage deteriorates the performance of a SOGI. The conversion of the continuous-time input signal into digital values generates an error, commonly known as quantization error. This error arises due to the input signal by a fixed number of digits in the ADC conversion process. If a normalized sinusoidal signal (i.e. amplitude varies between +1 to -1) is to be converted into digital ADC, it employs (b+1) bits including sign bits. The number of levels and quantization step size is 2^{b+1} and $\frac{2}{2^{b+1}} = 2^{-b}$ respectively. The quantization error is experienced due to rounding, which is the process of reducing the size of a binary number of a finite word size of b bits such that the rounded b-bit number to closest to the original un-quantized input signal. The quantization error, $e(n)$ is given by

$$e(n) = x_q(n) - x(n) \quad ; \quad x_q(n) = x(n) + e(n) \tag{8}$$

Where $x_q(n)$ and $x(n)$ are the sampled quantized value and the sample un-quantized value of the input signal to the ADCs respectively. Due to the rounding, the error signal obeys the following relations: $\frac{-q}{2} \leq e(n) \geq \frac{q}{2}$. In signal processing, a quantization error is commonly viewed as an unwanted discrete noise signal. Therefore, the output signal from the ADC is the sum of input signal $x(n)$ and error signal $e(n)$ as described in equation (8). The variance or power of the error signal $e(n)$ is given by:

$$\sigma_e^2 = \left\{E\left(e^2(n)\right)\right\} - \left\{E^2(e(n))\right\} = \left\{\frac{q^2}{12} - (0)\right\} = \frac{2^{-2b}}{12} \tag{9}$$

Here, $E(e(n))$ is the mean value of $e(n)$ and it is zero while $E\left(e^2(n)\right)$ is the average value of $e^2(n)$ and $p(e)$ is the probability density function.

The average value of $e^2(n)$ is mathematically described as:

$$E\left(e^2(n)\right) = \int_{-\infty}^{\infty} e^2(n)p(e)de = \frac{1}{q}\int_{-q/2}^{q/2} e^2(n)de = \frac{q^2}{12}; p(e) = \frac{1}{q} \quad \text{for } \frac{-q}{2} \leq e(n) \leq \frac{q}{2} \tag{10}$$

The output signal of an ADC converter is passed through a first-order filter and described by

$$y(n) = ay(n-1) + x(n) \tag{11}$$

Besides, the transfer function of the system and impulse response of the system is given as:

$$H(z) = \frac{Y(z)}{x(z)} = \frac{z}{z-a}; h(n) = a^n u(n) \tag{12}$$

The steady-state variance of a noise or quantization noise presents in the input signal is given as

$$\sigma_\varepsilon^2 = \sigma_e^2 \sum_{k=0}^{\infty} h(n)^2 = \sigma_e^2 \left[\frac{1}{1-a^2}\right] = \frac{2^{-2b}}{12}\left[\frac{1}{1-a^2}\right] \tag{13}$$

Generally, digital signal processors have 10-bit or 12-bit ADCs. To eliminate the steady-state variance or quantization noise in the input signal, a is preferably chosen from the range $0.5 \leq a \leq 0.99$ (ideally a lies between 0 <a<1 to remain Region of convergence (ROC) inside the unit circle for the stability). Assume a=0.98 and 12-bit digital signal processor, the quantization noise at the output of the filter is 4.2088e-22≈ 0.

2.4 PV inverter control

The active power injection is controlled by DC voltage controller as shown in Figure 1 .The PV voltage (Vdc) is sensed through the hall sensor and given to first-order low pass filter to block switching ripples. The DC voltage reference is generated by MPPT algorithm as shown in Figure 1. The difference of DC reference voltage and actual voltage is fed to a PI controller to extract maximum power from PV panel. The voltage error of DC link ($\triangle v_{dc,\,err}$) in nth sampling instant is described as:

$$\Delta v_{dc,err} = V^{*}_{dc,(MPPT)} - V_{dc,sensed} \tag{14}$$

The direct/ orthogonal component of current is created from the sensed grid current. The i_d and i_q are computed by the dq transformation. The error signal is generated by taking the difference of reference currents (i.e. $i_{d,ref}$ and$i_{q,ref}$) and computed i_d andi_q, which is further given to PI controller to generated duty cycles of the inverter (i.e. m_d and m_q)

The active current reference of the inverter at the nth sample is given as:

$$i_{d,ref} = K_{p1,dc}\left(\Delta v_{dc,err}\right) + K_{p1,dc}\left(\Delta v_{dc,err}\right) - \frac{2}{3}\frac{V_{PV}(n)I_{PV}(n)}{V_d(n-1)} \tag{15}$$

The reactive current reference of inverter at nth sample is given as:

$$i_{q,ref} = K_{p2,dc}\left\{V_{g,RMS}(\mathrm{n}) - V_d(\mathrm{n})\right\} + K_{i2,dc}\left\{V_{g,RMS}(\mathrm{n}) - V_d(\mathrm{n})\right\} \tag{16}$$

The duty cycles (m_d and m_q) of PV inverter at nth instant are represented as:

$$m_d = K_{p,\,\mathrm{inner}}\left\{i_{d,\,\mathrm{ref}}(\mathrm{n}) - i_d(\mathrm{n})\right\} + K_{i,\,\mathrm{inner}}\left\{i_{d,\,\mathrm{ref}}(\mathrm{n}) - i_d(\mathrm{n})\right\} \tag{17}$$

$$m_q = K_{p,\,\mathrm{inner}}\left\{i_{q,ref}(\mathrm{n}) - i_q(\mathrm{n})\right\} + K_{i,\,\mathrm{inner}}\left\{i_{q,ref}(\mathrm{n}) - i_q(\mathrm{n})\right\} \tag{18}$$

Here, $K_{p1,dc}$ and $K_{i1,dc}$ are proportional gain and integral gain of DC voltage controller respectively. $K_{p2,dc}$ & $K_{i2,dc}$ are proportional gain and integral gain of reactive power controller respectively. In the inner current loop, $K_{p,inner}$ and $K_{i,inner}$ are proportional gain and integral gain of dq- axis current controller.

Using the inverse park transformation, the modulating signal is generated as

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} m_d \\ m_q \end{bmatrix} \tag{19}$$

For the SPWM techniques, v_β is given as modulating signal and represented as:

$$v_\beta = m_d \sin\theta + m_q \cos\theta \tag{20}$$

If PV inverter only performs active power injection at that moment, m_q is zero and v_β is given as

$$v_\beta = m_d \sin\theta \tag{21}$$

The SPWM technique is used to generate gating signals for the power electronics switches and the inductor filter use as a bridge between the power electronic converter and grid.

2.5 Delay compensation block

Due to the computation of the control approach, it will inherently afford unit sample delay between the computed reference signal and actual signal. Indeed, the converter reference signals that are computed at the kth sample are given to the converter at the beginning of the (k+ 1)th sample. This inherent computation sample delay degrades the performance of the control approach. To compensate the computation sample delay, converter reference signals at the (k+ 1)th sample is predicted from the reference signals at the present sample i.e. kth sample and past sample i.e.(k-1)th sample, as presented in the eq. (16).

$$x^{*}_{ref}(k+1) = 2x^{*}_{ref}(k) - x^{*}_{ref}(k-1) \tag{22}$$

3 Experimental Results

The SOGI-FLL is implemented and tested by using a downscaled STM32F407VGT6 microcontroller and waijung block-set environment in the Simulink/MATLAB. The discrete- SOGI-FLL model is converted into c code, that further, compiled and dumped into microcontroller by KEIL-IDE (KEIL 4 and above, ST-utility driver) and physical interface USB cable. The STM32F407VGT6 is a low-cost, 32-bit microcontroller having two digital-analog converters (12bit-DAC) with 168 MHz crystal frequency, and supported by the waijung environment (i.e. model-based programming) in the SIMULINK/MATLAB. The convenient parameter value of the SOGI-FLL are chosen as k = 0.5,$\gamma = -5000$, sampling time t_s = 50 usec, and the grid voltage frequency f_g = 50 Hz. The DC-offset is generated due to the ADC conversion block and other discrete blocks cause uncertainty in the phase-detection of the SOGI –FLL. However, many researchers presented many improved structures of the SOGI-FLL. The SOGI-FLL was used along with a first-order infinite-impulse response (IIR) filter (i.e. known as DC blocker) to eliminate a DC offset without moving toward a complex modification in the structure. For the validation, SOGI-FLL is tested under the various cases individually in the experimental set-up as follow:

Test 1: It is conducted on the grid voltage affected by voltage sag of 0.6 p.u. and 5% of a DC-offset.

Test 2: It is conducted on the grid voltage experiences a -5 Hz frequency step change (i.e. frequency jump (50Hz to 45Hz), phase-angle shift (0^0 to45^0) and 5% of a DC-offset.

Test 3: It is conducted on the grid voltage affected by harmonics and 5% of a DC-offset.

In Figure 5, experimental results are obtained to measure the settling time of the SOGI-FLL on the grid voltage affected by a voltage sag of the magnitude 0.6 p.u at t=200 msec. These results are only visible in the digital oscilloscope has a frequency above 70 MHz and change must be applied after 200msec. Figure 5 shows that v_α/v' of SOGI-FLL settled down before the third cycle i.e 50 msec when grid voltage affected by sag of 0.6 p.u. and 5% of a DC-offset.

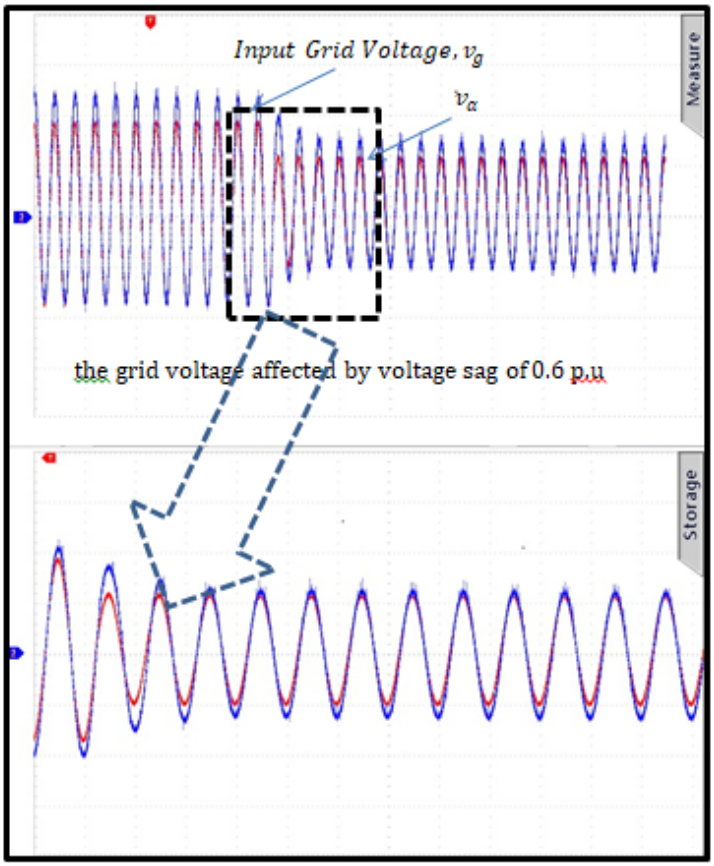

Fig 5. Experimental results: output signalv_α of SOGI-FLL with input grid voltage characterized simultaneously dc offset, voltage sag of 0.6 p.u. and 5% of DC-offset.

As shown in Figure 6, the dynamic response of SOGI-FLL is evaluated by performing experimental test-2 i.e. grid voltage experiences a -5 Hz frequency step change (frequency jump from 50Hz to 45Hz) and phase angle shift (0^0 to 45^0) at t =500msec. The phase-angle shift (from 0^o to 45^o) is intentionally made only to observe frequency change occurs at t =500msec, as shown in Figure 6. The frequency and phase-angle detected by the SOGI-FLL are settled down before the second cycle observe from the time instant at which the frequency shift is made in the grid voltage.

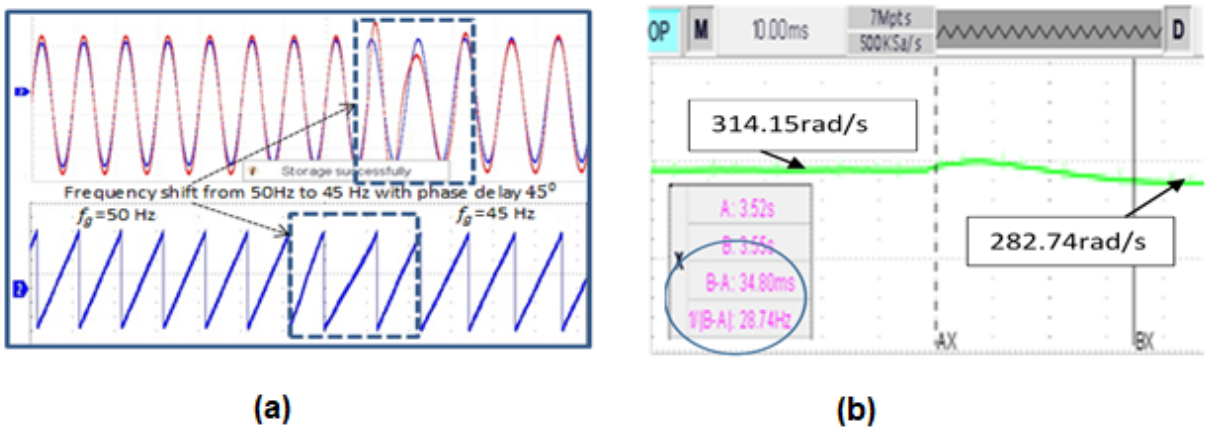

Fig 6. Experimental results: output signal v_α of SOGI-FLL with input grid voltage encountered with frequency jump (from 50Hz to 45Hz) and phase angle shift (0° to 45°), and also phase-angle detected by SOGI-FLL, (b) angular frequency

Due to the unavailability of AC grid simulator, test-3 is conducted by generating sin wave inside SIMULINK/MATLAB and frequency controlled by externally through the ADC pin of a microcontroller. As shown in the Figure 7, the dynamic response of SOGI-FLL is evaluated by performing experimental test-3 i.e. grid voltage affected by 3rd, 5th and 7th order harmonics with proportional amplitudes of 35%, 15%, and 8%, respectively, concerning fundamental grid voltage.

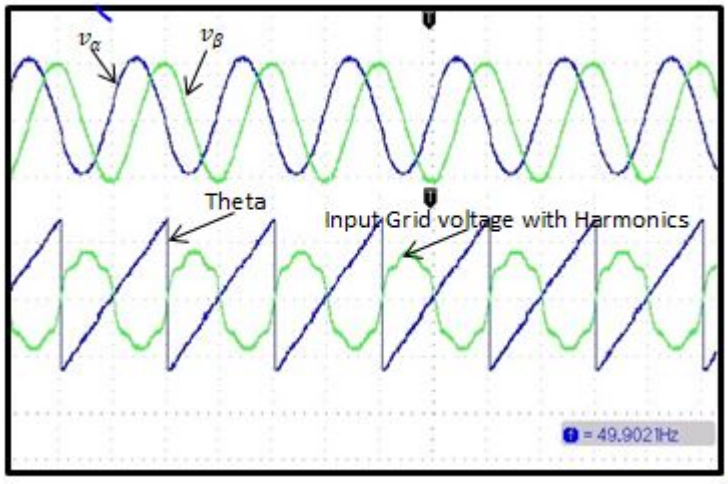

Fig 7. Experimental results: output signal v_α& $v_\beta$of SOGI-FLL with input grid voltage affected by harmonics component, and phase angle shift (0^0 to45^0), and also phase-angle detected by SOGI-FLL

Besides, the SOGI-QSG is experimentally proven as band-pass filter through the output signal of SOGI-FLL i.e. v_α/v' and v_β/qv' free from the effect of harmonics distortion as shown in Figure 8. The SOGI-FLL works in the same fashion even in the situation when the grid voltage is affected by multiple abnormalities. An experimental setup of a grid-assisted PV system implemented using a single-phase IBGT based power converter card, an IGBT driver card with short-circuit protection,

STM32F407VG 32-bit DSP based microcontroller, current and voltage Hall sensor for DC side, current transformer (CT) and power transformer (PT) for ac side along with the features of DC offset adjustment for uni-polar ADC in a microcontroller, line inductor, 2 series-connected PV panel strings, and step-up transformer interface between PV system and the utility grid. The experimental results are obtained by using the experimental setup of a grid-assisted PV system with the specification mention in Table 1. Figure 8 shows the experimental result of grid voltage and inverter current during various conditions (i) No-load conditions, (ii) inductive load connected at common coupling point, and (iii) load connected at the common coupling point.

Table 1. Experimental setup specification for the grid assisted PV system

PV panel specification	250 Watts; V_{oc} =37.20 ;V ;Vmp=30.80V ;Isc = 8.96 A; Imp=8.12 A No. of series connection :2 ; No. of parallel connection :1 ;
MPPT and PLL techniques	P& O MPPT algorithm; SOGI-FLL grid synchronization
Inverter Specification	Switching frequency = 2 KHz, $K_{p1,dc}$ =5 ; $K_{i1,dc}$=0.001; $K_{p2,dc}$ =2 ; $K_{i2,dc}$=0.001; $K_{p,inner}$ =40 ; $K_{i,inner}$= 0.0001 Sampling Time, Ts= 10e-6; MPPT Sampling Time = 150*Ts Inner Loop sampling time = 10*Ts ;Outer loop sampling time = 100*Ts
Filter	L = 5mH
DC link capacitor	470uF (100V)
Grid side Transformer	30V to 230V

Figure 8(a) presents that active power injected into the grid as well as grid voltage and inverter current is out of the phase. Figure 8(b) and (c) present that active power and reactive power supported by the inverter to the grid. The inverter behaves as capacitive when inductive load connected at common coupling point while inductive when capacitive load connected at common coupling point, shown in Figure 8 (b) and (c).

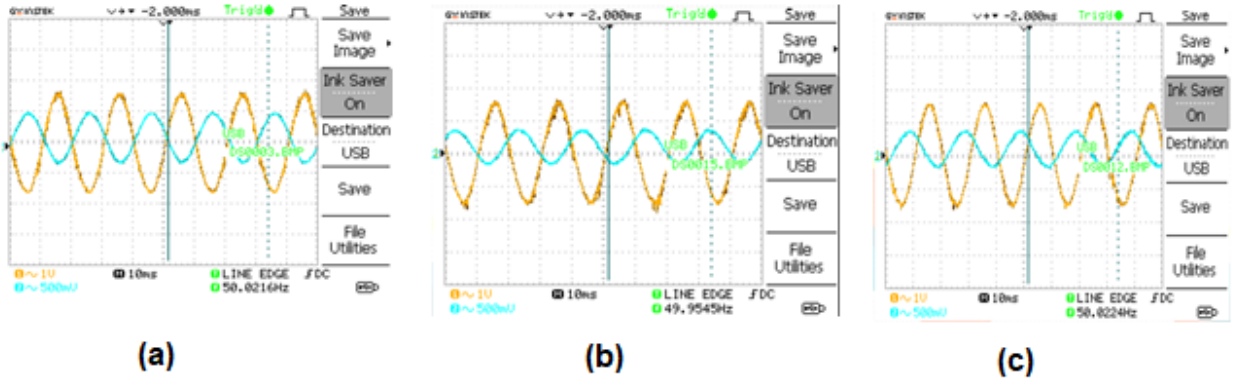

Fig 8. (a) Grid voltage and Inverter current during a no-load conditions, (b) Grid voltage and Inverter current during a capacitive load, and (c) Grid voltage and Inverter current during a inductive load [Note: yellow color indicates grid voltage, blue color indicates inverter current, and Time scale: 10ms/div]

4 Discussion

In very recent years, some attempts for designing high-order frequency-locked loops (FLLs) have become common practice for the elimination of dc-offset. Nevertheless, the merits and demerits of these structures, particularly in comparison with a SOGI-FLL and high-order PLLs, are rather unclear. The high-order PLLs and FLLs knowledge provides fast and accurate phase angle extraction by paying the cost of hardware implementation complexity. Many researchers put efforts into the implementation of the SOGI-FLL in the single-phase grid-assisted PV system, but none of the above have focused on the impact analysis of parameter k and γ and their effects in the transient and steady-state response SOGI-FLL. The dynamic performance of the frequency estimation in the SOGI-FLL is examined by experiencing a -5 Hz frequency step change (i.e. frequency jump (50Hz to 45Hz) and phase-angle shift (0° to 45°)at the 200msec with the feed-forward taking the initial frequency value i.e. $2\pi * 50$. In Figure 9 (a) & (b), the dynamic response of the frequency estimation is observed by taking a progressive value of k and constant value of γ while the progressive value of γ and constant value of k, as depicted in Figure 9(c) & (d). Impact analysis of

parameters k and γ in SOGI-FLL tabulated from Figure 9(a)-(d) in Table 2. The parameter k is used to amplify signal (ε_v), which affects the transient response and bandwidth and of the SOGI-FLL. The selection of the gain k is compromising between good signal filtering and the dynamic response of the system (Figures 3 and 9). The selection of the γ value is a trade-off between the precision of the frequency estimation and dynamics of the SOGI-FLL.

Table 2. Impact analysis of SOGI-FLL

Parameter	Progressive change	Transient response	Steady-state response	Filtering	Settling Time
k	Increasing	Good	Good	Good	Reduce
	Decreasing	Poor	Poor	Poor	Increase
γ	Increasing	Poor	moderate	No effect	Reduce
	Decreasing	Good	Good	No effect	Increase

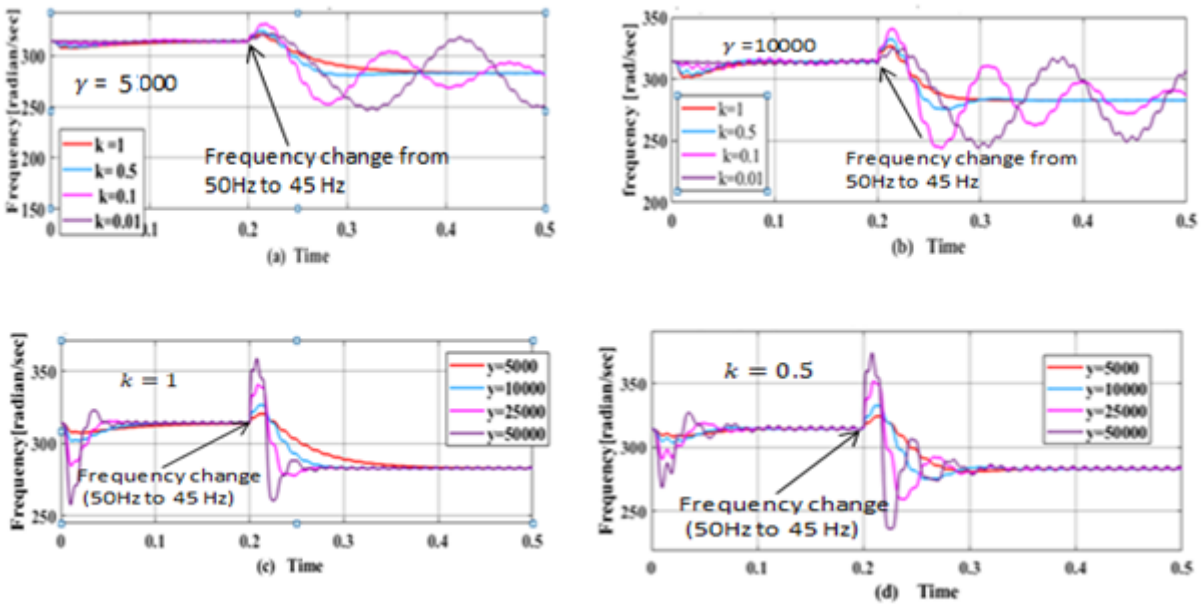

Fig 9. tep responseof Frequency Estimation (a) different value of k ,constant value γ=5000, (b) different value of k ,constant value γ=10000, (c) different value of γ ,constant value k=1, and (d) different value of γ ,constant value k=0.5

Narrower bandwidth increases the rise time (t_r= 0.35/ BW), further, degrades the successive value stabilization of frequency estimation, however, adversely improves the other parameters. The SOGI-FLL has superior performance over the other grid synchronization techniques except for DC-offset elimination. The DC-offset cancellation block before the SOGI-FLL eliminates the DC-offset without degrading the performance of SOGI-FLL. The delay compensation block improves the dynamics of the control approach to ensure the power quality at the PCC. The notable contribution in this paper can be summarized as follows:

1. SOGI-FLL has proven its ability to eliminate dc-offset generated due to the ADC conversion by adding DC blocker without increasing the tuning complexity of the control parameters in the SOGI-FLL.
2. The appropriate selection of control parameter in the SOGI-FLL improves synchronization speeds during the grid abnormality, increases robustness against input noise and disturbances, and estimates accurate and non-distorted values phase-angle for the control system. The impact analysis of parameter k and γ and their effects in transient and steady-state response SOGI-FLL.
3. The single-stage single-phase grid assisted PV system performs active power-sharing as availability of solar energy with reactive power compensation to achieve unity power factor at the utility.

5 Conclusions

In this study, attention was paid to estimate the frequency and further phase-angle detection by the SOGI-FLL method for changing the frequency and voltage of the single-phase utility. To this end, SOGI-FLL implementation with dc-offset cancellation block is presented for enhancing the capability of fast and precise phase-angle detection, harmonics and dc-offset rejection. It is confirmed by experimental and simulation results that there is no need to choose high-order FLLs or PLLs for the dc-offset rejection. Moreover, simulation assessment is also proven that the appropriate selection of control parameters is a trade-off between the dynamic response, filtering capability and the desired accuracy in detection of frequency and phase angle especially during non-ideal grid conditions for single-phase grid-tied inverter. The Virtual two-axis reference frame (SOGI based) power control for the single-stage grid-assisted PV system was implemented by utilizing an additional capacity power electronic converter to provide reactive power support to the grid. During a no-load condition, the PV inverter is only dumping active power into the grid. The PV inverter is behaving as inductive during capacitive load connected whereas capacitive when inductive load connected to common coupling point, as confirmed through experimentation.

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