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RESEARCH ARTICLE

Power Efficient Biquadratic Filter designing using OTA

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Abstract

Objectives: To present a power efficient Universal Biquad Operational Transconductance Amplifier circuit. **Methods:** OTA (operational transconductance amplifier) based Biquad filter is analyzed using three different simulated tools three different tools (CADENCE, XILINX, ORCAD and MATLAB tools) are used for designing the circuit. The 0.18μm CMOS technique is used using the Cadence tool for plan and reproduction. The same circuit has been implemented on ORCAD tool as well as Xilinx tool. **Findings**: The proposed Biquad filter improves the frequency response, power dissipation and provides vary of the KHN biquadratic filter circuits it uses minimum numbers of Operational Transconductance phenomenon Amplifier (OTA) to realize an equivalent. The assorted parameters specifically Center frequency, dcgain, Bandwidth, Power Dissipation and Quality issue are all electronically tunable. OTA based Biquad filter is simulated in CADENCE Virtuoso tool. Opamp-RC Biquad filter offers a bandwidth of 425 kHz, pass band gain of zero DB, whereas Gm-C measuring system based mostly filter offers 85MHz, passband gain of zero DB. Over-all power dissipation of the Biquad filter is 4.3mW with 1.8V DC Supply has basing current of 50μA with gracefully voltage $\pm$2.5v. by keeping the supply voltage, bias current and load capacitor as 2.5V, 50μA and 10pFrespectively, it has been seen that the power is reduced using the CADENCE virtuoso tool. **Novelty :** This study presents a Universal Biquadratic filter having less power dissipation. The circuit was optimized for gain, GBP, slew rate, areas, voltage offset, phase margin, power area etc. compared to all the previous filter circuits (OTA GMC filters, OTA type-C filters) designed with the help of OTA.

Keywords: OTA; CMOS; CADENCE Virtuoso; Static Power; Dynamic Power; MOSFET

1 Introduction

In the current scenario Digital Circuit is more common to use because it is easy to carry and provides lot of feasibility in day-to-day regular life but digital circuit faces two major problems that is define as environmental effect and supply variation of the circuit that is degrade the circuit performance. To reduce that problem som e of the researcher gives the concept of body bias of the MOSFET but due to body bias a leakage current come

on the picture and provide high power dissipation [1].

The first commercially available integrated circuit units were produced by RCA in 1969 (before being acquired by General Electric), in the form of the CA3080 (discontinued product) and they have been improved since that time for the designing [2,3]. Although most units are constructed with bipolar transistors, field effect transistor units are also produced. The OTA is not as useful by itself in the vast majority of standard op-amp functions as the ordinary op-amp because its output is a current. One of its principal uses is in implementing electronically controlled applications such as variable frequency oscillators and filters and variable gain amplifier stages which are more difficult to implement with standard op-amps [4].

Inductorless GHz-band lowpass filters within the literature area unit usually supported RLC reference structures, with the employment of active inductance circuits to substitute the physical inductors. However, implementations supported the Gm-C [5] approach area unit quite common, and filters supported the closed-loop system Sallen–Key [6] and Tow–Thomas Biquad filter [6] topologies have additionally been reportable within the low-GHz vary. closed-loop system filter architectures supported non-conventional active building blocks such as second-generation current conveyors [5] or second-generation voltage conveyors [6] have been additionally exploited at lower frequencies. However, only a few lowpass filter implementations higher than 4 Gc area unit reportable within the literature, and none of them area unit supported closed-loop architectures. In the Biquad filter [7], a tunable fifth order elliptic Gm-C lowpass filter in a hundred and 70 GHz-fT SiGe BiCMOS with a most information measure of four.1 Gc was reportable, and a third order Gm-C filter with a most information measure of 10 Gc, in 65-nm CMOS was reportable. Filters supported the active inductance approach are given in [6], that reports a fifth order 4.57-GHz lowpass filter in 180-nm CMOS that describes a 10.5-GHz Biquad in SiGe HBT technology.

On the opposite hand, the ever-increasing frequency performance of advanced bipolar technologies and deep submicron CMOS permits achieving vast gain-bandwidth merchandise, therefore creating it doable to adopt a closed-loop approach for the planning of multi-GHz filters. this enables mistreatment filter style techniques that area unit usually adopted at lower frequencies, each for the topology of the essential filter stage, the Biquad, and for the system style of upper order filters below technology constraints (e.g., limits on the most quality issue which will be achieved) [8,9]. The closed-loop approach offers the benefits of multiplied dimensionality and low sensitivity to active devices variations, because of feedback; the filter characteristics area unit associated with the values of passive elements and/or to their ratios, and will be simply tuned, e.g., by mistreatment varactors. The key differences between the OTA and the conventional op-amp are that the OTA is a current source and the output impedance of this amplifier is high in contrast to the op-amp's very low output impedance. As a result, low output impedance is often a desirable trait in general amplifiers used to drive resistive loads, certain of the newer commercial OTA's have on-chip controlled impedance buffers.

It is possible to design circuits using the OTA that do not employ negative feedback. Instead of employing feedback to reduce the sensitivity of a circuit's performance to device parameters, the Transconductance is treated as a design parameter, much as resistors and capacitors are treated in op-amp based circuits [5]. It is usually used open-loop because the magnitude of the output resistance controls its output voltage and a resistance can be chosen to keep the output from going into saturation, even with high differential input voltage. The output of the OTA is a current signal whereas in a standard operational amplifier the output is a voltage signal [6,7].

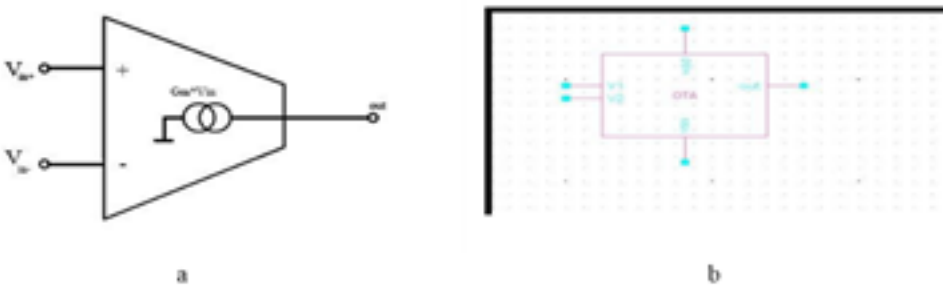

Fig 1. (a) OTA symbol, (b) OTAsymbol using CADENCE tool

OTA symbol can be designed with the help of CADENCE virtuoso tool [5]. In the ideal OTA, the output current is a linear function of the differential input voltage, calculated as follows:

$$I_{out} = (V_{in+} - V_{in-}) \cdot g_m$$

Where Vin+ is the voltage at the non-inverting input, Vin− is the voltage at the inverting input and Gm is the transconductance of the amplifier[10,11]. The transconductance of the amplifier is usually controlled by an input amplifier bias current denoted as Iout. The amplifier's transconductance is directly proportional to this current. This is the feature that makes it useful for electronic control of amplifier gain.

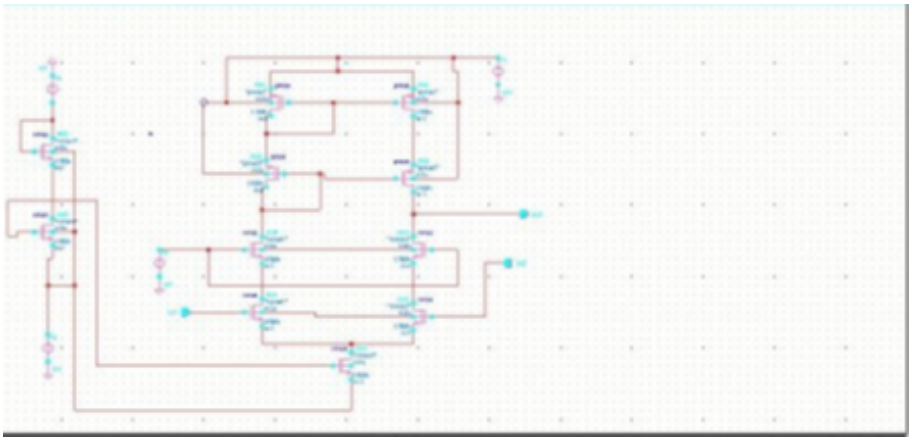

Fig 2. Reference OTA circuit

2 Proposed OTA Circuit

The proposed circuit obtain by the using of two capacitors more added to the circuit.In this paper we use OTA symbol for designing the schematic of the LPF, HPF, BPF and Universal Biquad Filter circuit.

PM0,PM1,PM2,PM3	$10\mu/2\mu$	NM0,NM1,NM2,NM3,NM4, NM5	$10\mu/2\mu$	R0	50KΩ
R1	100KΩ	Vdc	x	p/n	m:1

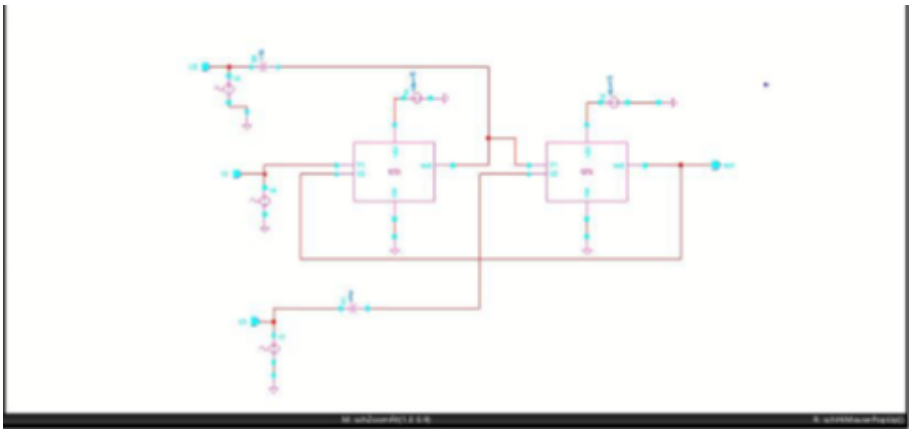

Fig 3. Proposed Universal Biquad Filter Circuit using OTA (operational transconductance amplifier)

Before designing the LPF by using the OTA first we have designed the schematic of LPF with the help of other tools like ORCAD, CADENCE and MATLAB tool. The circuit schematic of LPF by using the OTA symbol is designed with the help of the CADENCE virtuoso tool.

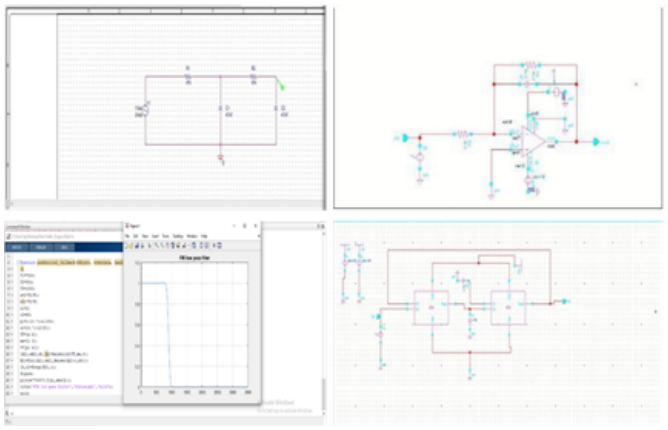

Fig 4. Proposed schematic of LPF Circuit using OTA

The transfer function of the LPF can be written as:

$$\frac{w_0^2}{(jw)^2 + jw(w_0/Q) + w_0^2}$$

the response of the LPF by using the various tools can be shown as:

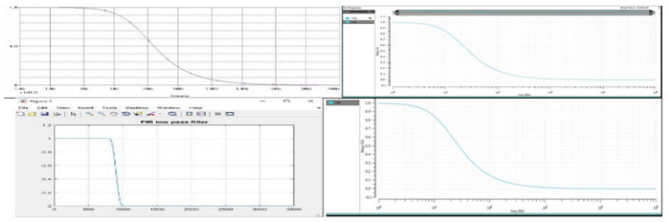

Fig 5. Proposed response of LPF Circuit using OTA

Before designing the HPF by using the OTA first we have designed the schematic of HPF with the help of other tools like ORCAD, CADENCE and MATLAB tool. The circuit schematic of HPF by using the OTA symbol is designed with the help of the CADENCE virtuoso tool.

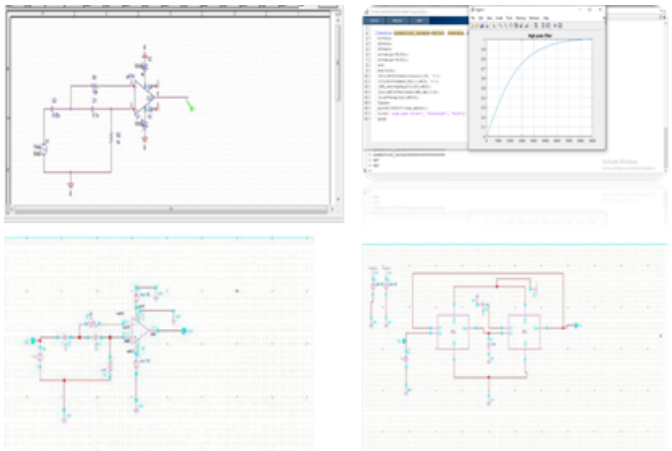

Fig 6. Proposed schematic of HPF Circuit using OTA

The transfer function of the HPF can be written as:

$$\frac{(jw)^2}{(jw)^2 + jw\,(w_0/Q) + w_0{}^2}$$

the response of the HPF by using the various tools can be shown as:

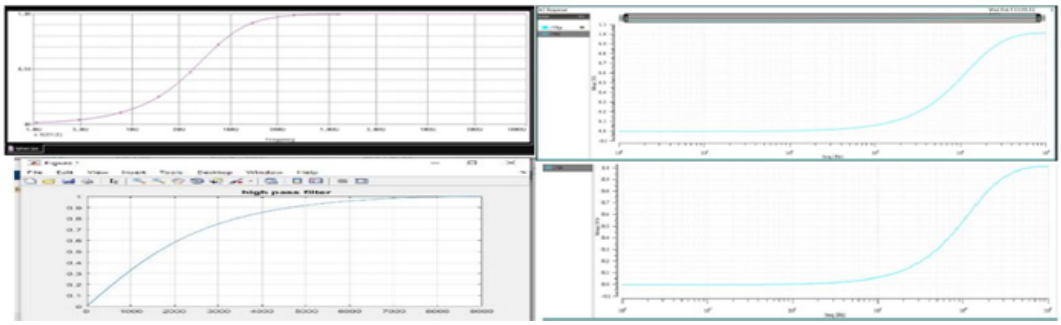

Fig 7. Proposed response of HPF Circuit using OTA

Before designing the BPF by using the OTA first we have designed the schematic of BPF with the help of other tools like ORCAD, CADENCE and MATLAB tool[8]. The circuit schematic of BPF by using the OTA symbol is designed with the help of the CADENCE virtuoso tool.

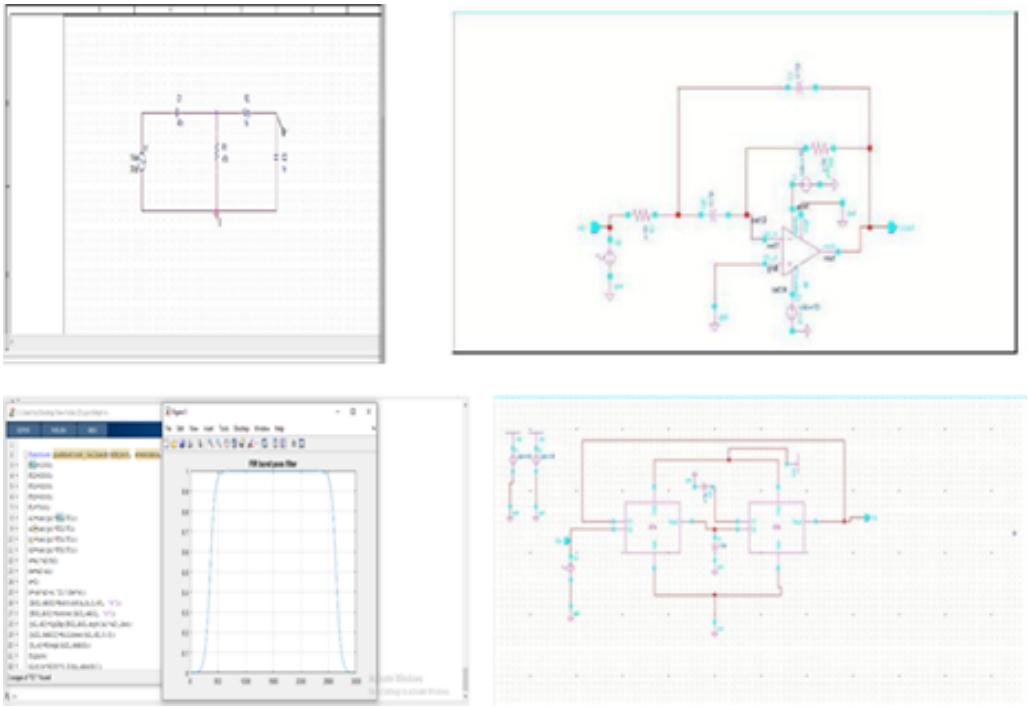

Fig 8. Proposed schematic of BPF Circuit using OTA

The transfer function of the BPF can be written as:

$$\frac{jw\,(w_o/Q)}{(jw)^2 + jw\,(w_o/Q) + w_0^2}$$

the response of the BPF by using the various tools can be shown as:

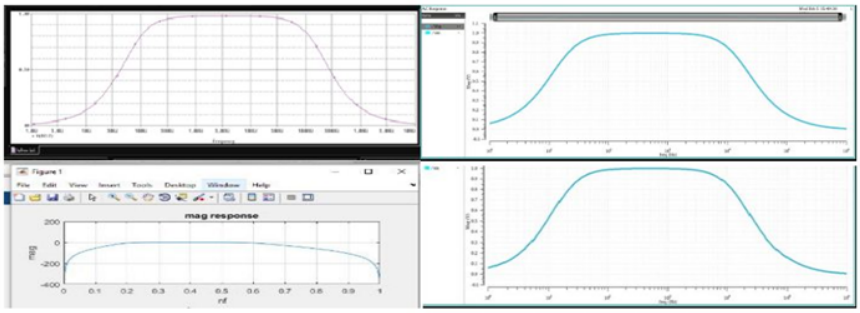

Fig 9. Proposed response of BPF Circuit using OTA

2.1 Comparison of biquad filter using different tools

The designing of KHN Biquad filter using different tools has been done and the waveform of KHN Biquad filter has been generated using ORCAD tool, CADENCE tool, Xilinx 14.7 tool and Matlab tool[9]. The comparison between the various tools has been simulated.

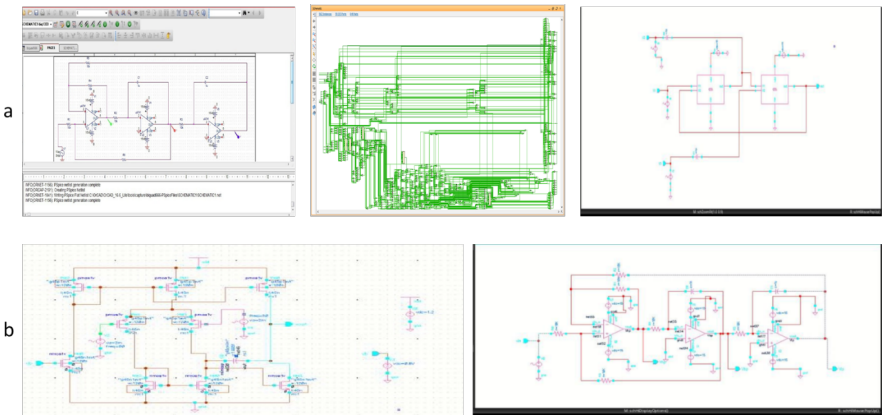

Fig 10. Proposed schematic ofBiquad Filter Circuit using OTA (operational transconductance amplifier), (b): Proposed schematic of Biquad Filter Circuit using OTA (operational transconductance amplifier)

2.2 Comparison of biquad filter using different tools

The designing of Biquad filter using different tools has been done and the waveform of Biquad filter has been generated using ORCAD tool, CADENCE tool, Xilinx 14.7 tool and Matlab tool[12]. The comparison between the various tools has been simulated.

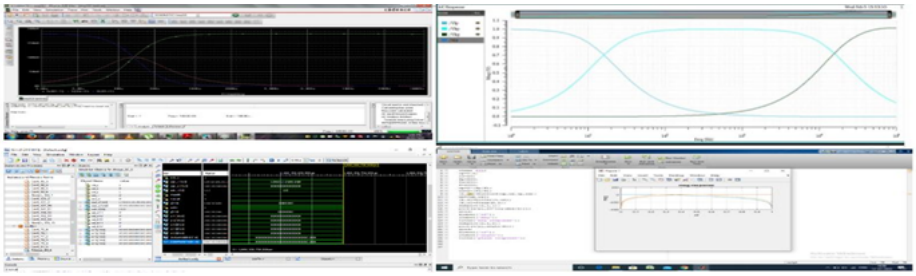

Fig 11. Proposed response of Biquad Filter using OTA (operational transconductance amplifier)

3 Simulation and Results

The propose circuit are validate using Cadence Virtuoso tool with gpdk 0.18μm technology, ORCAD tool and XILINX tool[8–13]. The analysis is taken on the basis of power with the three tools CADENCE, ORCAD and XILINX tool and with the help of XILINX tool layout of the proposed Biquad filter is also being prepared. In the figure (10) schematic of the propose Biquad using OTA circuit are represented using three different tools. In the figure (11) waveform of propose Biquad circuit shown with the variation of input supply. Inverter pMOS and nMOS are define with proper W/L ratio so that it provides best output with full swing. But when we are using in the CADENCE virtuoso tool OTA circuit it provides less static power dissipation as compare to other tool circuit use.

Table 1. Comparison of various parameters using ORCAD, CADENCE and XILINX tool

Parameter name	Using ORCAD	Using CADENCE VIRTUOSO	Using Xilinx
Power	150mW	300μW	177mW
Supply Voltage	2.5V	2.5V	2.5V
Bias Current	50μA	50μA	50μA
Load Capacitor	10pF	10pF	10pF
Gain	36.747db	70.37db	39.747db
Slew Rate	12.5V/μs	46.97V/μs	22.5V/μs

Table 2. Comparison of various parameters of Proposed OTA circuit using CADENCE tool

Parameter	OTA Circuit in Literature [1]	Proposed OTA Circuit (180nm)	Proposed OTA Circuit (90nm)
Technology used for implementation	180nmtechnology	180nmtechnology	90nmtechnology
No of Transistors	24	11	9
PMOS (W/L)	2160n/65n	1800n/65n	1200n/65n
NMOS (W/L)	720n/65n	600n/65n	300n/65n
Resistance	8	5	3
Capacitance	5	2	2
Layout Area	665µm×184µm	268µm×118.9µm	150µm×108µm
Gain	36.74db	70.37db	72db
Slew Rate	12.5V/µs	46.97V/µs	66V/µs
Power Dissipation	534µW	330 µW	270 µW

3.1 Power calculation using various tools

The power of Biquad filter has been calculated with the help of various tools ORCAD, CADENCE and XILINX FPGA tool.

Fig 12. Comparison of power calculation with three different tool, (b): Comparison of power calculation with three different tool

In the figure (12) comparison of power calculation using the ORCAD, CADENCE and XILINX tool is presented. Itis evident that power comes under the CADENCE virtuoso tool is less as compared to the other two tool and making the layout of the proposed Biquad Filter the XILINX tool is being used.

3.2 Clock variation report

The proposed circuit values under the clock variation have been shown. It basically shows the entire source rise time and the fall time of the given circuit.

```
Clock to Setup on destination clock dspclk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk_i          |    5.518|         |         |         |
dspclk         |    5.025|         |         |         |
---------------+---------+---------+---------+---------+
```

Fig 13. Clock variation report

3.3 Proposed circuit design summary report

The proposed circuit design summary report has been shown. It basically shows how many flip flops, clock buffers and IO buffers are present in the circuit while designing.

```
*                            Design Summary
=====================================================================

Top Level Output File Name         : bqmain.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 302
#      GND                         : 1
#      INV                         : 11
#      LUT1                        : 1
#      LUT2                        : 5
#      LUT3                        : 30
#      LUT4                        : 62
#      LUT5                        : 37
#      LUT6                        : 33
#      MUXCY                       : 59
#      VCC                         : 1
#      XORCY                       : 62
# FlipFlops/Latches                : 198
#      FDCE                        : 198
# Clock Buffers                    : 2
#      BUFGP                       : 2
# IO Buffers                       : 57
#      IBUF                        : 32
#      OBUF                        : 25
# DSPs                             : 5
#      DSP48E1                     : 5
```

Fig 14. Proposed circuit design summary report

3.4 Proposed circuit HDL synthesis report

The proposed circuit HDL synthesis report has been shown. It basically shows how many registers, adders and multiplexers are present in the circuit while designing.

```
=========================================================================
HDL Synthesis Report

Macro Statistics
# Multipliers                                          : 5
 11x7-bit multiplier                                   : 2
 7x7-bit multiplier                                    : 3
# Adders/Subtractors                                   : 12
 14-bit addsub                                         : 4
 32-bit adder                                          : 8
# Registers                                            : 17
 12-bit register                                       : 1
 14-bit register                                       : 4
 16-bit register                                       : 5
 8-bit register                                        : 7
# Multiplexers                                         : 16
 1-bit 2-to-1 multiplexer                              : 7
 14-bit 2-to-1 multiplexer                             : 1
 16-bit 7-to-1 multiplexer                             : 1
 32-bit 2-to-1 multiplexer                             : 6
 8-bit 2-to-1 multiplexer                              : 1
# Xors                                                 : 5
 1-bit xor2                                            : 5
```

Fig 15. Proposed Circuit HDL Synthesis report

3.5 Proposed circuit timing and delay report

The proposed circuit timing analysis report has been shown. It basically shows the clock period of 5.027ns and the total number of paths and ports in the circuit while designing.

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.027ns (Maximum Frequency: 198.938MHz)
   Minimum input arrival time before clock: 1.194ns
   Maximum output required time after clock: 1.605ns
   Maximum combinational path delay: 1.479ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'dspclk'
  Clock period: 5.027ns (frequency: 198.938MHz)
  Total number of paths / destination ports: 20863 / 110
```

Fig 16. Timing and delay report

3.6 Proposed circuit fan in fanout report

The proposed circuit fan in fanout analysis has been shown. It basically shows all the signal rate and the slice fanout of the given circuit.

Name	Power (W)	Signal Rate	% High	Fanout	Slice Fanout	Clock
biquadi/nreset_inv	0.00000	0.0	1.0	118	33	Async
nreset_IBUF	0.00000	0.0	99.0	1	1	Async
rst_i_IBUF	0.00000	0.0	1.0	80	20	Async

Fig 17. Proposed circuit fan infanout report

3.7 Proposed circuit toggle rate report

The proposed circuit toggle rate analysis has been shown. It basically shows all the toggle rate and the reset toggle values of the given circuit.

Name	Value	Range
FF Toggle Rate (%)	12.5	0.0 to 200.0
I/O Toggle Rate (%)	12.5	0.0 to 200.0
Output Load (pF)	5.0	0.0 to 1000000.0
I/O Enable Rate (%)	100.0	0.0 to 100.0
BRAM Write Rate (%)	50.0	0.0 to 100.0
BRAM Enable Rate (%)	50.0	0.0 to 100.0
Set/Reset Probability (%)	1.0	0.0 to 100.0
Set/Reset Toggle Rate (%)	1.0	0.0 to 200.0
Enable Probability (%)	99.0	0.0 to 100.0
Enable Toggle Rate (%)	1.0	0.0 to 200.0
DSP Toggle Rate (%)	12.5	0.0 to 200.0

Fig 18. Proposed circuit toggle rate analysis report

3.8 Proposed circuit layout diagram

The proposed circuit Biquad filter zoomed layout diagram has been shown. It basically shows all connections of the layout of the given circuit.

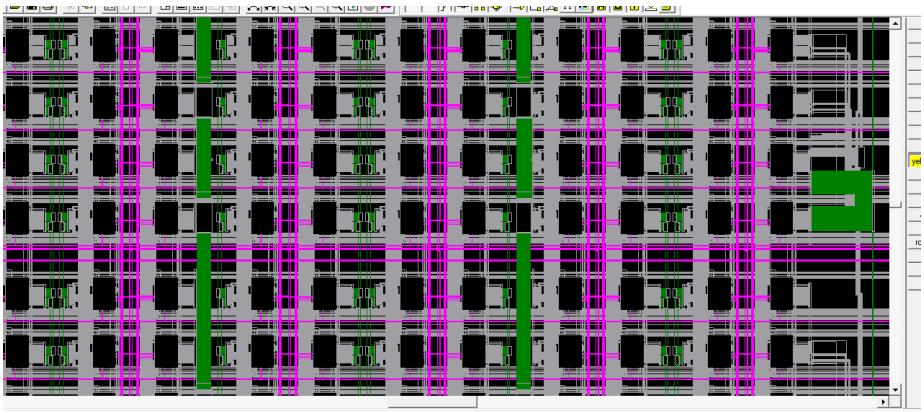

Fig 19. Layout of proposed Biquad circuit using OTA

4 Conclusions

In this study OTA based filter and its performance has been analyzed using the four different simulation tools (CADENCE Virtuoso, ORCAD, XILINX and MATLAB tool). After designing the OTA circuit, the performance of the OTA based Biquad filter has been analyzed on the ground on power, gain and slew rate. After implementing and analyzing all the filter results in the circuit, it has been observed that power has reduced to 300microwatt in CADENCE which is a lot less that of 150milliwatt using ORCAD tool and 177milliwatt using the XILINX tool. The maximum gain is 70.37DB which is observed using CADENCE virtuoso tool which is increased as 34% with respect to ORCAD and 37% with respect to Xilinx tool. The Slew rate is 46.97V/μs by using the CADENCE virtuoso tool. By analyzing the other parameters, CADENCE is found to be the best tool to design the Biquad filter circuit. One of the key design parameters for any filter is its efficiency. This can be particularly important for battery power equipment where battery life is of importance.The efficiency of the amplifier is essentially the output power divided by the input power.Normally the input power is taken to be the DC power applied to supply the filter.

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