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RESEARCH ARTICLE

Minimization of power and area of digital modulator for cellular communication using cadence in 180nm, 90nm and 45nm CMOS technology

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Abstract

Background/Objectives: Low power modulators are most efficient for wireless communication. Quadrature Amplitude Modulation (QAM) is used widely for high data rate communication than BPSK and QPSK, since it carries more bits of information per symbol over the channel. The objective of this work is to minimize the power consumption and area utilization of 32-bit QAM modulator. **Methods/Statistical analysis:** In this work, three new procedures are introduced for 32QAM modulator. In the first approach, sine and cosine data generated using conventional technique are stored in ROM and the stored data is selected based on the input sequence to generate the output signal. This approach reduces the power consumption and area utilization. In the second approach, information bit stream is modulated with sine and cosine waves generated by iterative algorithm to minimize power and area requirement. In the third approach, booth multiplication algorithm is employed to generate QAM signal. This method of generating QAM signal consumes less power and area in comparison with the conventional modulator. The work is synthesized, analyzed, and compared in 180nm, 90nm and 45nm CMOS technology using Cadence software. **Findings**: In 180nm CMOS technology power consumption noticed is 60662.740nW, 617020.071nW and 133679.687nW with the proposed method1, method2 and method3 respectively. An Area utilized in 180nm CMOS technology is 1341μm2, 20746.757μm2, and 2754μm2 respectively in proposed 32QAM modulator with ROM, 32QAM modulator with proposed Iterative algorithm and 32QAM modulator with Booth multiplication algorithm. **Novelty/Applications:** The conventional 32QAM devours additional power and area. In this work area and power reduction is achieved with respect to the conventional method. The same work is carried out with 90nm and 45nm CMOS technology. Three novel approaches to 32QAM are proposed. The proposed work is synthesized, analyzed, tabulated and compared with conventional method and shown that power consumption and area utilization are minimum than compared to the conventional method.

Keywords: QAM; multiplier; power; area; communication; cadence

1 Introduction

Wireless networks are rapidly developing as an imperative advancement and turning in to a fundamental segment of contemporary day by day life. Digital modulation is used in numerous applications. Mobile radio communication has become an essential part of everyone's life. In order to increase the battery life of this electronic gadgets, the power and area reduction to be achieved through new techniques. Hence low power digital modulators are in demand.

Quadrature Amplitude Modulation (QAM) allows some considerable gains for the data transmission. As 16QAM transitions to 32QAM, 64QAM, 256QAM and onwards, more eminent information pace could be attainable by the side of the deprivation of noise margin. QPSK and QAM techniques are used to increase the capability and speed of wireless networks. Analog QAM is the combination of AM and PM. Digital QAM is the combination of ASK and PSK. In QAM modulation both amplitude and phase are modulated. The higher order of modulation permits to empower more bits/symbol. Information rate adaptability is maintained between channel considerations and modulation rate. If good signal to noise ratio is attainable, then higher order modulation is employed to achieve higher data rate at higher speed. In case of channel conditions are not meeting the appropriate signal to noise level, and then low information rate can be adaptable to ascertain low error rates [1–4]. QAM can be employed in various mobile radio and quality information delivery appliances. Direct to home (DTH), cable television applications transmit more information signals over the channel. This kind of application utilizes higher order modulation such as 64QAM and 256 QAM. Even though higher order modulators are proficient to provide high speed information signal pace and these are perceptibly minimum reluctant to distortion. [5–8].

The typical QPSK modulator demands Frequency synthesizer (DDS), adders, and multipliers to generate sine waveform. It requires adders, multipliers to generate a symbol with respect to input bit streams. As low power modulators are in demand for satellite and mobile radio networks, in this work, implantable QPSK modulator is developed, which requires less power for operation. The work is based on generating a symbol using data storage inside a memory block consorting to the incoming information streams. The work is modeled with Verilog hardware description language and Xilinx ISE [9,10]. Low power wide area networks problems are solved through innovative applications developed in recent years, In this work turbo Frequency shift keying is implemented, this FSK outputs the constant envelope waveform [11–13]. In the fourth generation networks, orthogonal frequency division multiplexing employed with Turbo-Frequency shift keying to obtain the constant envelope of the output signal. This improves the performance by minimizing error rate [14].

2 Proposed Methods

Three new approaches are projected to 32 bit QAM modulator to achieve low power consumption and area reduction.

- **Proposed 32QAM modulator with Memory**
- **32QAM modulator with proposed iterative algorithm:** A new iterative algorithm is proposed to produce digital sine and cosine signals. This new approach for 32bit QAM digital modulator reduces the area and power consumption.
- **32QAM modulator with Booth multiplication algorithm**: A new approach is introduced for 32QAM modulators. In this work, the analog multiplication using product multiplier is replaced through the Booth multiplier. This results in reduction in area, gate utilization and minimizes the power consumption. The proposed work performance parameters such as area and power are compared with the existing work.

2.1 Proposed 32QAM with Memory

The conventional 32QAM modulator is shown in Figure 1. The three input bits in I-arm and two input bits in Q-arm are multiplied with the sine and cosine streams respectively. The multiplier output is added together to generate 32-QAM output.

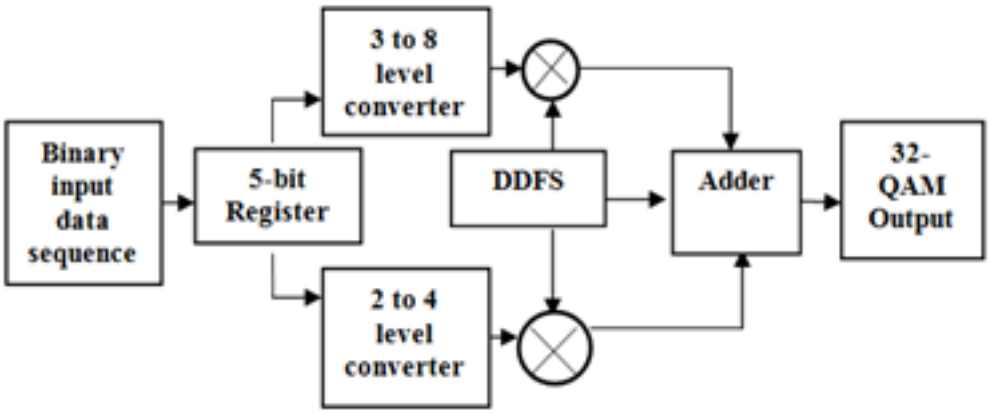

Fig 1. Conventional 32QAM

The sine and cosine data generated out of conventional method are stored in ROM as shown in Figure 2. The stored phase data is selected accordingly with the input bit streams.

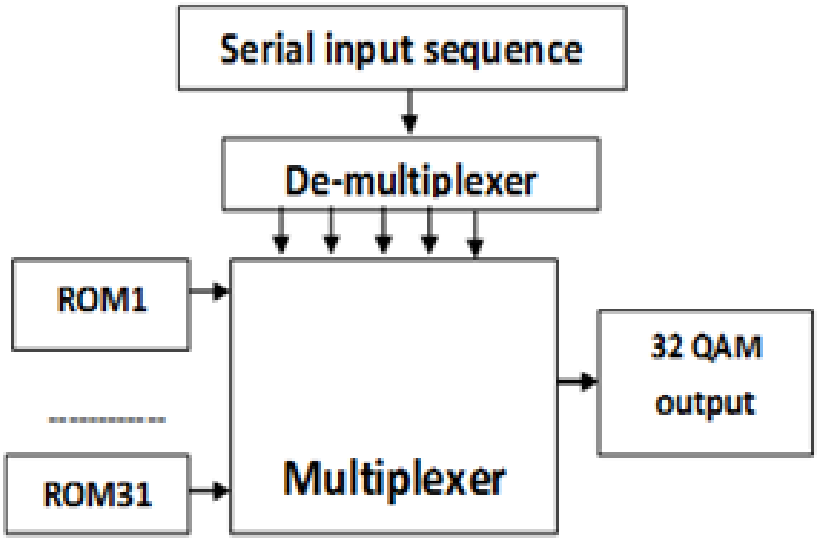

Fig 2. Proposed QAM with ROM

The intended 32QAM modulator-3 is designated in Figure 3 below. It comprises of 6-bit register to store information bits, a register to store 6-bit address, a register to store control bits, multiplexer and adder. The real and imaginary data generated and added up to obtain digital 32QAM output.

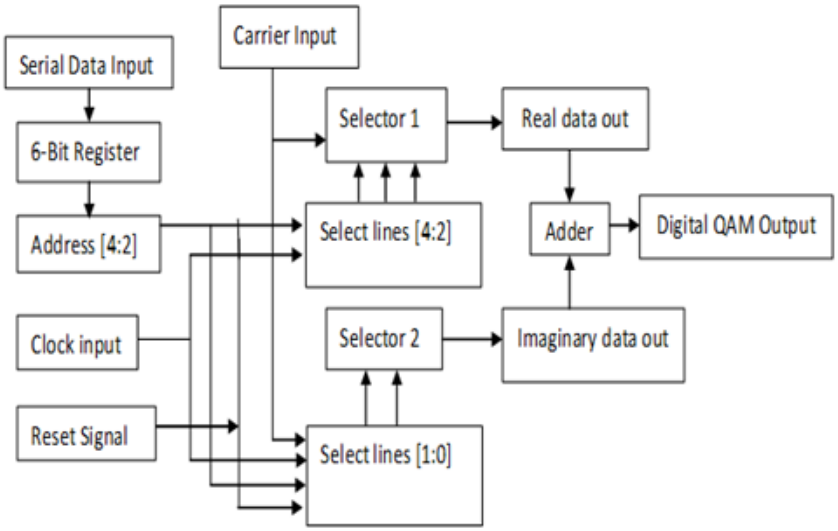

Fig 3. 32QAM with selector

2.2 32QAM with Proposed Iterative Algorithm

The flow chart shows the steps to generate sine and cosine using proposed algorithm as shown in Figure 4. Initially sine and cosine registers are declared and an initial data is stored in these registers. After satisfying the applied input conditions, the sine and cosine values are calculated as shown in Equation (1). The computed values are stored in sine_reg and cos_reg. The generated sine and cosine values are applied to the modulator block. An iterative algorithm is employed to generate digital sine and cosine signals as depicted below in Figure 4 and its

implantation is shown in Figure 5.

$$\begin{aligned} \text{sine} &= \text{sine\_reg} + \{\text{cos\_reg}[n], \text{cos\_reg}[n], \text{cos\_reg}[n], \text{cos\_reg}[n:m]\} \\ \text{cos} &= \text{cos\_reg} - \{\text{sine}[n], \text{sine}[n], \text{sine}[n], \text{sine}[n:m]\} \end{aligned} \quad (1)$$

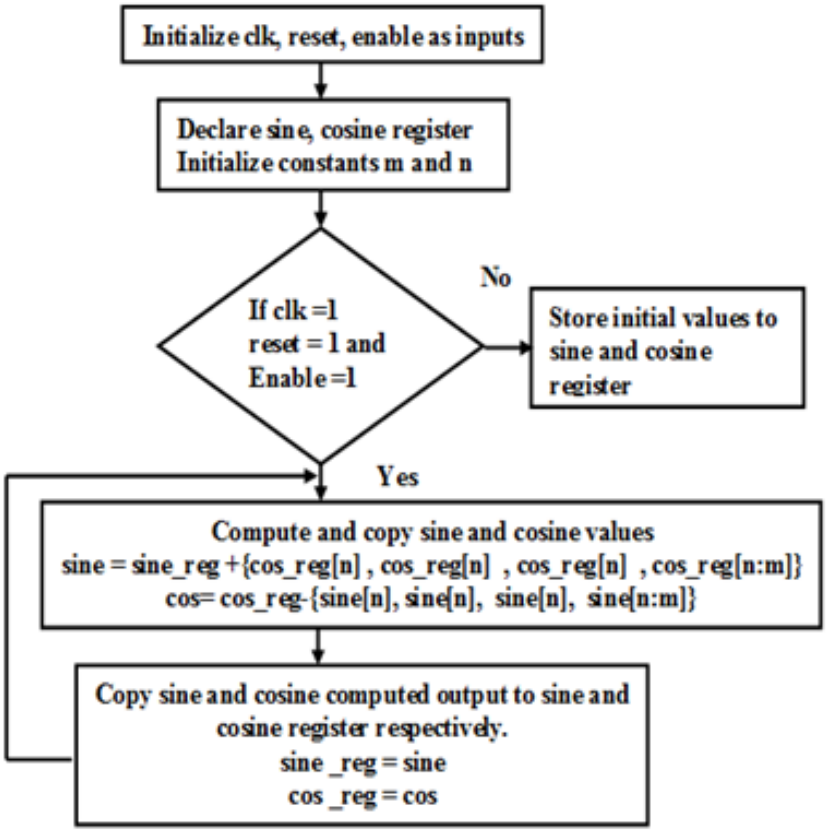

Fig 4. Flowchart indicating the computation of sine and cosine of 32QAM

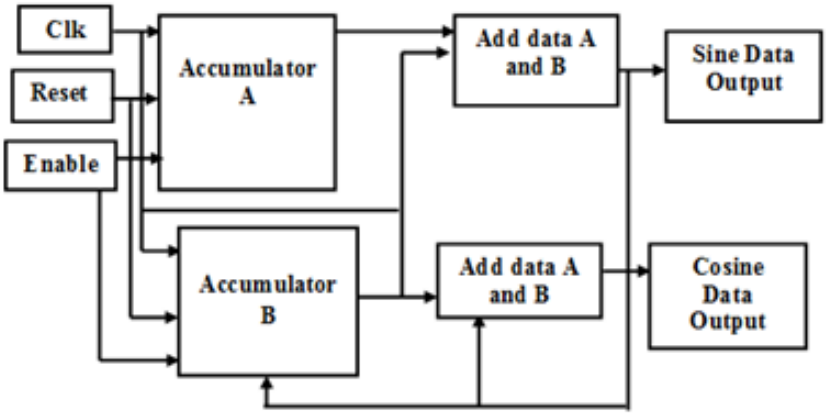

Fig 5. Implementation of 32QAM with iterative algorithm

2.3. 32QAM with Proposed Iterative Algorithm

The flow chart is shown in Figure 6. Low power multipliers are highly demanded today. Most of the digital signal processing applications is based on arithmetic operations. They require high speed and low power multipliers. In this work, multiplication is carried out by using Booth multiplication, which in turn reduces the area and power in comparison with the typical design of 32bit qudrature amplitude modulator. The total power consumption is summation of static power and the dynamic power consumption. The significant power utilization is the dynamic power. While doing arithmetic operations, the power utilization primarily relied on the repetitive operations performed.

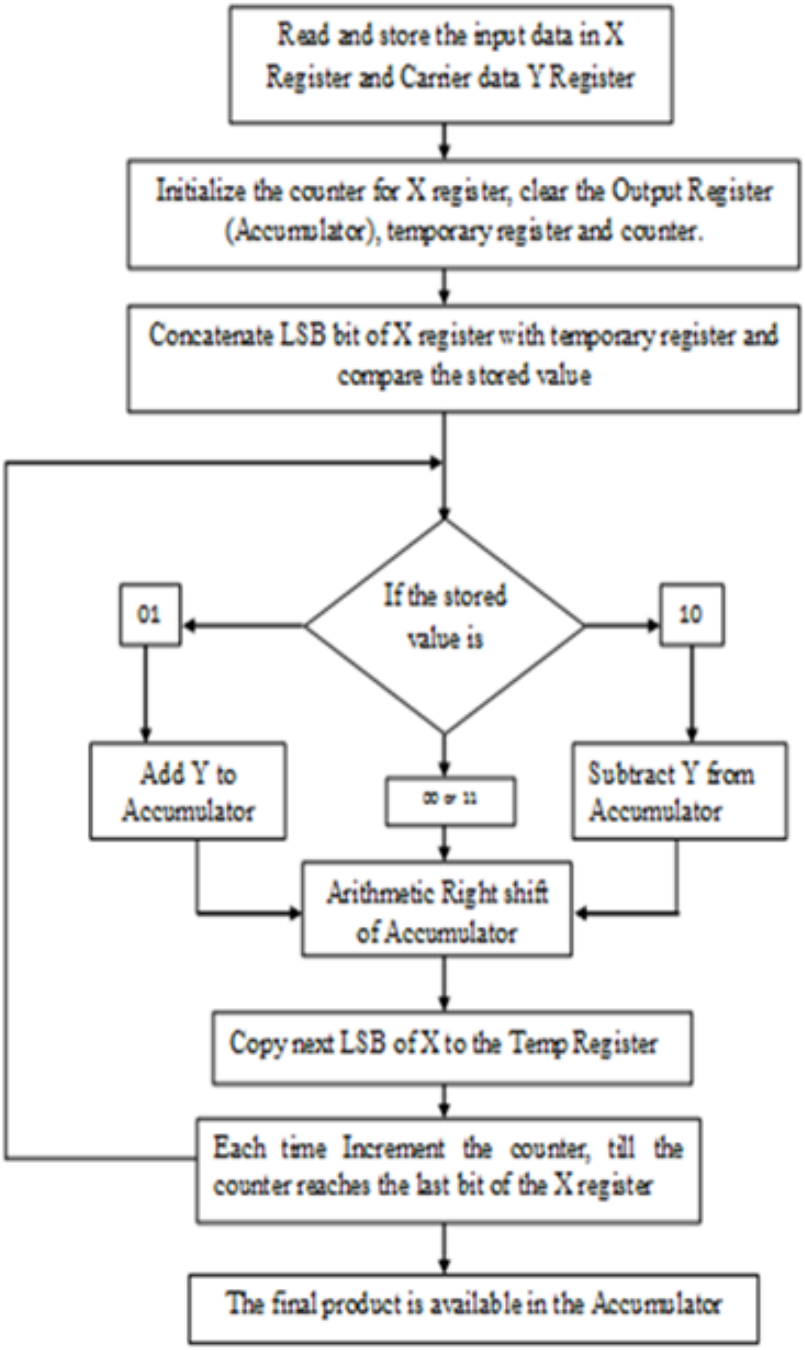

Fig 6. Flowchart representing Booth multiplication algorithm

In case of multiplication, power can be minimized through reducing the number of mathematical process. Numerous form of multipliers

are "Booth multiplier, combinational multiplier, Wallace tree Multiplier, array multiplier and sequential multiplier". The input message signal stream is renewed in to parallel data streams. This is stored multiplicand register. The carrier bit streams are stored in the multiplier register. The booth algorithm performs the signed multiplication of multiplicand and the multiplier.

The "Booth algorithm" is employed to product two signed numbers. The signed numbers are in two's complement format. The binary information stream is converted into parallel bits of data. This data is the multiplicand and the multiplier are the digitized carrier signal. This multiplier is advantageous in terms of speed. If the transition bit and LSB of the input data is 10 and 01 then carrier data is subtracted and added to the product register, then arithmetic right shift is performed. If the transition bit and LSB of the input data is 00 or 11 then only arithmetic right shift is performed on product register. The counter is incremented each time till the input data stream reaches its maximum count. The implementation of 32QAM with multiplication method is represented in Figure 7.

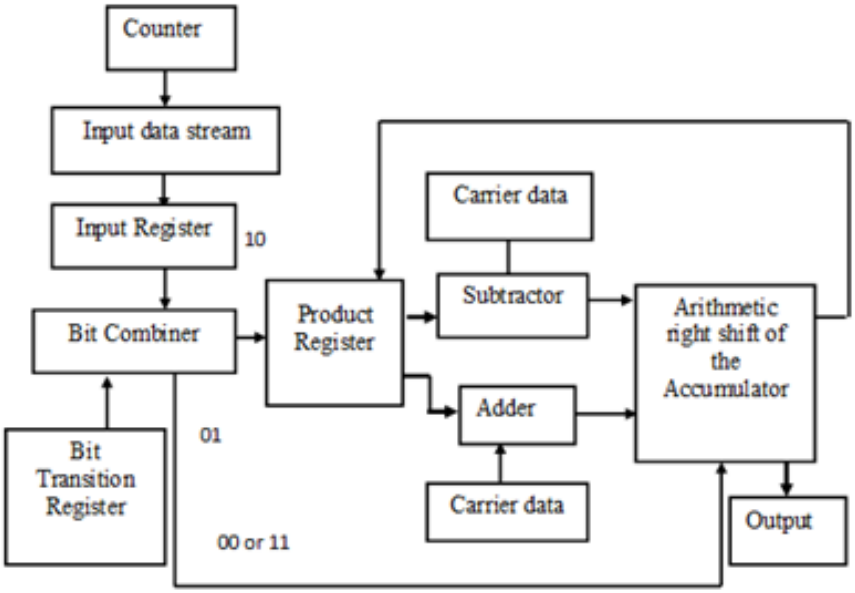

Fig 7. Implementation of 32QAM using Booth multiplication algorithm

3 Results and Discussion

The results of 32QAM modulators are compared. The analysis with respect to power and area utilization is carried out using Cadence software.

3.1. Proposed 32QAM with memory

Table 1 detail about leakage and dynamic power. The total power is the summation of dynamic and leakage power.

Table 1. Power and Area Report of 32QAM with Memory in 180nm, 90nm and 45nm Technology

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total Area (μm^2)
180nm	40	41.97	60620.768	60662.740	1341
90nm	43	2314.9	13344.346	15659.278	419
45nm	47	76.66	3871.279	3943.94	125

The total power in nW and area in μm2 is represented in 180nm, 90nm and 45nm technology respectively. The total area utilized for this design is 1341μm2, 419μm2 and 125μm2 and the total power consumption is 60662.740nW, 15659.278nW and 3943.94nW in 180nm, 90nm and 45nm CMOS technology respectively.

3.2 Power and area analysis of 32QAM with iterative algorithm

The result of 32QAM modulator with iterative algorithm detailed in Table 2 below. Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 is used for simulation and synthesis. The total power in nW and area in μm2 in 180nm, 90nm and 45nm technology is 617020.071nW, 156727.033nW and 14905.582nW and total area is 20746.757μm2, 6341μm2 and 966μm2 respectively.

Table 2. Power and area report of 32QAM with proposed iterative algorithm in 180nm, 90nm and 45nm technology

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total (nW)	Area
180nm	563	831.986	616188	617020.07	20746	
csa_tree_a	65	210.056	143463.7	143673.81	4131	
csa_tree_mul_99_15	77	76.614	33155.32	33231.935	1790	
final_adde..ux_	50	62.864	35925.44	35988.305	1467	
final_adde..ux_	50	62.864	27679.75	27742.617	1454	
csa_tree_mul_101_15	66	60.745	6498.094	6558.839	1454	
sub_27_26	20	25.105	6466.940	6492.045	582	
csa_mux_a_mux_	34	25.012	20392.77	20417.786	575	
csa_mux_a_mux_	36	23.976	22059.14	22083.117	539	
add_25_26	22	20.857	11340.97	11361.828	532	
csa_mux_a_mux_	34	25.012	20392.77	20417.786	575	
csa_mux_a_mux_	36	23.976	22059.14	22083.117	539	
add_25_26	22	20.857	11340.97	11361.828	532	
csa_mux_b_mux_	11	5.932	6145.343	6151.275	146	
csa_mux_b_mux_	11	5.932	1640.546	1646.478	146	
90nm						
csa_tree_a	624	33146.4	123580.5	156727.0	6341	
csa_tree_mul_99_15	75	6208.64	21910.91	28119.55	1270	
csa_tree_mul_101_15	82	2437.32	5330.687	7768.012	548	
final_adde..ux_iRES_	79	2287.54	946.266	3233.810	458	
final_adde..ux_qRES_	69	1873.82	3814.582	5688.398	446	
csa_mux_a	69	1873.82	3008.073	4881.889	446	
csa_mux_a	32	982.680	5160.882	6143.562	173	
csa_mux_a	32	945.122	4696.514	5641.636	170	
add_25_26	25	740.957	1688.024	2428.981	163	
sub_27_26	18	706.540	2092.739	2799.279	157	
csa_mux	11	298.882	1703.732	2002.614	50	
csa_mux_b	11	298.882	456.444	755.326	50	
45nm						
qam32_cor	568	543.895	14361.687	14905.582	966	
mul_99_15	181	121.847	3293.702	3415.549	218	
mul_99_15	130	92.242	407.290	499.532	160	
sub_27_26	48	23.394	454.866	478.260	45	
add_25_26	37	21.483	544.572	566.055	43	

3.3 Power and area analysis of 32QAM with Booth multiplication algorithm

The 32QAM with proposed method-3 is shown in Table 3 below. The total power consumed is 133679.687nW, 85601.465nW, 6452.911nW and the total area utilized is 2754μm^2, 3075μm^2 and 214μm^2 in 180nm, 90nm and 45nm technology respectively.

Table 3. Power and area report of 32QAM using Booth algorithm in 180nm, 90nm and 45nm Technology

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total Area (nW)
180nm	196	66.270	133613.4	133679.6	2754
90nm	367	5647.3	79954.16	85601.46	3075
mux_output	10	541.825	4623.57	5165.39	252
minus_69_28	42	494.837	6060.497	6555.334	229
add_47_58_I5	33	386.256	6803.298	7189.554	229
add_49_58_I5	33	386.256	5430.852	5817.108	229
add_47_58_I4	33	386.256	6232.807	6619.063	229
add_49_58_I4	33	386.256	5481.578	5867.833	229
add_47_58_I3	33	386.256	5297.709	5683.964	229
add_49_58_I3	33	386.256	4457.876	4844.132	229
add_47_58_I2	33	386.256	4303.839	4690.095	229
add_49_58_I2	33	386.256	3018.781	3405.037	229

Continued on next page

Table 3 continued

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total Area (nW)
mux_output	5	255.937	3749.530	4005.467	153
mux_output	5	255.937	4990.730	5246.668	153
mux_output	5	255.937	5548.394	5804.331	153
minus_41	5	255.937	5387.226	5643.163	153
minus_41_16	18	227.437	3192.387	3419.824	107
mux_output	5	194.058	1460.784	1654.841	76
45nm					
qam32_45	212	117.715	6335.195	6452.911	214

4 Comparison and analysis of all proposed methods

The power and area report of all the three new approaches to 32QAM modulators are discussed compared and analyzed in 180nm, 90nm and 45nm CMOS technology using Cadence tool. The power and area reports are discussed below in Tables 4 and 5 respectively.

4.1 Power utilization report

The power consumed in all methods are compared and reported in Table 4 and the bar graph representation is depicted in Figure 8 below.

Table 4. Power Utilization of all proposed 32QAM in 180nm, 90nm and 45nm technology

Technology	32QAM with Memory	32QAM with Iterative algorithm	32QAM with Booth Multiplier
180nm	60662.740	617020.071	133679.687
90nm	15659.278	156727.033	85601.465
45nm	3943.94	14905.582	6452.911

As depicted in the figure below, the first approach consumes 60662.740nW, the second approach with iterative algorithm consumes 617020.071nW and the third proposed approach with Booth algorithm consumes 133679.687nW in 180nm technology. The power consumed in method1 in 90nm technology in 32QAM modulator with memory is 15659.278nW; with iterative algorithm is 156727.033nW and proposed 32QAM with method-3 is 85601.465nW respectively.

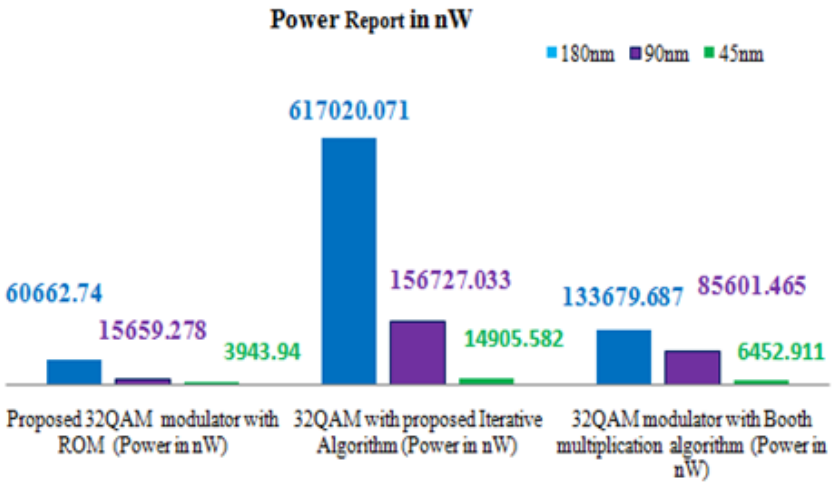

Fig 8. Power comparison report

In 45nm CMOS Technology, the first approach consumes 3943.94nW, second approach with iterative algorithm consumes 14905.582nW and the third proposed approach with Booth algorithm consumes 6452.911nW.

4.2 Area utilization Report

An area utilization and comparison is carried out using cadence synthesis tool in 180nm, 90nm and 45nm technology is reported below in Table 5. The area utilized in 180nm technology in method1, method2 and method3 is 1341μm^2, 20746.757μm^2, and 2754μm^2 respectively.

The area utilized in 90nm technology in method1, method2 and method3 is 419μm^2, 6341μm^2 and 3075μm^2 respectively. The area utilized in 45nm technology in method1, method2 and method3 is 125μm^2, 966μm^2, and 214μm^2 respectively.

Table 5. Area utilization in μm2 of all proposed 32QAM in 180nm, 90nm and 45nm technology

Technology	32QAM with Memory	32QAM with Iterative algorithm	32QAM with Booth Multiplier
180nm	1341	20746.757	2754
90nm	419	6341	3075
45nm	125	966	214

Table 5 is depicted with bar graph in Figure 9 below. The area utilized for 32QAM with iterative algorithm is maximum than the other two approaches. The proposed modulator-1 utilizes minimum area among other proposed methods.

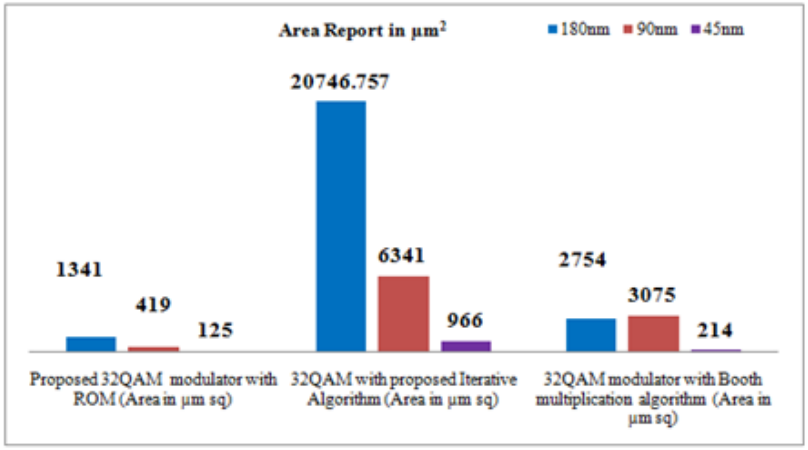

Fig 9. Area comparison report

The area comparison report of all the three proposed 32QAM modulators in 180nm, 90nm and 45nm technology is represented in above figure.

5 Conclusion

In this study, new three approaches are discussed for 32QAM modulator. Area utilization and power consumption report is generated using cadence synthesis tool in 180nm, 90nm and 45nm technology. The proposed techniques for 32QAM system achieves effective concert in terms of area and power comparatively with typical way of designing 32QAM system with Direct Digital Frequency Synthesizer (DDFS). The proposed 32QAM modulator-1 consumes minimum power and utilizes minimum area compared with other proposed methods. The results are tabulated, analyzed and compared. The power consumption is much reduced in the proposed method in comparison with the existing work. The work is carried out in 180nm, 90nm and 45nm CMOS technology. The three novel approaches proposed in this work minimizes the power consumption and area utilization of 32QAM than compared to the conventional method. As the technology scales downs the area and power parameters are further minimized.

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