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Design of Efficient Low Power Flash ADC Using TIQ in 45 nm Technology

Dr. Ayyavoo Mithila*, A. Lavanya, A.R. Nithyashree and T.R. Mithra

Department of ECE, Sri Krishna College of Technology, Coimbatore, India; mithila6@gmail.com, lavanyaanjee@gmail.com, ar.nithyashreeeceskct@gmail.com, t.r.mithraeceskct@gmail.com

Abstract

Objective: To design and implement flash ADC for high speed operation thereby to minimise the power consumption and improve the performance efficiency. **Methods:** At present, there exists a variety of Analog-to-Digital Converter (ADC) with different architecture, sampling rates, resolutions, temperature ranges, and power consumption. The existing ADCs used in various multiple applications which include mobile communication hardware to measuring instruments. Therefore, their significant performance and working of ADCs are determined by its architecture, the commonly existing ADC design is not suitable for all applications. In order to meet the high speed operation scenario, a Flash type ADC model is proposed. **Findings:** Resistor ladder would be commonly used in all type of ADC circuits, but downside it consume maximum area and power. In all existing methods, the average power consumption of Flash ADC is found to be higher when compared with our methodology. This can be overcome by using threshold inverting quantization (TIQ) comparator for low power operation. **Improvements:** An efficient thermometer to the binary code converter is targeted for 45 nm CMOS technology that has been proposed and implemented Flash CMOS ADC Design using the CADENCE VIRTUOSO Tool. The optimal power analysis has been carried out to prove the design absolutely a low power model.

Keywords: Flash ADC, Low Power, CMOS Technology, TIQ Comparator, CADENCE VIRTUOSO

1. Introduction

In our day-to-day life, most of our needs have been encountered by two kinds of electronic systems – analog and digital system. Present technologies and devices are digital systems but generally the source signal in nature is in analog form. In very large-scale integration (VLSI) world, for designing integrated circuits (ICs) the key component used is Analog-to-Digital converter (ADC) which act as an interfacing bridge to process the available analog signal.[1] There exists many types of ADC like Sigma delta ADC, successive approximation ADC, flash ADC, dual slope ADC which is preferred for different applications. Among them, Flash ADC has high operating speed and widely utilised for high speed data instrumentation, optical communication, wideband radar and the recent advent of Wireless Personal Area Network (WPAN) which necessarily requires extremely fast transmission of data that operates in low power mode.[2,3] Conventional flash ADC with resistive ladder structure consumes more area as it divides design, but it has extreme negative exertion in advent with large area and consuming high power. The required performance characteristics can be obtained by replacing conventional comparator with threshold inverting quantization (TIQ) comparator. Here, we propose to design less power consuming flash ADC in 45 nm technology using TIQ comparator. When compared to other ADC components, Flash ADC is ultimately used for their high speed operation. They are usually accurate over a period of technology growth. Unlike conventional comparator, TIQ comparator produces thermometer code that compares the internal switching voltage and input signal. By reducing the usage of high power consumption components, the proposed design is made to operate efficiently as a low power model.

**Author for correspondence*

2. Flash ADC and its Components

Flash ADC which can be called as parallel ADC is one among the fastest of all available ADC. Those ADCs can be categorised by their relevant usage of different type of comparators.[4] The analog signal processed by the comparators produces thermometer code as the output. If Resistor ladder logic is embedded on the chip it results in the downside effect of more area and power consumption. To overcome this, we use TIQ comparators that will make use of reference voltage internally. Usage of such impeccable comparator provides a thermometer code which is fed to an encoder that in turn converts into binary codes.[5] The conventional N bit Flash ADC is figured out in Figure 1.[6]

2.1. Comparator

Two inverters are cascaded which forms the basic structure of TIQ technique. Among the two inverters, one acts as switching regulator which produces pulsed voltage and the second acts as a signal strengthener. The TIQ comparator works same as that of voltage comparator by comparing given analog input with internal switching voltage.[7] The TIQ comparator's output is explained in terms of digital system with the help of binary bits "0" and "1" (i.e.) if given sinusoidal input value is higher than the switching voltages then comparators output will be represented as "1" logic or high and if the given analog input value smaller than the internal switching voltages then comparators output results as "0" logic or low output. For 4-bit flash ADC, the number of TIQ used is 15 which are arranged in parallel manner is fed as an input to encoder design. The cascaded inverters produce different switching voltages for different CMOS nanometer technology and internally reference voltage can be generated by varying the channel width of the transistor by maintaining its length value unchanged. TIQ comparator is shown in Figure 2.

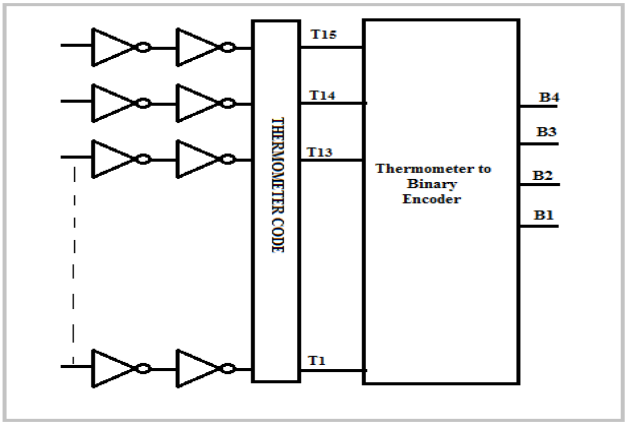

Figure 1. Block diagram of our flash ADC model.

2.2. Encoder

The thermometer code which is the response value of TIQ comparator has now fed to Encoder named as thermometer to binary encoder. There are several methods available[8–10] for designing the encoder. Of all the encoding styles, the multiplier based encoder design is considered as most efficient design as it consumes less power. So encoder is designed using 2 × 1 Multiplexer (MUX) as shown in Figure 3.

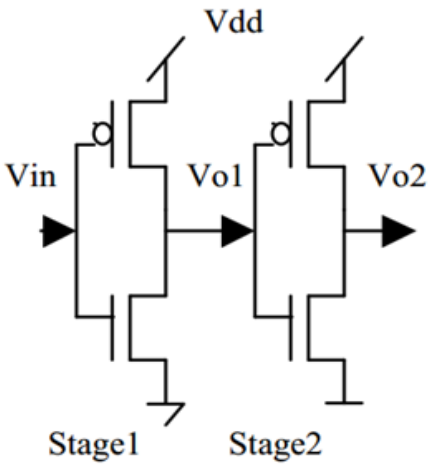

Figure 2. TIQ schematic.

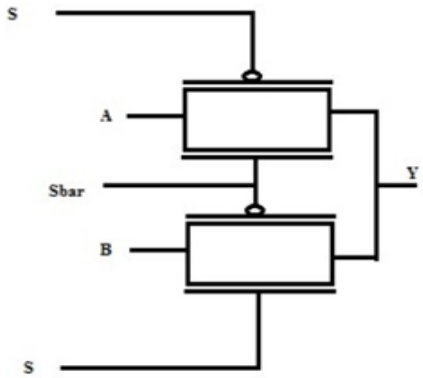

Figure 3. Transmission gate of 2 × 1 MUX used for encoder design.

3. Proposed Method

The proposed design operated at 1 V of input frequency 10 MHz has been implemented in 45 nm technology using the Cadence Virtuoso tool. The design is simulated and power analysis was done to calculate the average power (Figures 4–6).

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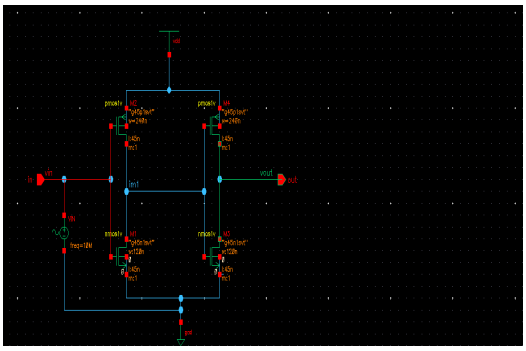

Figure 4. CMOS TIQ comparator schematic.

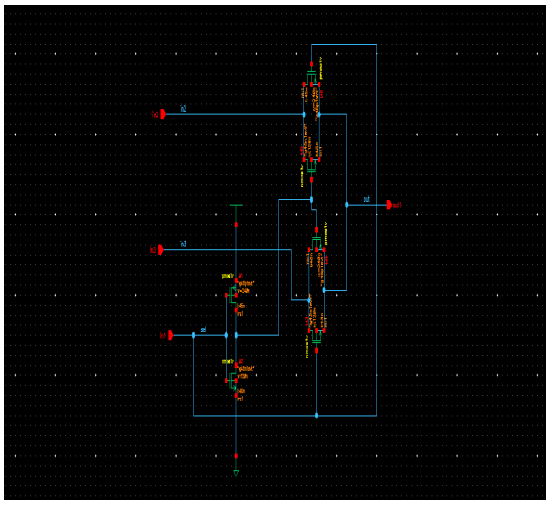

Figure 5. Encoder schematic using 2 × 1 MUX.

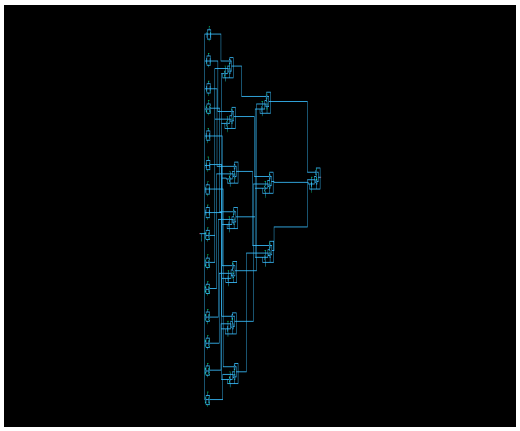

Figure 6. CMOS 4-bit flash ADC schematic.

3.1. TIQ Comparator Schematic

Comparator is design using two cascading inverters where the size of p-type MOS and n-type MOS in widthwise is 240 nm and 120 nm, the dimension in lengthwise is 45 nm. 1 V sinusoidal signal of 10 MHz is given as the input. The value obtained from first stage was fed to the second stage as an input driver. Final comparator's output is taken from the second stage.

3.2. Encoder Schematic

The encoder is designed using 2 × 1 MUX where the channel parameters of PMOS and NMOS were same as the comparator design. The final value of the comparator was provided as an input for 2 × 1 MUX which is selected and given as output based on the select line.

3.3. Flash ADC Schematic

Flash ADC circuit uses 15 TIQ comparators and eleven 2 × 1 MUX as the encoder stage. 11 MUX are divided as three stages where first stage consists of 7 MUX, second stage consists of 3 MUX, and final stage contains single MUX.

4. Results and Discussion

4.1. Flash ADC Output

When a 1 V sinusoidal signal of 10 MHz was fed as an input to our Flash ADC design in order to perform transient analysis and the obtained result is 1 V digital signal, shown in Figure 7.

4.2. Power Analysis

Transient power analysis of Flash ADC was done and the result is shown in Figure 8. Average power was calculated

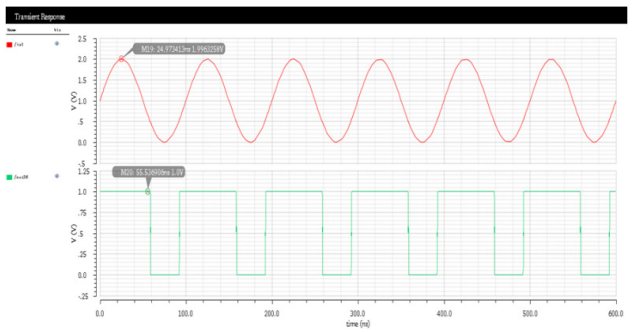

Figure 7. Output of flash ADC.

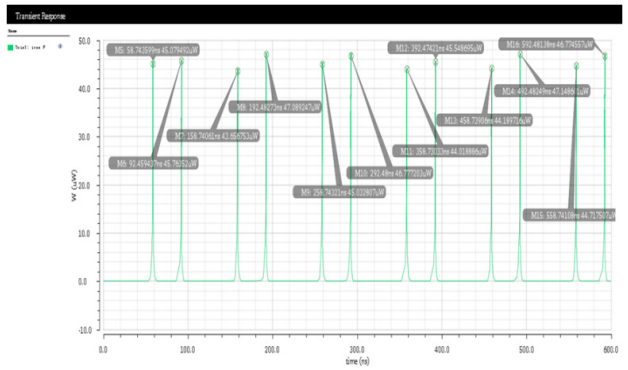

Figure 8. Output of transient power analysis.

and the value is found to be 810 nW. This is optimal power dissipation when compared with existing work.[11]

4.3. Power Analysis Table

When comparing the average power of the existing system with the proposed system design, it has seen been noticed that the proposed design has very low power value. The values are listed in Table 1. Hence the design is named as low power flash ADC design and could be used in applications which require low power.

Table 1. Comparation of average power in different submicron technologies

CMOS technology	Supply voltage (V)	Average power (μW)
180 nm[12]	1.5	300
90 nm[13]	1.2	3300
90 nm[4]	1.2	2424
45 nm[11]	1	14.8
45 nm[a]	1	0.81

[a]In this proposed paper, the average power consumption.

5. Conclusion

Flash ADC was designed with TIQ comparator and encoder in 45 nm technology using the CADENCE VIRTUOSO tool. Conventional ADC design requires resistor ladder which is the main source for power consumption. The significant work of using TIQ comparator eliminates the resistor ladder logic, thereby achieving low power. Thus the proposed Flash ADC design in 45 nm technology gives average power of 810 nW.

In future, we are planned to extract the mask layout of proposed 45 nm 4-bit Flash ADC Design. Area and power in layout may be measured to make it suitable for system designs.

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