

Power Efficient Optimal Structure CAM-Cell in QCA Technology

Ali H. Majeed^{1,2*}, Bassam A. Salih¹, Mohd Shamian Bin Zainal² and Danial M.D. Nor²

¹Electrical Department, Faculty of Engineering, University of Kufa, Kufa, Iraq; alih.alasady@uokufa.edu.iq, bassama.albaidhani@uokufa.edu.iq

²Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Johor, Malaysia; Shamian@uthm.edu.my, Danial@uthm.edu.my

Abstract

Background/Objectives: Quantum-dot Cellular Automata (QCA) is a new nanoscale technology that is expected to be a persuasive replacement of CMOS technology. QCA technology competing for features concerning low power consumption, small physical size, and ultra-high speed. These features are beneficial for memory design. This study presents a new structure of the CAM cell in QCA technology. The presented cell is carried out in an optimal form by using a proposed unique block. **Method:** In this study, the QCADesigner tool was used for circuit design and the QCAPro tool was used for power analysis. Both of these tools were used in default parameters. **Findings:** It was found that the proposed CAM cell is less complexity and efficient in power consumption with improvements by 6%, 29% and 15% in terms of leakage, switching and total energy consumption. **Improvement:** The CAM cell is the main building block for the whole memory. So, the reduction in complexity and power consumption in the CAM cells is important to reach an optimal memory circuit.

Keywords: CAM Cell, Memory Cell, Nanoelectronics, QCA Technology, Quantum-dot Cellular Automata

1. Introduction

Quantum-dot Cellular Automata (QCA) is a new technology that researchers have presented as a solution to overcome and minimize some CMOS limitations concerning the consumption of power, leakage current, and physical size^{1,2}. QCA is a recent nanoscale technology with design techniques that can be considered as a good replacement for those used in classical circuit design. It can achieve good performance with very little consumed power compared to CMOS technology³. The main building block in QCA design is a square cell that has four holes (dots) with two electrons. When Coulomb repulsion occurs, the two electrons occupy holes diagonally inside the cell^{4,5}. QCA memory cell design has been attracted by many researchers. Research efforts⁶⁻¹¹ have focused on the design and performance of the Random Access Memory cell (RAM cell) in QCA. In this work, a new Content

Addressable Memory cell (CAM cell) has been proposed. The CAM, which differs from RAM, is a kind of memory that is likely used in applications that require searching with very high speed¹². In CAM, the access time to stored data in memory is reduced⁴. A new efficient CAM cell with lower complexity (cell counts) and minimum power required has been presented. The gates used to design this structure are XOR gate with two inputs and a majority gate of three inputs. A QCA Designer simulation tool was used for modeling and performance evaluation of the proposed CAM cell structure.

The contents of this study will be as follows: Section 2 will present a review of QCA technology and CAM cell. The proposed model of CAM cell will introduce in Section 3. Section 4 will provide the results and compression with discussion. The conclusion will summarize the work in Section 5.

*Author for correspondence

2. Preliminaries

2.1 QCA Technology

QCA is a new nanoscale technology that was introduced for the first time by¹³. The basic building unit in QCA circuits is a square cell. Each cell contains four holes with two electrons. The Coulombic force controls the electron's movement inside the cell¹⁴. Logic states whether 0 or 1 in the cell depends on the electrons configuration inside the cell. Cell polarization can be calculated using Equation (1). Where p_i represents the probability of the electron existing inside dot i . The cell represents logic 1 if it is polarized equal to +1 and if it is polarized equal to -1 it represents logic 0¹⁰. Figure 1 explain the QCA cell structure with its polarization.

$$p = \left(\frac{p_1 - p_2 + p_3 - p_4}{p_1 + p_2 + p_3 + p_4} \right) \quad (1)$$

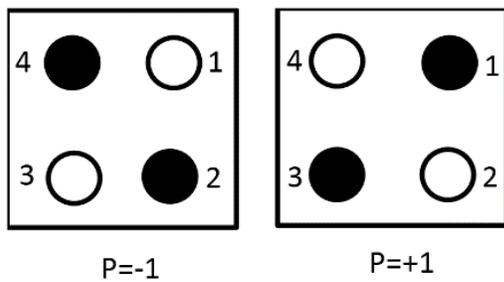


Figure 1. Polarized QCA Cell forms.

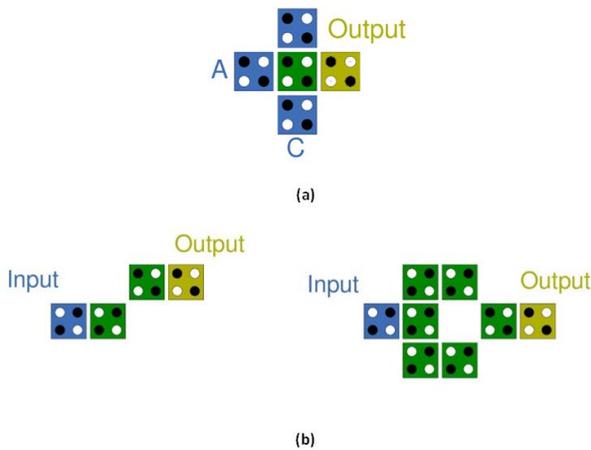


Figure 2. QCA Basic gates. (a) 3-inputs Majority structure. (b) Inverter structures.

2.1.1 QCA Basic Gates

The basic gates in QCA technology are the majority gate and the inverter as shown in Figure 2¹⁵. The majority gate function for 3 inputs (A, B, C) is $AB+AC+BC$. OR or AND gates with 2-inputs can be constructed utilizing 3-inputs majority gate. This can be done by connecting any of the three bits of majority gate to logic 1 or logic 0. Many papers were published in literature focused on the majority gate for both three and five bits¹⁶⁻²³.

2.1.2 Clock Signal

In QCA circuits, a clocking signal is necessary for controlling the information flow²⁴. The circuit can be divided into four different regions (zones). Each zone has four phases. The clock signal controls the barrier between the holes to allow or prevent electron tunneling²⁵. Figure 3 shows the four-zone clocking scheme.

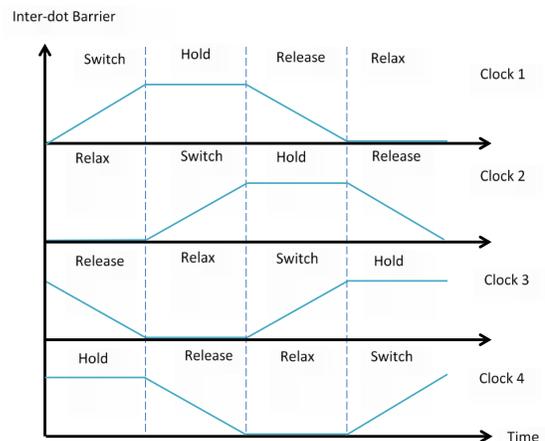


Figure 3. The common clock zones in QCA.

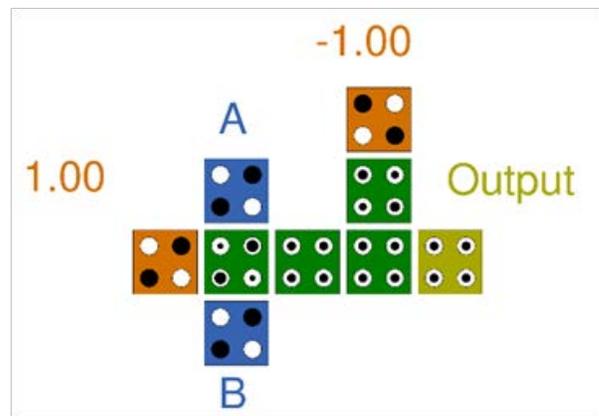


Figure 4. Optimal QCA XOR gate³³.

2.1.3 The XOR Gate

The 2-input XOR gate is widely used in logic circuits. In QCA, researchers introduced many forms of 2-input XOR gates²⁶⁻³³. Some of them follow Boolean function while others use the inherent capability of QCA to get the output. The optimal design XOR layout was presented by³³ as shown in Figure 4. This layout will be utilized in this study to obtain the XNOR gate by exchanging the fixed cells.

2.2 CAM

CAM structure is built for very fast memory searching purposes. The CAM has the ability to search all of its contents within just one clock cycle. To access stored data on CAM, it makes a searching process, produces a match signal and then, restores addresses of the content.

3. The Proposed Structure

This section will explain a new CAM cell structure formative by a proposed unique block.

3.1 The Proposed Unique Block

As mentioned before, the most significant challenge for researchers is to minimize cell count and to increase speed. This research introduces a new QCA block as attempting to improve the performance of CAM memory. Equation (2) describes the function of this block. An XNOR and majority gates were utilized to design the unique block as shown in Figure 5.

$$\text{Output} = (A \odot F) + K \tag{2}$$

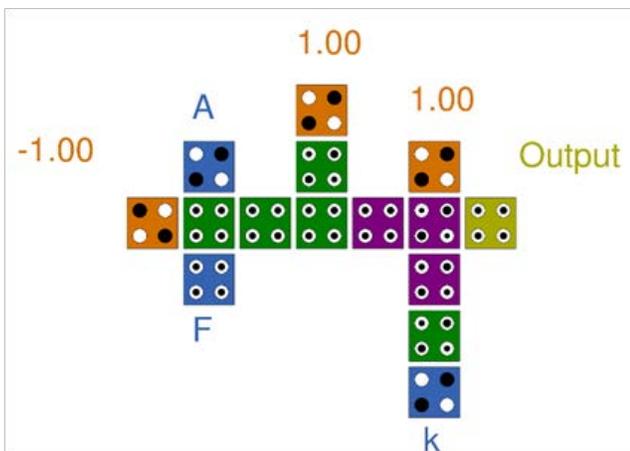


Figure 5. The proposed unique block.

3.2 The Proposed CAM Cell

Figure 6 shows the proposed QCA structure of the CAM cell. The structure of this cell consists of a single unique block and three of 3-input majority gates. The CAM cell comprised of two main parts which are the proposed block and memory unit. The memory unit receives two signals which are Read/Write (R/W¹) control signal, and input data (I). Additionally, it has one output signal (F). The proposed block has three inputs which are input (F) which comes from the memory unit, input (A) and input (K). It also has an output (M) which determines its state according to (A) and (K) inputs. The operation of the memory unit depends on the value of the (R/W¹) control signal. Connecting (R/W) line to logic ‘0’ makes the output (F) tends to logic ‘0’, which represents the (Write) operation whereas setting (R/W¹) to logic ‘1’, the memory cell will perform the (Read) operation accordingly. The memory unit functionality table is illustrated in Table 1. In the proposed unique block, the setting input (K) to logic (1) will tend output (M) to (1), regardless of the logic state of (A) and (F). While connecting input (K) to logic (0), the output (M) will be dependent on (A) and (F) values.

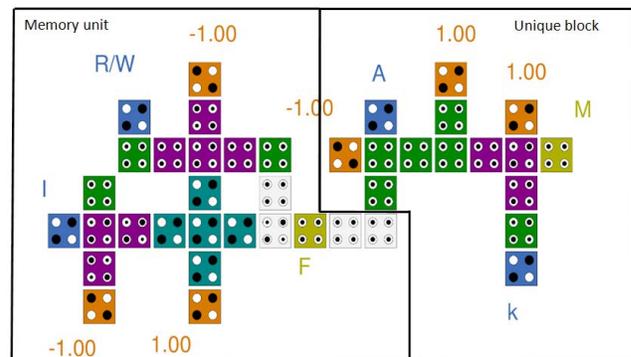


Figure 6. QCA layout of proposed CAM cell.

4. Simulation Waveforms and Discussion

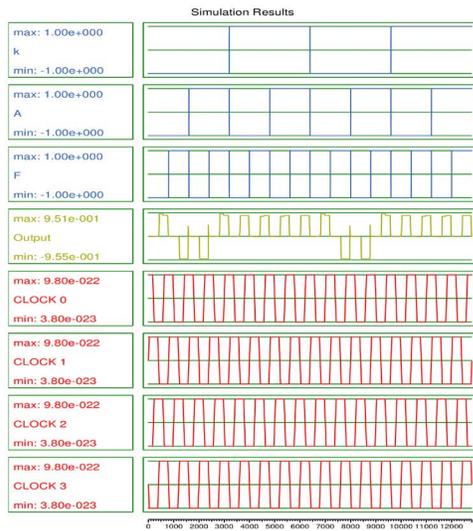
The circuits simulation using QCA Designer software³⁴ are provided in this section. The software parameters have been set to default. Figure 7(a) shows the simulation result of the proposed block while Figure 7(b) shows the simulation result of the proposed CAM cell as well. The CAM cell comparison table is given in Table (2). In addition, QCAPro software hyperlink³⁵ has been used for power consumption analyses of the presented QCA

circuits. The energy dissipation thermal map in the proposed CAM cell is shown in Figure 8. The analysis of power consumption is illustrated in Figure 9.

Table 1. Memory operation truth table

Operation type	R/W	Previous F	I	F
Write	0	x	1	1
Write	0	x	0	0
Read	1	1	x	1
Read	1	0	x	0

(a)



(b)

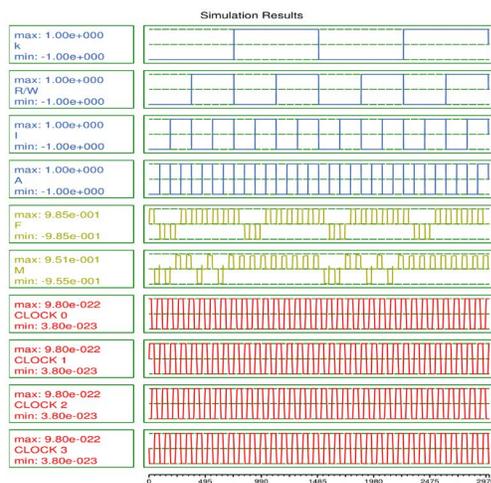


Figure 7. Simulation output for. (a) Proposed block. (b) Proposed CAM cell.

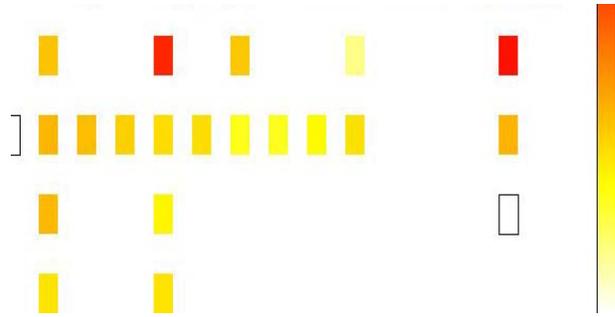


Figure 8. The energy dissipation thermal map for proposed CAM cell.

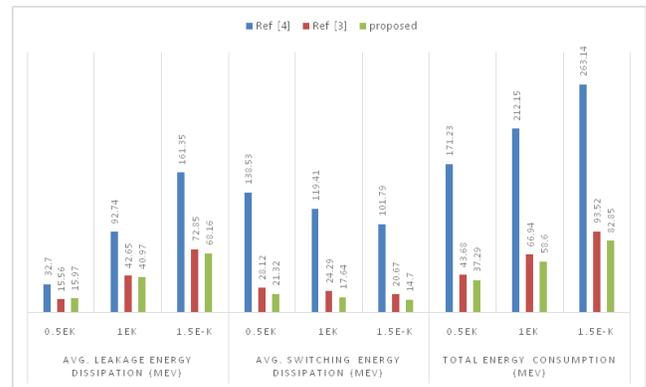


Figure 9. Power dissipation comparison of CAM Cell.

Table 2. CAM cell compression table

CAM cell	Cell counts	Delay	Area (μm^2)
$\text{In}^{4,12,3}$	100	2	0.14
In^{12}	94	2	0.11
In^3	46	1.25	0.04
proposed	40	1.25	0.04

As previously seen, the power analysis indicates that the proposed CAM cell is efficient in power consumption and makes improvements by 6%, 29% and 15% in terms of leakage, switching and total energy consumption. The results have been analyzed at three stages ($0.5 E_k$, $1 E_k$, and $1.5 E_k$).

5. Conclusion

In this research, a unique block with minimum cell counts was proposed for utilizing in CAM cell design. Next, a

new power-efficient structure of CAM cell has been proposed. QCADesigner tool was used to design the circuits while the QCAPro tool was used for power analysis. Simulation results clearly showed through comparison that the proposed design performance is better than the same counterparts.

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