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Design and Simulation of 4-Bit Flash Analog to Digital Converter (ADC) for High Speed Applications

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Abstract

Objective: To design 4-bit flash Analog to Digital Converter (ADC) for high speed applications. The objectives of the project are to design sample and hold circuit, high efficient DAC circuit, to design a high speed, low power and minimum delay CMOS comparator and thermometer to binary code convertor logic. **Methodology:** The main block of flash ADC is designing of comparator. For high speed applications Flash ADC requires comparator having high sensitivity and low power dissipation. In this we have used CMOS comparator with cascaded stages, each stage will help in increasing gain and sensitivity and reducing the all types of noises. First stage is the pre-amplifier stage whose output is given to the input of decision stage. Decision stage is followed by post-amplifier stage. **Findings:** In most papers for designing flash ADC they used dynamic comparator, these dynamic comparators are more difficult to design and will give more power dissipation. In our design we used CMOS comparator with cascaded stages, this type of comparator provides less power dissipation, less delay and high sensitivity by reducing the noise like kickback noise, offset voltages etc. The design is simulated in 180 nm Technology with Cadence Virtuoso Tool and LT spice. Designed comparator has Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) error considered for design within +/- 0.5LSB. For N-bit flash ADC we have 2^{N-1} comparators, whose outputs will generate patterns of 0's and 1's in form of thermometer code; in order to convert it into binary format we have used mux encoder. This mux encoder logic reduces area and very easy to design compared to other methods. **Applications/ Improvements:** Flash ADC's are used in various applications ranging from radar receivers, digital sampling, and LAN interface. The proposed design achieved a power dissipation of 0.121 mW with delay of 19.4 ns. The comparator block is designed and simulated. The sensitivity of the comparator is 0.003V.

Keywords: CMOS Comparator, DNL and Binary Code Converter, Flash Analog to Digital Converter (ADC), Integral Non-Linearity (INL)

1. Introduction

Analog to Digital Converter's (ADC) have primary importance in converting real world analog signal to digitized signals in the form of 0 and 1. Among all ADC's Flash is preferred due to its high speed in nature[1]. Flash ADC's are used in various applications ranging from radar receivers, digital sampling, and LAN interface[2]. Figure 1 shows main blocks of flash ADC. In general for N-bit flash ADC needs 2^N resistor ladder, 2^{N-1} comparators, Thermometer to binary code convertor. Main four blocks in Flash ADC includes sample and hold circuit, DAC circuit, comparators and thermometer to binary code convertor[3].

In[4] the A/D conversion process, first step is to convert continuous analog signal to discrete number of values and hold the signal till next clock pulse which is run by sample and hold block. This discrete signal is given as an input to comparators it compares the analog signal with the output of the DAC block. Comparator outputs as thermometer code are given to binary code converter. The purpose of the comparator is to give the difference between the two applied voltages in terms of 0 and 1[5]. The comparator output gives 1 when input given to positive terminal is equal or more than negative terminal of the comparator, otherwise it will give zero. The output from comparators generates a pattern of 1's and 0's, called as

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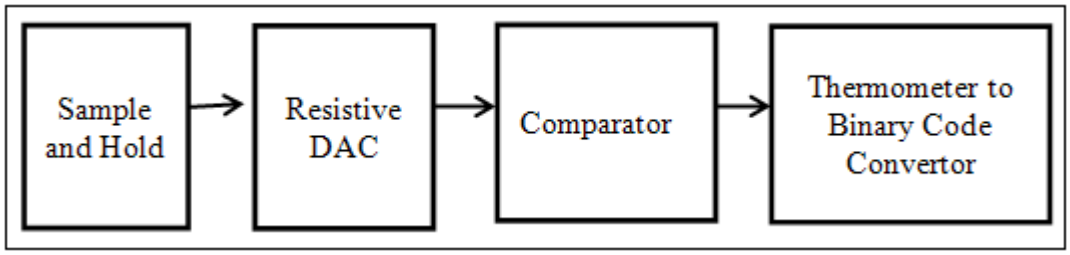

Figure 1. Main blocks of flash ADC.

thermometer code which is outputted to binary code conversion in order to convert it into binary format[6]. Comparator is heart of the ADC[7]. Figure 2 shows the block diagram of CMOS Comparator which is designed by preamp, latch and post amp stage.

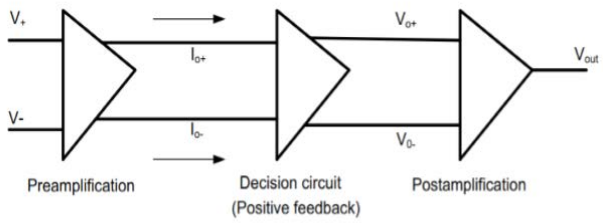

Figure 2. Main block diagram.

The preamp stage improves the input signal and increases the susceptibility of the comparator. It also improves the signal strength by filtering the noise coming from previous stages[8]. The positive feedback stage discriminates milli volt signal and finds the larger input signal. The post amplifier magnifies the data from positive feedback stage[9,10]. Figure 3 shows N-bit Flash ADC circuit.

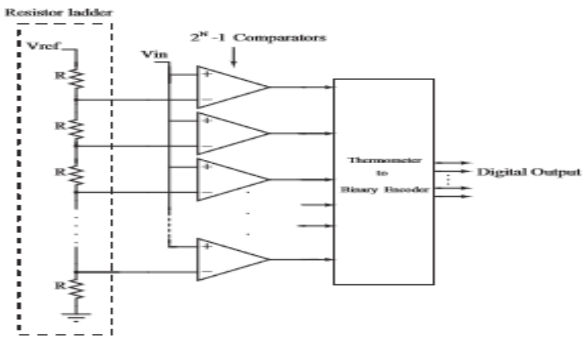

Figure 3. Flash ADC.

2. Literature Survey

Increasing speed, sampling rate and resolution and low power consumption is the main focus of the research on ADCs.

In[1] presented a 7-bit 500-MHz flash ADC is designed achieving very low noise error and having very high propagation speed. This ADC architecture was simulated in cadence environment using gpdk90-nm CMOS technology with a power supply of 1.2-V. Simulated results achieved SNDR of 39.36 dB, SFDR of 40.75 dB and an ENOB of 6.25 bits at a sampling rate of 500 M Hz.

In[2] present different types of ADCs. Different ADCs have their different encoding methods, conversion time, conversion methods, size, andresolution and simulated in different simulation environments. In preset world physical values, such as pressure, humidity, temperature and voice can be measured are in the form of analog (continuous) signals. In this paper, there are many types of ADCs which can be classified according to the applications and concept on which they were designed are showcase for processing real world analog signals. ADCs including, Direct conversion or parallel ADC (Flash), Successive AppRoximation (SAR) ADC, integrating ADC, Pipeline ADC are discussed. In some cases, many comparators are used to reduce the complexity of design, power consumption and improve the linearity and noise which are also explained in this paper.

In[6] presented Low power 3 bit Flash ADC with less leakage power reduction by using SVL [self-controllable voltage level] technology and eliminating ladder resistor bank is designed and simulated. This paper, the focus is given on dynamic power, static power consumption and total delays of ADC. The Threshold Modified Comparator Circuit (TMCC) is used in order for reducing total power dissipation. The SVL technique used here reduces the leakage power dissipation.

In[9] presented 6 bit flash ADC using 180 nm CMOS technology is designed to greatly reduce the total area covered by using less number of transistors. The sub-blocks of ADC like resistor ladder network, comparator, modified sample and hold circuit; and ROM encoder are implemented and simulated and verified. The proposed project used two transistor based TIQ comparator as it is advantageous over conventional comparators, as it greatly reduces the area with less number of transistors count. The proposed comparator dissipates total power of 867.9 pW with maximum delay of 46.31 ps. The modified sample and hold circuit achieves very less leakage current of 796.2 μA. The ROM encoder has very less propagation delay of 580.46 ps and low power consumption of 2.07 mW.

In[11] presented 5-bit hybrid flash ADC architecture uses both conventional double-tail comparators and standard cell comparators. The proposed flash architecture has low power consumption as compared to conventional architecture. Low power consumption is achieved by using more number of standard cell comparators than double-tail comparators. In addition to low power consumption, the input dynamic range of the proposed flash architecture is also increased compared to standard cell and TIQ based flash ADC.

In[12] presented a low power dynamic comparator with 4-bit flash ADC which reduced power dissipation from 0.19uW to 0.169uW is designed. Also the propagation delay observed in conventional is 8.5584ns which is further reduced to 3.9151ns in proposed comparator.

In[13] presented a ccomparator evaluation technique that enables full signal reconstruction using a 1-bit periodic comparator beat frequency measurement is designed. 4-bit and 8-bit versions of the flash ADC with a DQOS comparator and a 3-bit time-interleaved ADC using the SDSW comparator have also been designed. The DQOS ADC has been tested up to 25 GHz input signal frequency with performance of 4.3 bits of resolution in Gray code for 19.7 GHz input signal. The time interleaved ADC performance is 4.3 bits for a 15 GHz beat frequency test with an effective sampling rate of 30 GHz.

In[10] presented 6-bit proposed ADC needs only $2^{(N-3)+2}$ preamplifiers and $2^{(N-2)+1}$ comparators, while the traditional flash ADC requires 2^{N-1} preamplifiers and comparators. Compare to the conventional 6-bit flash ADCs, the proposed one can be implemented using reduced number of preamplifiers stages and comparators count. As a result, the proposed ADC architecture has smaller size and lower power consumption. In addition, the operation speed can be improved since the total input capacitance of the preamplifiers and comparators can be reduced substantially.

In[14] presented designed single-bit comparators and multi-bit flash ADCs using three flavours of periodic comparators; one flavour uses a Differential Quasi-One-junction (Superconducting Quantum Interference Devices (SQUID)) (DQOS) comparator, the second use a Differential SQUID Wheel (DSW) comparator and the third uses a Symmetric Differential SQUID Wheel (SDSW) comparator with time-interleaved clocks. This evaluation technique enables to quantify the comparator SNR, duty cycle distortion, and sensitivity to duty DC bias, in addition to comparison with simulated reconstruction using a similar scheme.

In[15] presented among all high speed low power Flash ADC. A design with 3-bit resolution has been implemented using seven OTA based comparators with a reference voltage of 250mV and a high speed encoder have been implemented using four full adders upon which the integration of different block ADC has been designed. All the circuits are simulated using 180nm technology in Cadence Virtuoso Design environment. This paper demonstrates ahigh speed three bit flash ADC used for Wireless LAN applications. The designed converter is a practical approach targeted at low power high speed converter for wireless applications. This design is a flash based ADC converter with a finite output resolution of three bits and power consumption about223uW and occupies a chip area of 0.089287 mm.

In[7] presented a fully integrated master-slave Emitter-Coupled Logic (ECL) comparator and a frequency divider implemented in 4H-SiC bipolar technology. In this paper the comparator consists of two latch stages, two level shifters and an output buffer stage. According to the simulation results the circuits have been tested up to 500 °C, the single ended output swing of the comparator is -7.73 V at 25 °C and -7.63 V at 500 °C with a -15 V supply voltage. The comparator consumes 585 mW at 25 °C. The frequency divider consisting of two latches shows a relatively constant output voltage swing over the wide temperature range. The output voltage swing is 7.62 V at 25 °C and 7.32 V at 500 °C.

In[3] presented the design of the conventional three-stage comparator in 90-nm CMOS technology. The paper also provides a comparative analysis of the conventional comparator with the latch-based and hysteresis-based comparators and the circuit design and analysis has been

done using Cadence at 1 V supply voltage. From the comparative analysis, it is seen that the offset voltage of the conventional comparator is less than others. Noise immunity of the hysteresis comparator is better than other comparators. If the area is concerned, the latch based comparator is better.

In[8] presented Analysis and design of a high-speed comparator with improved input referred offset is presented in this paper. In this paper comparator is designed in TSMC low power CMOS technology under 1.2 V power supply and new presented comparator has low power consumption and utilizes dual offset cancellation technique. According to the simulation results the minimum convertible input voltage is calculated to be 52 μV and the propagation delay at this worst case is equal to 219 ps and the power consumption at 1 GHz clock frequency is 755 μW.

In[16] presented an ultra-high speed and low offset preamplifier-latch comparator, the comparator use two negative resistors parallel with positive resistors as load resistors of preamplifier to improve its gain so as to reduce offset voltage and meanwhile, the comparator uses a novel method to reduce the recovery time of regenerative stage by add a pre-set quiescent current. Based on TSMC 0.18um CMOS process model, simulated results show the comparator can work under ultra-high speed clock frequency 1GHz and the comparator has a low offset voltage (0.9mv), a short fall delay time (60ps) and rise delay time (50ps). With 1V swing, it is suitable for 10bit 1GSPS high speed ADC.

In[5] presented a 8-bit Successive Approximation Register (SAR) ADC is designed using non-redundant SAR structure and sequencer/code Register structurefor low power operation. In this work, op-amp based comparator is used instead of dynamic latched comparator. Voltage mode R-2R ladder DAC is used to provide analog signal for Comparison to the comparator. The proposed SAR ADC draws a small amount of power 1.49mW for non-redundant SAR logic structure and 1.65mW for sequencer/code register structure at 1.2volt supply and 14MHz sample frequency.

The conclusion drawn from the literature survey is as follows:

1. Various comparator architectures are available in literature. It is found that, dynamic comparators have less power dissipation and input offset voltage.
2. Among all encoder logics studied in papers, encoder logic using mux reduces the power dissipation and area.
3. Various ADC architectures are available in literature. It is found that, Flash ADC is used in high speed applications; SAR ADC is used for medium to high resolution and less power consumption applications. For applications including precision and industrial measurement sigma-delta ADC is used and for voice band and audio applications pipeline ADC is used.

3. Proposed Architecture

3.1 Comparator

3.1.1 Preamplifier

Figure 4 shows Preamplifier stage of the comparator comprises of a single stage diff amp with active circuitry. The preamplifier stage helps in minimizing offset voltage[17]. The preamp strengths the input signal to increase the speed of comparator, because large the difference to positive feedback, faster the speed of the positive feedback stage makes the good decision[11].

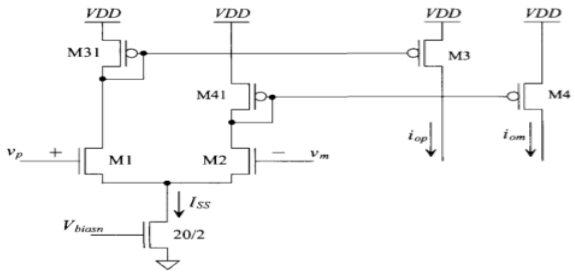

Figure 4. Preamplifier stage.

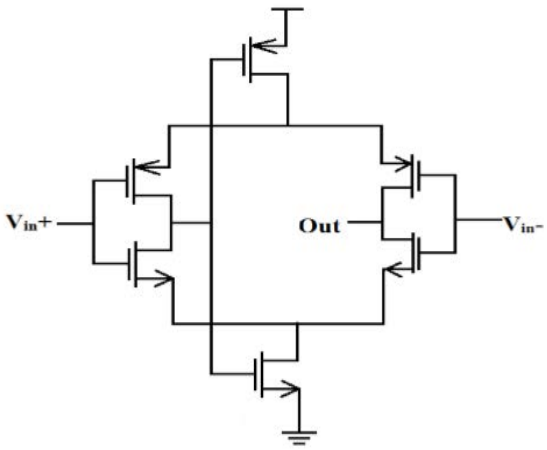

Figure 6. Buffer circuit.

3.1.2 Positive Feedback Circuit

Figure 5 shows the positive feedback circuit is basically a simple latch circuit. It takes input from the preamp circuit and provides output in terms of 0's and 1's depending on if the inputted signal is high or low[16].

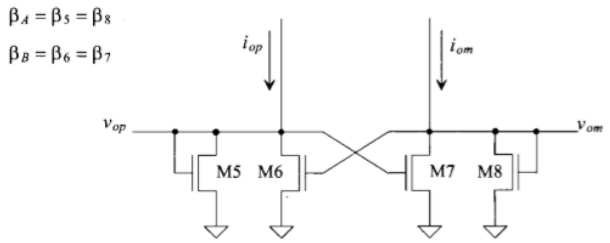

Figure 5. Positive feedback circuit.

3.1.3 Output Buffer

The output of the positive feedback stage is given to buffer stage. Figure 6 shows buffer circuit. This stage simply consist back to back CMOS inverters. This stage boosts the signal coming from positive feedback stage to desirable level[14].

3.2 Thermometer to Binary Code Convertor

The block is required to get the correct binary values of the applied input analog signal. It encodes set of zero's and one's coming from comparators to binary format[15]. Figure 7 shows realization of binary code converter circuit using multiplexor. In our design we used 2:1 multiplex for realization of binary code convertor circuit. It has 15 inputs and 4 outputs[12,13].

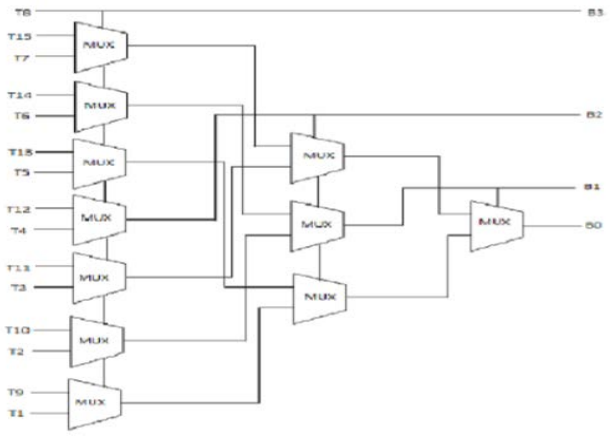

Figure 7. Realization of binary code converter circuit using multiplexor.

4. Simulation Results

Figures 8 and 9 show schematic and output of sample and hold circuit design for 0.1MHz. Figure 10 shows the schematic of realization of 2:1 mux by using NAND gates.

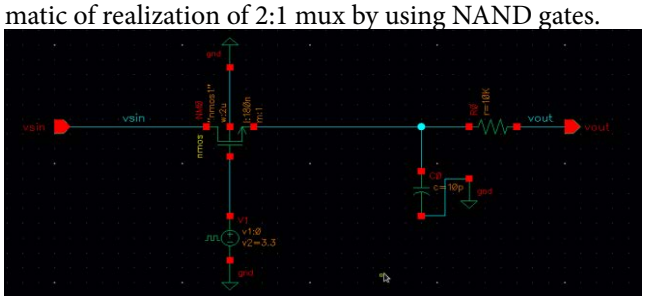

Figure 8. Schematic of S/H circuit.

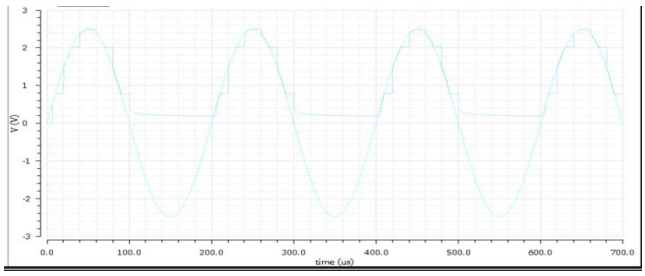

Figure 9. Output waveforms of S/H circuit.

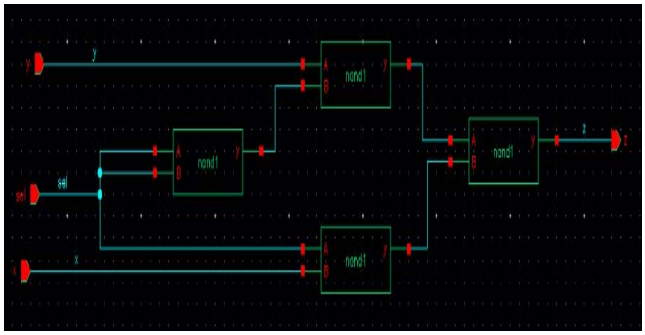

Figure 10. Schematic of realization of 2:1 mux by using NAND gates.

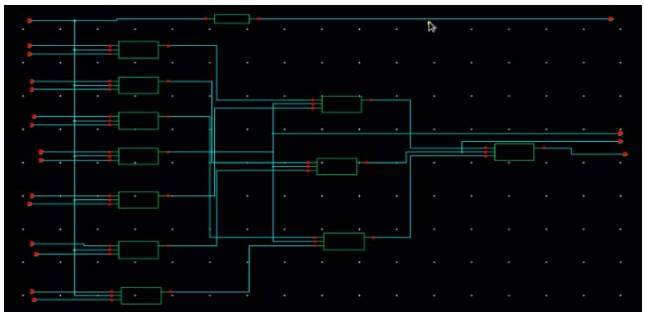

Figure 11. Schematic of binary code converter for 4-bit flash ADC.

Figure 11 shows the schematic of binary code converter for 4-bit flash ADC. Figure 12 and 13 shows the schematic and output of comparator circuit. Figures 14 and 15 shows the final schematic and output of 4-bit Flash ADC simulated in cadence virtuoso tool.

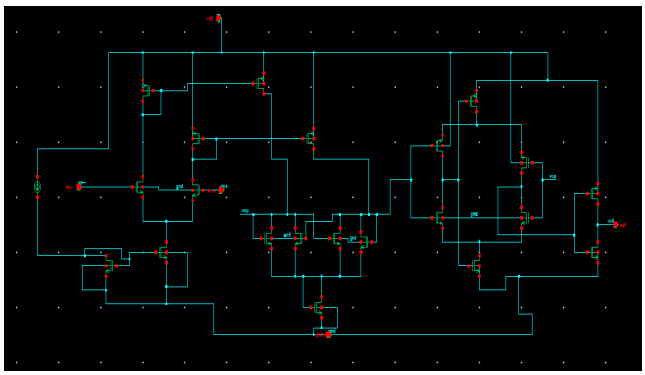

Figure 12. Comparator circuit diagram in cadence.

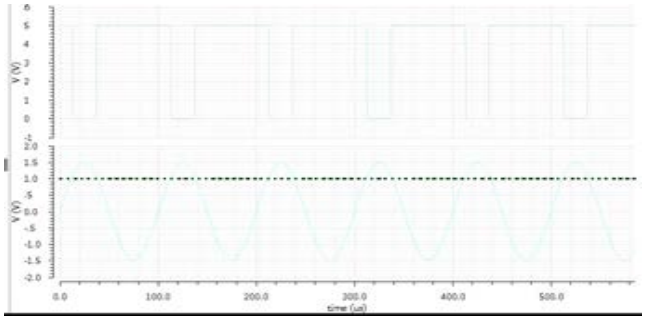

Figure 13. Comparator output.

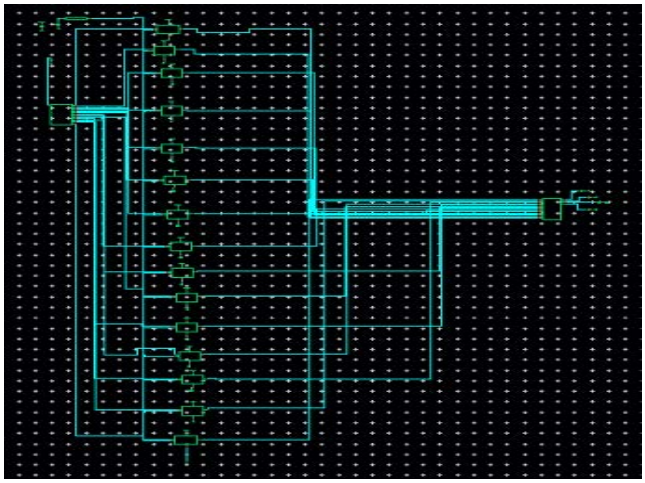

Figure 14. 4-bit Flash ADC circuit diagram in cadence.

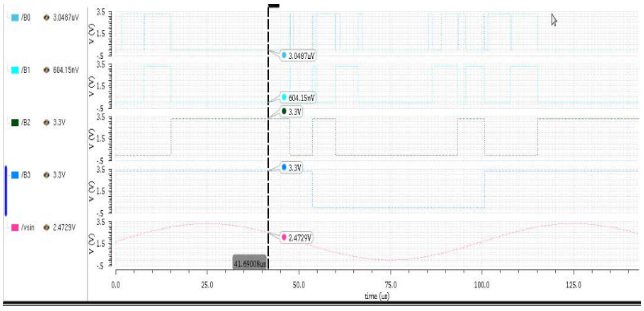

Figure 15. 4-bit flash ADC output.

5. Conclusion and Future Work

The sample and hold circuit, DAC, comparator and Thermometer to binary code converter is designed and simulated in CADENCE virtuoso tool using 180 nm technologies and also verified by LT spice tool. The various analysis like AC, DC and transient analysis are performed for above said functional blocks with the help of CADENCE tool. The comparator design achieved sensitivity of 3mV, having power dissipation 35.5µW and total propagation delay of 5.1 ps. The proposed flash ADC design achieved a power dissipation of 0.091 mW with delay of 19.4 ns. The flash ADC is working as per the specifications. The Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) achieved are within the +/- 0.5 LSB. The proposed architecture can be extended to medium to high resolution applications. For comparator design offset cancellation techniques can be adopted in order to reduce the offset voltage which improves the efficiency of Flash ADC. For thermometer to binary code converter logic can be implemented using another technique instead of multiplexers to reduce area and power dissipation.

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