Indian Journal of Science and Technology, Vol 12(36), DOI: 10.17485/ijst/2019/v12i36/147751, September 2019
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Study of the Impact of Variations on Standard Cells

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Abstract

Objectives: The scaling down of CMOS technology feature size may bring out many benefits in terms of area, performance, cost etc., but the undesirable effects such as variability in the parameters of the circuit and operating environment are increasing which in turn leads to uncertainty in the circuit performance and lowering of yield. In this study, the impact of variations has been analyzed, on the delay of standard cells. It is necessary to model variations to predict the performance. **Methods:** This analysis is performed by different Variation modeling techniques for Standard Cell Characterization. The Monte Carlo technique introduces randomness by changing the threshold voltage such that it is different for different transistors at the same time. In contrast, Liberty Variation Format used for lower technologies, gives the variation of a cell delay at 1 sigma of delay distribution per arc which covers all slew-load, arc and when conditions. **Findings:** The delay for every cell varies based on the active arc/input transition/output load. After running the simulations for Cell a using Monte Carlo and Liberty Variation Format technique, the result and delay spread for Monte Carlo simulations is obtained which is compared with the standard deviation values from the Liberty Variation Format simulations. After comparing them we can see the values almost tend to be equal. This way instead of running the Monte Carlo Simulations, which have a huge runtime we can also obtain the accurate standard deviation (sigma) values from the Liberty Variation Format simulations. **Application:** The simulation results demonstrate the variation in the delay of those cells from the nominal value and which modeling technique can be used for efficient Variation calculation for circuit parameters.

Keywords: Liberty Variation Format, Monte Carlo Simulations, Process Variations, Standard Cells, Variations

1. Introduction

Semiconductor technologies are scaling down the size of transistors in order to increase the density and to improve the device performance. In the course of manufacturing process, parameters like channel length (L), the channel width (W), doping concentration and oxide thickness (Tox) may vary. This will in turn affect the threshold voltage (Vth) and mobility (μ) that defines the performance of MOSFET devices. The impact of variations on older technologies was limited, compared to the problems faced after the introduction of lower technologies especially below 90nm.

2. Background

"Process variations are the physical deviation of the parameters of devices and interconnections with respect to the intentionally designed values."Changes in the manufacturing process leads to variations in the properties which in-turn defines the behavior of the cells. Standard cells refer to a group of transistors and interconnect structures that provide a Boolean logic or a storage function[1,2]. Figure 1 represents the probability of variations on delay for a single cell for different iterations. Here, the delay spread lies between 55ps to 75ps approximately.

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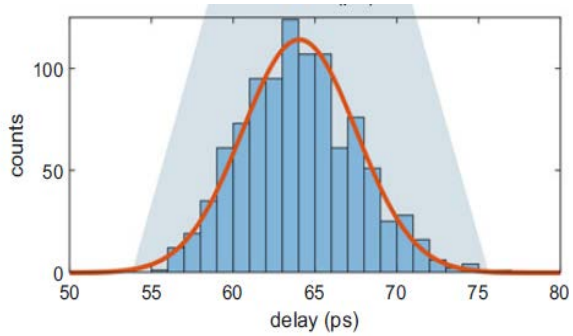


Figure 1. Delay variability due to variations. Adapted from 'Timing Performance of Nanometer Digital Circuits under Process Variations'.

2.1 Sources of Variations

Physical parameters like channel length (*L*), the channel width (*W*), oxide thickness (*T*ox), mainly defines the performance of MOSFET devices[3].

- Channel length (*L*) defines the size of technology. It is affected by manufacturing steps like photolithography and etching.
- Line Edge Roughness (*LER*) of polysilicon edges which leads to variation because of light sources with large wavelengths during lithography.
- Channel width (*W*) variability takes place due to mask alignment during the manufacturing process.
- Gate oxide thickness (*Tox*) is affected by the technology shrinking.
- All the above parameters including random dopant fluctuation affect the Threshold voltage (*Vth*)

2.2 Classification of Variations

The classification of Variations is shown in Figure 2.

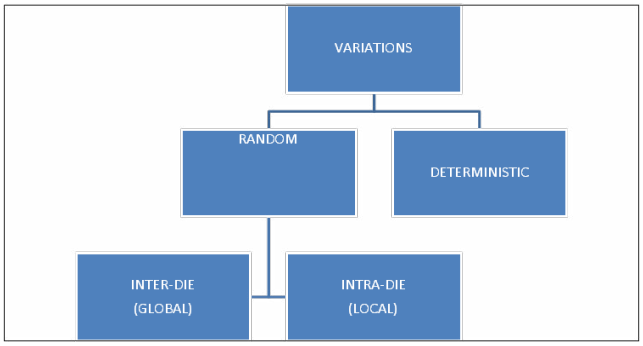


Figure 2. Classification of variations.

Deterministic (Systematic) variations are caused mainly by the steps in the manufacturing flow or equipment related effects.

Random (Non-Systematic) variations are unpredictable in nature which includes channel length, doping variations; this can be divided into Inter-die (Global) and Intra-die (Local) variations[5] shown in Figure 3.

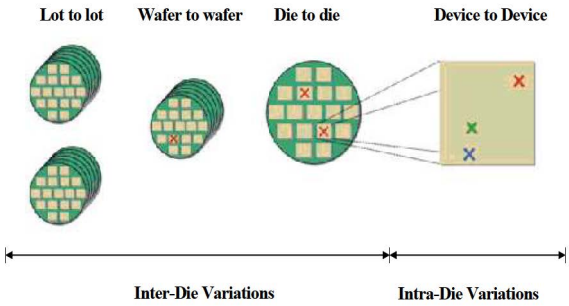


Figure 3. Types of random variations. Adapted from 'Analysis and Design of Networks-on-Chip under High Process Variation' by Rabab Ezz-Eldin, Magdy Ali El-Moursy and Hesham F. A. Hamed, Springer Publication.

2.2.1 Inter-die Variations (Global)

In circuit design, the inter-die variation is regarded as a shift in the mean or expected value of a parameter equally across all devices on any one die[5]. Thus, this variation does not lead to mismatch between different transistors in the same die.

2.2.2 Intra-die Variations (Local)

Intra-die variations occur within a single die and cause device parameters to vary from their intended values across different locations in the same die[6]. Due to this, devices designed with equal dimensions, and manufactured in the same die results in properties and performance which are different from each other.

3. Analysis Methods for Studying Variability

The fluctuations in fabrication steps lead to variations in the performance devices which are undesirable. This excessive spread can result to loss in yield and increase in the cost. So, it is necessary to model variations in order to predict the performance and minimize the impact of it[7]. The key features that affect the delay of a circuit is given in Figure 4.

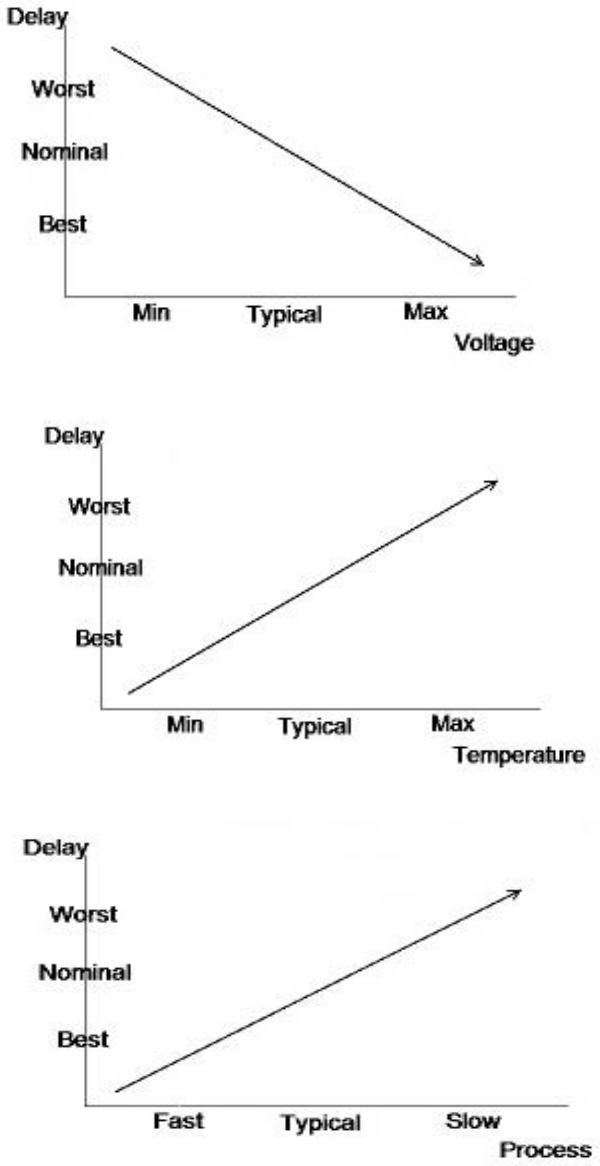


Figure 4. Variation of delay w.r.t PVT, Adapted from "http://vlsi-soc.blogspot.com/2012/06/pvt-and-how-they-impact-timing.html".

Some general techniques used to model the variations in circuit design are given below:

3.1 Corner Analysis

It is the most widely used technique to verify the circuit performance under variations. Here we use the number of PMOS and NMOS parameters to see the performance at nominal, worst and best of process corners as shown in Figure 5.

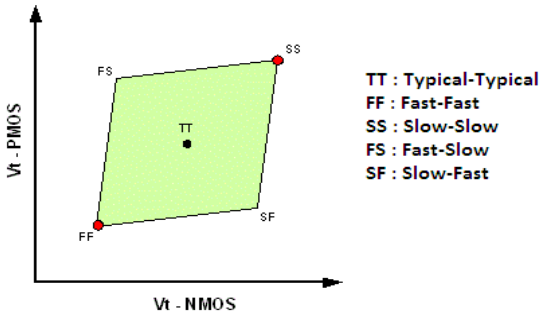


Figure 5. Process corners, Adapted from https://www.vlsifacts.com/mystery-monte-carlo-simulation/.

3.2 Monte Carlo Analysis Technique

After running the simulations across Process Corners, the case where variations in transistors exist across the same process corner is being left out[8]. So, Monte Carlo introduces randomness by changing the threshold voltage such that it is different for different transistors at the same time.

This can be done in two ways: Local Monte and Global Monte.

a. Global Monte: It is unconstrained over different process corners.
b. Local Monte: It is constrained only to a particular corner.

3.3 Sensitivity Analysis

This technique is used to find how sensitive the output with respect to the changes in the input parameters is. This can be used for analytical based modeling or along with other modeling techniques.

4. Existing Variation Modeling Methodologies

4.1 On Chip Variations (OCV)

On Chip Variations (OCV) is used to model local variations during Timing Analysis for nodes above 90 nm. It uses derate number for early and late path for different transitions.

Example: For Early -20%, For Late +20%

Nominal delay = D0

Early delay = 0.8*D0

Late delay= 1.2*D0

This derate is used for all the cells, which may give optimistic values for some but pessimistic for the other cells when we move to lower technologies.

4.2 Advanced On-Chip Variations (AOCV)

Advanced On-Chip Variations (AOCV) also known as Stage Based OCV is simulated for a single input transition and output load combinations. Delay variation of cells in a path is lesser than a single cell because the variation cancels out in a group.

Example: object_type: lib_cell
delay_type: cell
rf_type: fall
derate_type: early
object_spec: */INV
depth: 1 2 3 4 5
Table: 1.0801 1.0736 1.0650 1.0601 1.055

These dates are calculated only for a single arc and slew-load condition. This becomes pessimistic for technologies below 14nm.

5. Variation Modeling Methodology used

5.1 Liberty Variation Format (LVF)

Liberty Variation Format (LVF) is preferred for lower technologies. It gives the variation of a cell delay at 1 sigma of delay distribution per arc. Here the delay variation for all possible slew-load, arc and when conditions are calculated.

Below is one example for LVF table:

```
ocv_sigma_cell_rise(lut_4x4) {
sigma_type : "early" ;
index_1("0.000519, 0.00231, 0.0132,0.0350");
index_2("0.0002, 0.00145, 0.00553, 0.0136");
values("0.00475, 0.0087, 0.0234, 0.0453",\
"0.00657, 0.0108, 0.0240, 0.0481",\
"0.0115, 0.0167, 0.0319, 0.0560",\
"0.0150, 0.0233, 0.0422, 0.0710");
}
```

Delay for every cell varies based on the active arc/input transition/output load[9]. This methodology reduces the pessimism enormously.

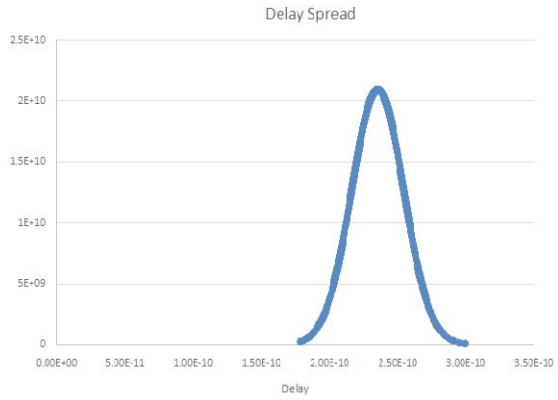
6. Results

The result and delay spread for Monte Carlo simulations for Cell a now looking into the standard deviation values we have obtained from the LVF simulations, in Table 1 and Figure 6.

Table 1. Cell a condition X

Early (s)	Nominal (s)	Late (s)	Average (s)
2.02E-011	2.18E-010	1.95E-011	1.98E-011

Comparing the above average standard deviation with that of Monte Carlo runs, Table 2 is created. We can see the values almost tend to be equal. This way instead of running the Monte Carlo Simulations, which have a huge runtime we can also obtain the accurate standard deviation (sigma) values from the LVF simulations.



Statistics:	
max	2.99E-10
min	1.78E-10
mean	2.35E-10
variance	3.63E-22
stddev	1.91E-11
avgdev	1.52E-11
failedtimes	0

Figure 6. Delay Spread for Cell A

Table 2. Comparison between Monte Carlo and LVF results

Monte Carlo	Liberty Variation Format
1.91E-011 s	1.98E-011 s

7. Conclusion

Here, the impact and causes of variations, on the delay of standard cells has been analyzed. This analysis has

been performed through Monte Carlo simulations and comparing the different methods of Variation modeling techniques for Standard Cell characterization. The simulation results demonstrate the variation in the delay of those cells from the nominal value and which modeling technique can be used for efficient variation calculation.

8. Future Scope

In this study we find the delay variations of a cell for all the possible arcs and conditions, similarly we can perform the same simulations on similar cells or the same cell with different drives and predict the variations for the same. This can later be taken forward for generating an algorithm using interpolation for finding the standard deviation of any number of similar cells. This method will be more time efficient.

9. References

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