

FPGA Implementation of High Speed Digital Pulse Width Modulator (DPWM) Technique for DC-DC Converter

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Abstract

Objectives: Digital Pulse Width Modulator (DPWM) remains essential element in power controlling devices that command power switch of power converters. The focus of this study is to structure DPWM of FPGA base for DC chopper. **Methods:** Buck, Boost, Buck and Boost convertor versions are developed in MATLAB-SIMULINK. Verilog coding is performed for Digital Controller to operate for greater rates, which may be incorporated in high speed surroundings; synthesis is completed utilizing Xilinx ISE, along with Behavioral and Period simulation performed with Xilinx Simulator. After affirmation of code it is downloaded on FPGA Spartan 3AN board. The output is confirmed by means of Oscilloscope. **Findings/Application:** The resulting DPWM is a high speed and less power consuming architecture for Buck, Boost, Buck and Boost DC-DC converter. The utilization of Gray counter and One-hot encoder in DPWM has helped in speed improvement and reduced power consumption. The grey encoding method has fewer states in comparison with the sequential encoding method, which makes them quicker. The output is a Pulse-Width Modulation (PWM) signal, for varying clock frequency and duty cycle. The power consumed by DPWM for various frequencies was verified in comparison with the high frequency DPWM. For 6 MHz frequency, the power consumed by DPWM is 0.01486 w and that by a high frequency DPWM is 0.01486 w. The proposed DPWM can operate at a maximum frequency of 140.298 MHz. This DPWM is best suited for Buck, Boost, and Buck and Boost DC-DC converters.

Keywords: DC-DC Converter, Field Programmable Gate Arrays (FPGA), Pulse-Width Modulation (PWM), Spartan, MATLAB, SIMULINK

1. Introduction

Current research tasks focused on boosting stable state along with the dynamic behaviour of DC-DC converters for high-performance, by signaling different techniques of layout and controlling procedures together with the growing trend to applying digital execution included in analog techniques. Because of accelerated progress in Semi-Conductors and also Micro-processor business, digital controller increased in popularity among Pulse-Width Modulation (PWM) converters and can be shooting more than analog techniques because of accessibility of

rapid pace microprocessors, versatility and resistance to noise and ecological variations. Additionally, greater curiosity in Field Programmable Gate Arrays (FPGA) has made it more suitable layout platform for digitally controlled power converters¹.

2. PWM

PWM, a modulation method which controls the pulse width, officially the duration of pulse, depends on signal information of modulator. Nevertheless, the modulation method might be used to encode data that has to be

transmitted, and also its own primary usage will be to permit the restraint of the power provided to electric apparatus, notably to inertial loads². The standard significance of voltage provided to the load would be managed by the rotation of switch between load and supply and forth in a speedy rate. The more the switch will be on than the off stages, more complex will be the power provided towards the loading. The switching frequency of PWM should be greater compared to that which will impact the load, and that would be to mention the consequent wave form sensed by the load needs to be smooth as you can. A PWM signal isn't constant. Rather, the signal is still on for a portion of its own period off to the others. Even the duty cycle D, refers to proportion of time scale where the signal is currently around. The duty cycle is anywhere from 0, so the signal is necessarily off, to inch, at which the signal is continually on. A 50% D ends in a great square wave. The major PWM benefit is the power loss from switching devices is extremely less. If switch is not turned on, there is no current practically. As soon as the switch is turned on and power has been moved to the load, then there's hardly any drop of voltage throughout the switching. Reduction of power, the product of voltage and current, is hence in each case is near to 0. Even PWM works nicely for controllers, due to its off/on character, quickly will situate the required duty cycle. It has also been applied in some specific communication methods in which its duty cycle was used to communicate information over a communications channel. Like every sort of energy conversion, PWM

drivers or related loads need to be tested and designed to satisfy particular performance and efficacy standards but given the sophistication of waveforms connected with PWM application, precise measurement isn't a very simple job³.

3. Proposed Architecture

The PWM architecture employed for FPGA is shown in Figure 1 which consists of the following⁴:

- *DCM* - It offers SPARTAN 3A FPGA related applications an enhanced clocking ability⁵. DCM generates a new frequency of clock by multiplying the incoming clock frequency. It also eradicates delay in the external clock input and the clock is reduced. DCM understands the input signal from the CLKIN pin and creates phase changed, clock frequency multiplied (2Clk) values. Here in the design clock doublers (2Clk) is employed.
- *Gray Counter* - Grey code assesses the character of binary code or data which consists of on and off indicators, commonly represented by ones and zeros. Grey code is used to check error and clarity correction in binary communications. Grey code is known as reflected binary code. Shifting action is paid off due to one-digit shift in consequence code words.
- *One Hot Encoder* - One hot coding is used to keep away from a comparator, which consumes lot of area and power.

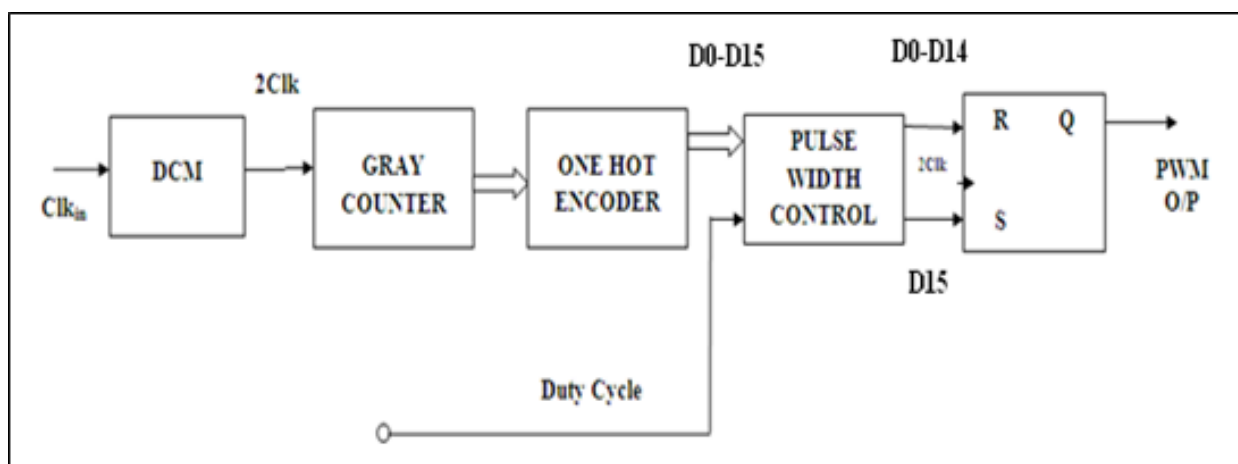


Figure 1. PWM architecture for FPGA.

- *Pulse Width Control* - This block is needed, when there is a feedback in the outside circuit, So PWM width automatically corrects depending on the voltage.
- *S-R Flip-Flop* - It is used for PWM generation, where inside the Set pin makes the line high and Reset Pins makes it low and thus develops a pulse.

PWM benefit in switching circuits is its low power and higher resolution. The input is compared by binary comparator in traditional PWM architectures together with the counter output signal and resetting the Set-Reset flip-flop alike, thereby producing varying duty cycle. Most important benefit in this architecture will be reduced power consumption and smaller circuit area which would necessitate replacing. Comparator and Binary counter alongside One-hot encoder and Gray counter are used to create variable pulses for DC-DC Converters control. Within this structure, for each positive edge of this clock, Gray counter ends turned on. After attaining a "0000" in the counter output, enable logic is made high, switching on the one-hot encoder behaving like a reset pin to this⁶. One-hot encoder output signal is offered for SR flip -flop pin. PWM controller circuit resets the flip-flop dependent on the duty cycle demand and creates a varying duty cycle. The overall device utilization is listed in Table 1.

Table 1. Device utilization summary

Logic utilization	Used	Available	Utilization%
Number of Slices	23	704	3%
Number of slice flip flops	32	1408	2%
Number of 4 input LUTs	19	1408	1%
Number of bonded IOBs	8	108	7%
Number of GCLKs	2	24	8%
Number of DCMs	1	2	50%

4. Result

Our project will result in the following:

- Verilog HDL IP Core for High Throughput DPWM Core.
- A MATLAB-SIMULINK Model for DC-DC convertor for Buck, Boost and Buck-Boost.
- Demonstration of DPWM on FPGA board.

The Xilinx ISE simulation has been used for practical verification of topologies of a PWM generator. Simulations result of 4-bit data entered to PWM device for distinct duty cycle can be seen in Figure 2-4.

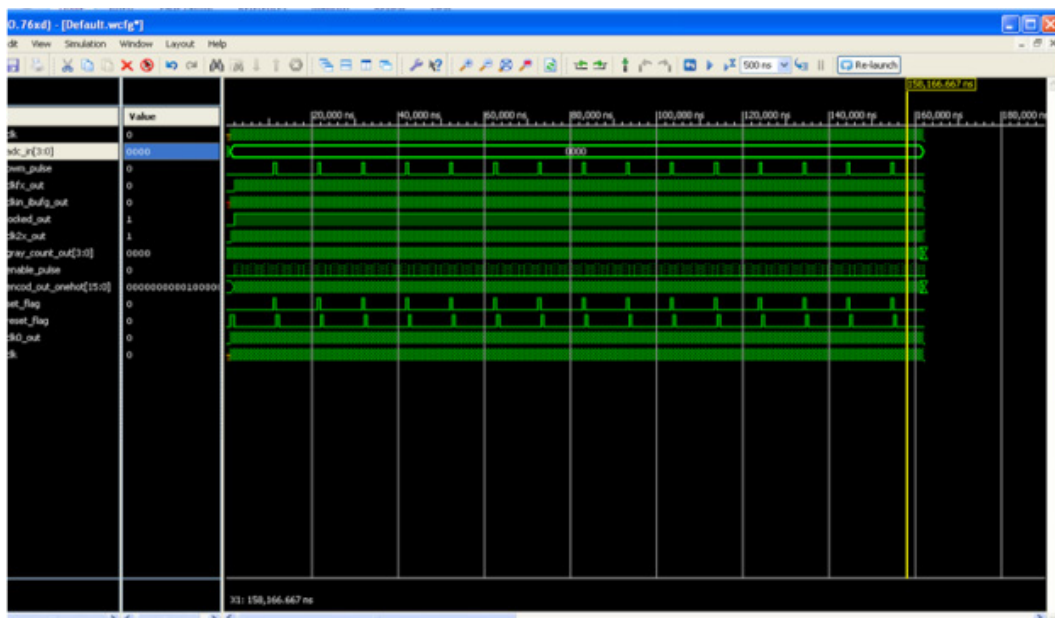


Figure 2. Simulation waveform for duty cycle = 6%.

The oscilloscope output Figures 5 and 6 are shown below following the code has been dumped in the FPGA Spartan

3A kit after code verification. The power analysis report for different frequencies can be seen in Table 2.

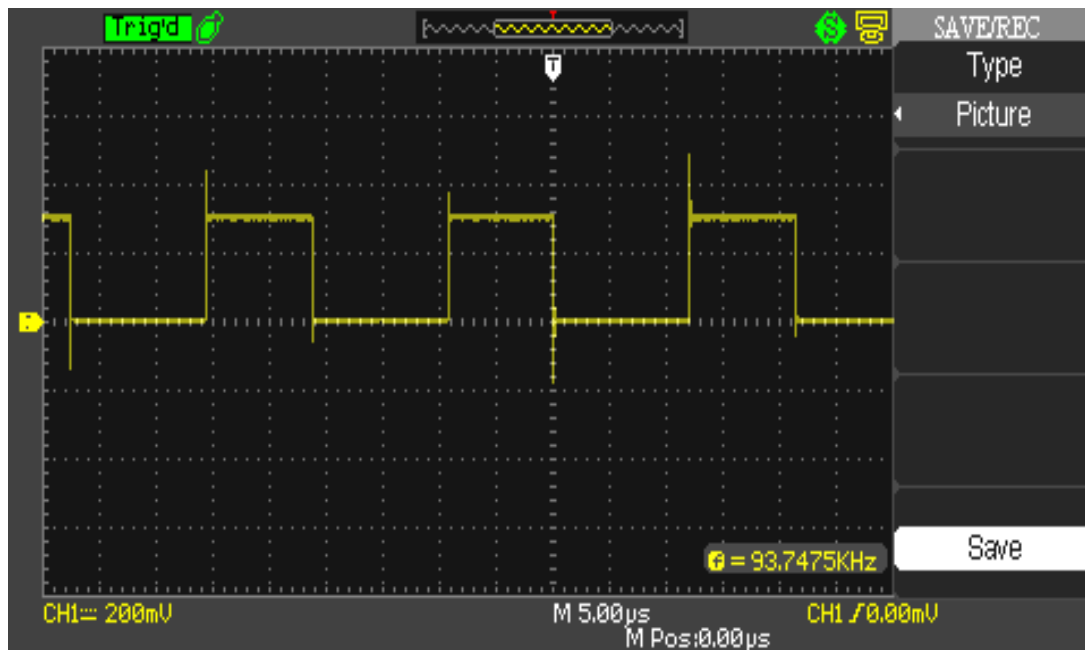


Figure 5. DPWM output for duty cycle = 55%.

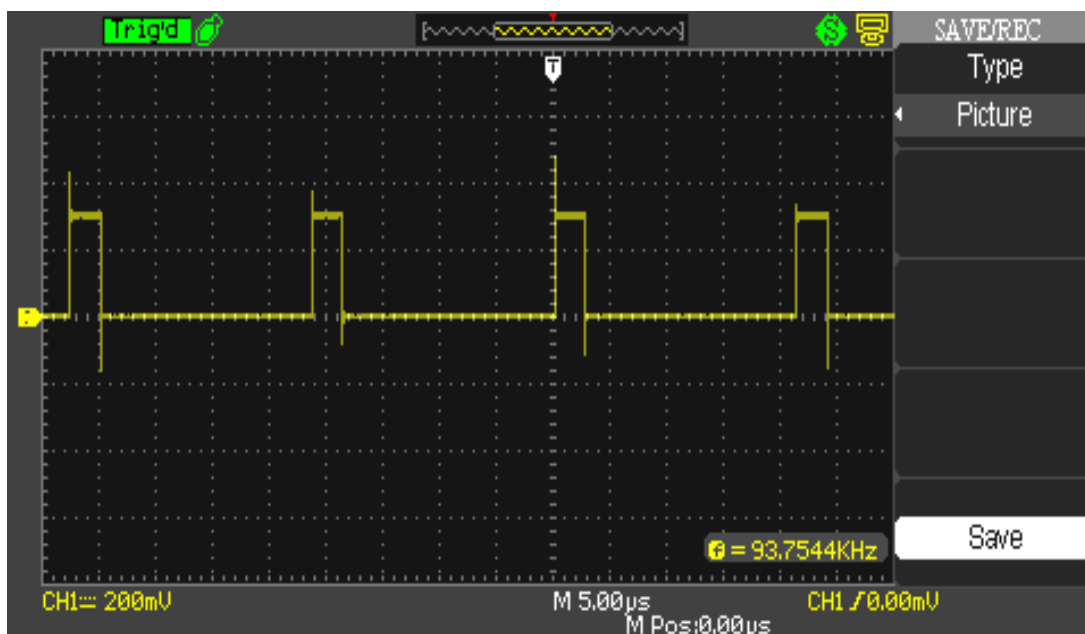


Figure 6. DPWM output for duty cycle = 6%.

Table 2. Power analysis report

Device	Frequency (Mhz)	Power consumption (w)	
		Proposed DPWM	High frequency DPWM
SPARTAN 3A (XC3S50A-4tq144)	6	0.01479	0.01486
	12.5	0.01544	0.01549
	15	0.01569	0.01586
	25	0.01668	0.01696
SPARTAN 3A (XC3S50A-5tq144)	6	0.01480	0.01488
	12.5	0.01544	0.01561
	15	0.01569	0.01561
	25	0.01569	0.01702

5. Conclusion and Future Scope

A new DPWM structure was introduced in this study is to restrain the DC-DC converter. The procedure suggested is based on the grey encoding method; it has fewer states in comparison with the sequential encoding method, which makes them quicker. This DPWM isn't hard to look and can readily alter the resolution too. Based on the FPGA device goal and the amount of control bit inputs the structure operating frequency fluctuates. The suggested DPWM could be implemented in appropriate FPGA device by means of obligatory input control bits and frequency of clock, and as per application requirements. The suggested DPWM structure is examined with SPATRAN 3A FPGA. Resulting PWM signals might be employed for its DC-DC converter to manage the output voltage.

6. References

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