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Analysis on Circuit Metrics of 1-Bit FinFET Adders Realized using Distinct Logic Structures

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Abstract

Objective: To compare and analyse different FinFET full adder circuits by varying the temperature. **Method/Analysis**: A 1-bit full adder is designed using various logic styles and the performance of these adders are compared over a range of temperature values. 32nm FinFET Predictive Technology Model (PTM) is used for designing purpose. Various logic design styles utilised are Complementary Metal-Oxide Semiconductor (CMOS) logic, Transmission Gate (TG) logic, Complementary Pass-Transistor (CPTL) logic, Gate Diffusion Input (GDI) logic. Cadence Virtuoso and Spectre are used for designing and simulation purpose, respectively. **Findings**: The performance of these adders are analysed based on key circuit metrics like static power, dynamic power, leakage power, delay and power delay product (PDP). On comparison, it is evident that the GDI based adder consumes less leakage power. Also, the propagation delay and power delay product is very less in GDI adder. **Novelty/Improvements**: The simulation results prove that the GDI adder structure outperforms other structures in sub nanometer technology. This advantage makes GDI technology suitable for realisation of combinational circuits. Future research in digital circuits can be carried out by using GDI technology for designing low power and compact integrated circuit design.

Keywords: Complementary Pass-Transistor, Delay, FinFET, Gate Diffusion Input, Leakage Power, Low Power Adder, Transmission Gate, CMOS

1. Introduction

Power consumption and operation speed are the most decisive factors for any circuit design. Below the 90nm technology, leakage power acts as a predominant power dissipation. Due to the scaling down of device size, the threshold voltage is also scaled down for improving the performance. As a result, the leakage current increases. Scaling is a process which helps in improving the operation speed at the expense of increase in power dissipation. Hence, it is essential to reduce the leakage power at sub nanometer level. Transistors designed using FinFET technology are used for reducing the leakage power as they provide better control over the channel and allow minimal current to leak through the body during cut-off state.

Various techniques have been utilised for controlling the power dissipation issues. An innovative technique of designing an adder is explained in[1], where a high speed adder is designed using a Branch Based Logic design. Current sink restorer and Diode connected FinFET inverter were used for reducing the voltage step. The proposed architecture had a reduced delay value in comparison with conventional CMOS adder. A 1-bit low power adder was designed in[2], which made use of inverter, multiplexer and an XOR gate in 45nm FinFET technology. It was observed that the proposed circuit exhibits minimal leakage current and is more stable against temperature variations.

A 1-bit full adder is designed in[3], which made use of 32nm FinFET technology. In this study, three differ-

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ent FET models, MOSFET, Double-Gate (DG) FinFET and Carbon Nano Tube FET (CNTFET) were employed. The full adder was designed in CMOS and GDI logic. On comparison, GDI based CNTFET adder consumed less power and had less propagation delay. A quantum FinFET (QFinFET) and a trigateFinFET are analysed in[4], where parameters like drain current and gate capacitance were measured. On observation, QFinFET displayed high gate capacitance and had a reduced leakage power dissipation. On the whole, QFinFET outperformed trigateFinFET when scaling to sub atomic level.

In[5], a Reconfigurable Approximate Carry Look Ahead adder (RAP-CLA) was designed in 15nm technology. This adder operates in two modes i.e. exact and approximate. A correction unit was used for converting approximate value into exact value. Power gating technique is applied. In approximate mode, delay and power were reduced by 55% and 28% respectively. Another pioneering technique of adder design is discussed in[6], where an 8-bit ripple carry adder was designed in 90nm MOSFET technology and 32nm FinFET technology. Various circuit design techniques like TG, CMOS, CPL and GDI logic were used. Parameters like dynamic power, static power, leakage power, delay and power delay product were measured. The FinFET structure reduced the leakage power dissipation by 99% and delay was also reduced by 39%. Comparatively, the GDI based FinFET adder performed better than other adder structures.

By taking into account of the above study, this paper contributes to the following:

- Design and simulation of 1-bit full adder in 32nm FinFET technology.
- Distinct logic design styles like CMOS, TG, CPTL, GDI are used for designing purpose.
- Key circuit metrics like Dynamic power, Leakage power, Static power, Delay and Power delay product are measured.

2. Implementation using Cadence Virtuoso

The 1-bit full adder structures are designed using Cadence Virtuoso in 32nm FinFET technology. The length of both NMOS and PMOS transistor is 32nm. The width of NMOS transistor is 50nm and width of PMOS transistor is 100nm. The supply voltage provided is 0.5V. The full adder designed in CMOS logic is constructed using 28 transistors (14 NMOS and 14 PMOS). It consists of a pull-up network (PUN) and a pull-down network (PDN). The main advantage in this structure is that it passes both strong 0 and strong 1.

The full adder designed in CPTL logic is constructed using 38 transistors (27 NMOS and 11 PMOS). It consists of both true and complementary inputs/outputs. It is mainly used in high speed circuit designs. In this circuit, the threshold voltage drop of the output is restored by using an inverter. The full adder designed in TG logic is constructed using 24 transistors (12 NMOS and 12 PMOS). This type of adder works very slowly and consumes high amount of power. Both the sum and carry have the same value of delay. The full adder designed in GDI logic is constructed using 10 transistors (5 NMOS and 5 PMOS). It is the most efficient circuit design in terms of area as it requires only 10 transistors.

3. Simulation Results and Discussion

The simulation of various adder circuits were carried out using Spectre simulator. Key circuit metrics like dynamic power, static power, leakage power and delay were calculated for every 25°C change in temperature (-25°C to 125°C).

For analysis purposes, the performance metrics like dynamic power, static power (all inputs at logic high), static power (all inputs at logic low), leakage power (all inputs at logic high), leakage power (all inputs at logic low), delay and power delay product of all the design styles are compared over a range of temperatures and illustrated in a graphical manner in Figures 1, 2, 3, 4, 5, 6, 7 respectively.

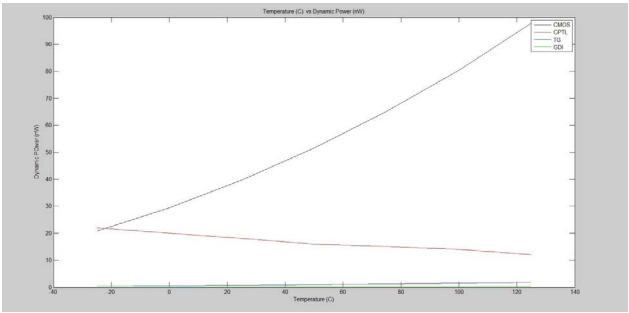

Figure 1. Dynamic power of 1-bit full adder.

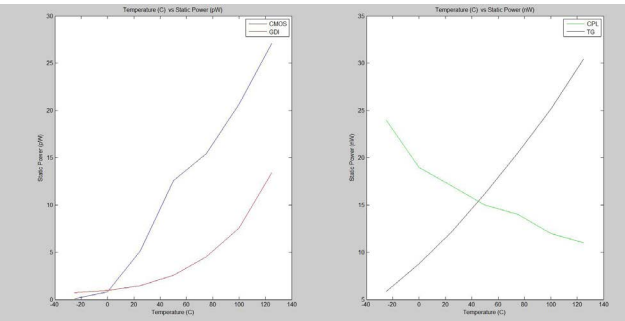

Figure 2. Static power (all inputs at logic high) of 1-bit full adder.

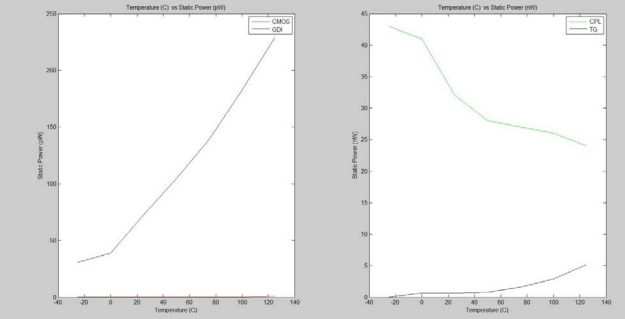

Figure 3. Static power (all inputs at logic low) of 1-bit full adder.

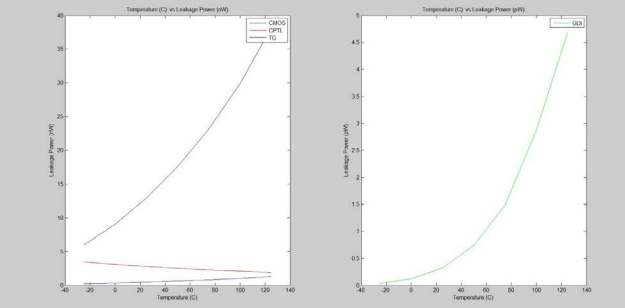

Figure 4. Leakage power (all inputs at logic high) of 1-bit full adder.

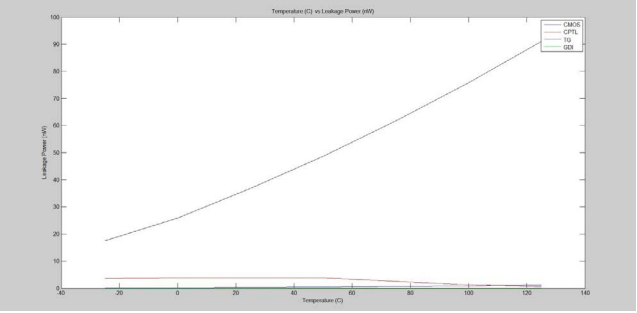

Figure 5. Leakage power (all inputs at logic low) of 1-bit full adder.

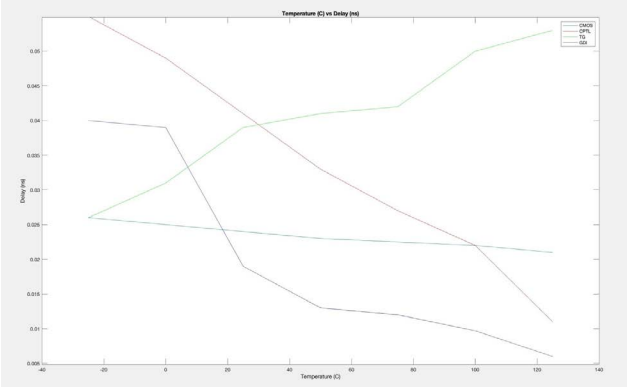

Figure 6. Delay of 1-bit full adder.

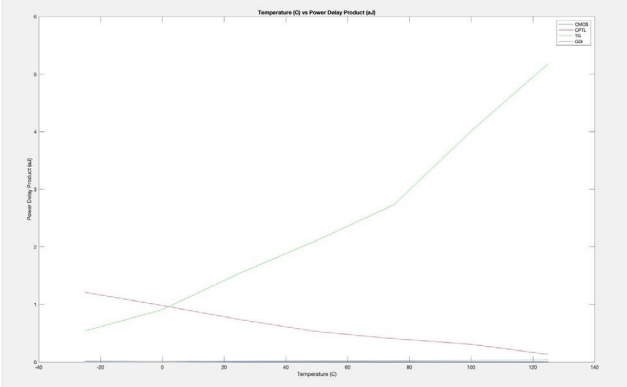

Figure 7. Power Delay Product of 1-bit full adder.

For comparative analysis, the average value for all the circuit metrics over the range of temperatures are tabulated. The following can be inferred from Table 1.

- The GDI logic adder provides 74%, 98.4% and 99.5% reduction in dynamic power when compared to the CMOS, CPTL and TG logic design respectively.
- The GDI logic adder provides 99.91%, 99.99% and 99.99% reduction in static power (all inputs at logic low) when compared to the CMOS, CPTL and TG logic design respectively.
- The GDI logic adder provides 91.8%, 98.3% and 99.9% reduction in leakage power (all inputs at logic low) when compared to the CMOS, CPTL and TG logic design respectively.
- The GDI logic adder provides 60%, 99.99% and 99.99% reduction in static power (all inputs at logic high) when compared to the CMOS, CPTL and TG logic design respectively.
- The GDI logic adder provides 99.8%, 99.9% and 99.99% reduction in leakage power (all inputs at

Table 1. Comparison of average values circuit metrics

Logic Style	Dynamic Power	All Inputs Low		All Inputs High		Delay	Power Delay Product
		Static Power	Leakage Power	Static Power	Leakage Power		
	(nW)	(nW)	(nW)	(nW)	(nW)	(ns)	(aJ)
CMOS	1.022	0.113	0.582	0.011	0.69	0.023	0.022
CPTL	16.7	31.5	2.79	16	2.601	0.034	0.59
TG	54.95	1.701	51.08	17.03	19.53	0.04	2.43
GDI	0.265	0.00016	0.048	0.004	0.0014	0.019	0.005

logic high) when compared to the CMOS, CPTL and TG logic design respectively.

- The GDI logic adder provides 17.4%, 44.1% and 52.5% reduction in delay when compared to the CMOS, CPTL and TG logic design respectively.
- The GDI logic adder provides 77.3%, 98.2% and 99.8% reduction in power delay product when compared to the CMOS, CPTL and TG logic design respectively.

4. Conclusion

In this study, different full adder structures were designed using FinFET 32nm technology. The FinFET technology was employed for the purpose of designing low power and high speed circuits below sub nanometer technology. A 1-bit adder was designed and simulated using CMOS, CPTL, TG, GDI logic and was used as a test circuit. Based on the observations, the GDI based FinFET adder exhibited minimum and excellent tradeoff in all the circuit metrics compared to other circuit designs. These simulations also show that the number of transistors required for designing the adder in GDI is very much less than other designs.

Therefore from the comparison results, we can infer that the GDI technique is one of the advantageous alternatives for designing combinational circuits. I believe that the presented results will promote further research work on GDI technique.

5. References

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