A High Gain Low Noise Figure Double Balanced Down Conversion Mixer for Band 1 of WiMedia System

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Abstract

Objective: To propose an improved double balanced down conversion mixer for band 1 of WiMedia system at RF frequency of 3.432 GHz and IF frequency of 264 MHz. **Method/Analysis**: The proposed mixer is based on the Gilbert cell architecture. It uses switch bias technique to improve the noise figure and resistive current injection technique to improve the conversion gain and linearity. A resonating inductor is used to cancel out the effects of parasitic capacitances. Moreover, T type impedance matching, LC impedance matching and output buffer are used at RF trans conductance stage, LO switching stage and load stage respectively for matching purpose. Mixer is simulated in 0.18 μm CMOS technology using keysight Advanced Design System (ADS) software. **Findings**: Simulation results show that mixer achieves maximum conversion gain of 8.057 dB, third order Input Intercept Point (IIP3) of -10.88 dBm, Double Sideband (DSB) noise figure of 3.515 dB and S₁₁ of -22.926 dB at 1.8 V dc supply voltage. **Novelty/Improvement:** A high gain, low noise figure double balanced down conversion mixer with low value of input reflection coefficient and suitable linearity is proposed for band 1 of Wimedia system.

Keywords: Current Injection Technique, Double Balanced, Down Conversion Mixer, L and T Type Matching Networks, Switch Bias Technique, Wimedia System

1. Introduction

WiMedia system provides an ISO-published radio standard for high-speed, ultra-wideband wireless personal area network. This technology is accepted by industries for wireless USB and high-speed bluetooth applications¹. This standard uses 3.1–10.6 GHz unlicensed frequency spectrum. This spectrum spans into 14 bands, each with a bandwidth of 528 MHz Band 1 ranges from 3.168 GHz to 3.696 GHz with center frequency of 3.432 GHz².

This paper presents the design of down-conversion mixer for band 1 of WiMedia system. In literature various mixer topologies are reported^{3–7} but among them Gilbert cell architecture is most preferred due to its advantages as double balanced feature, which results in good port to port isolation and low even order distortion due to its differential pair architecture^{8–11}.

Schematic of double balanced Gilbert cell mixer is shown in Figure 1, in which transistors M1 and M2 work as a transconductance stage which convert differ-

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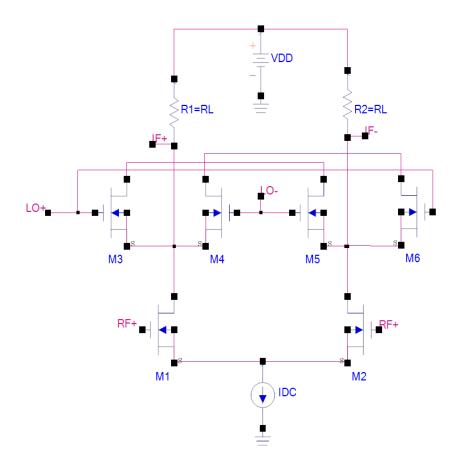


Figure 1. Double balanced Gilbert cell mixer.

ential input RF signal voltage to differential RF current. Transistors M3–M6 work as a differential switch controlled by differential LO signal. In this manner RF signal is periodically switched with LO frequency which results in mixing operation of RF and LO signals.

Load resistors R_L convert differential output IF current to differential output IF voltage.

Voltage conversion gain $(A_{\rm V})$ of the mixer is given as $A_{\rm V}=$ Amplitude of IF voltage/Amplitude of RF voltage as expressed by Equation (1).

$$A_{V} = \frac{\frac{4}{\pi} I_{RF} R_{L}}{2V_{RF}} = \frac{2}{\pi} g_{m} R_{L}$$
 (1)

Where g_m is the transconductance of transistors M1

and M2. R_L is the load resistance.

2. Proposed Work

In RF Integrated circuits design, there is trade off among different design parameters³. Main design objectives for receiver are high conversion gain and low noise figure with low vale of input reflection coefficient so main focus of this work is to propose a mixer for WiMedia receiver with high conversion gain, low noise figure and low value of input reflection coefficient with suitable linearity.

Figure 2 shows schematic of proposed mixer without matching circuits at RF and LO ports.

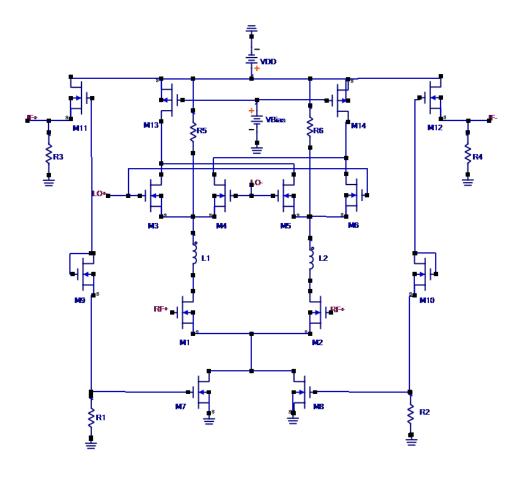


Figure 2. Proposed mixer without matching circuits at RF and LO ports.

In proposed mixer, transistor M7 and M8 works as switch bias transistors. Initially switch bias technique is proposed for reducing MOSFET flicker noise in oscillator design¹². Further this technique is adapted for mixing operation for a Direct Conversion Receiver (DCR) of UWB system¹³ and heterodyne receiver of wireless LAN system¹⁴. In proposed mixer circuit, diode connected transistors (M9, M10) provide proper gate bias for the switch bias transistors (M7, M8). Each of the transistors M7 and M8 are switched periodically between an active and passive state, which results in low flicker noise¹⁴.

 g_m of the trans conductance stage transistors is given by Equation (2).

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DC}}$$
 (2)

Where I_{DC} is the bias current through transconductance stage. So conversion gain in terms of ${\cal I}_{D\!C}$ is given by Equation (3).

$$A_{\nu} = \frac{2}{\pi} \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DC}} R_L \tag{3}$$

IIP3 (Third order input intercept point) is the parameter of the mixer to estimate the linearity performance of the mixer in terms of intermodulation distortion. IIP3 of the mixer is given by Equation (4).

$$A_{IIP3} = \sqrt{\frac{6I_{DC}}{\mu_n C_{ox} \frac{W}{L}}} \tag{4}$$

Equation (1) and Equation (4) implies that conversion gain and IIP3 of the mixer can be improved by increasing the bias current flowing through the RF transconductance stage transistors M1 and M2 but if the bias current is increased arbitrarily then it results in lesser

voltage headroom at the load stage¹⁵ as indicated by Equation (5).

$$V_{ds} = V_{bias} - I_{ds} R_L \tag{5}$$

If I_{ds} at the load increases, V_{ds} decreases which results in lesser voltage headroom at the active devices. Less headroom may distort the signal during negative half of input RF signal.

To solve this problem, current injection technique as a constant current source is used in literatures 14-16. Use

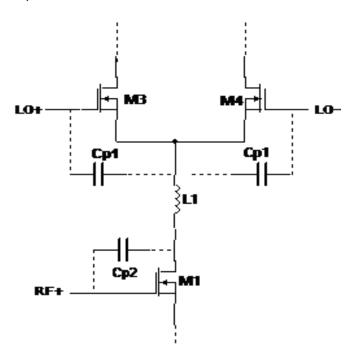


Figure 3. Tuning of added inductance with parasitic capacitances.

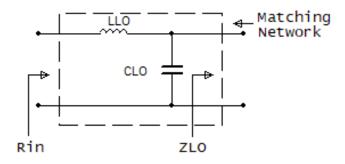


Figure 4. LC matching circuit used at LO stage.

of constant current source for current bleeding requires many design restrictions to be simultaneously satisfied¹⁵. A resistive current injection technique is used in the proposed mixer by injecting the additional bias current to the RF transconductance stage transistors, bypassing the load and LO switching stage through resistors R5 and R6. By this technique, the bias current at RF stage is increased without disturbing the current through the load stage, which results in better conversion gain and IIP3 without decreasing the voltage headroom.

In the proposed mixer, an inductance is added in series with RF and LO stage to cancel out parasitic capacitance¹⁷. Added inductances L1 and L2 make a pi type matching network by combining parasitic capacitances at the source of LO transistor and drain of RF transistors which results in better tuning of the mixer. Figure 3 shows the forming of pi type network with C_{p_1} , L1 and C_{p_2} , where $C_{_{\!\scriptscriptstyle D1}}$ is the gate to source parasitic capacitance of each of the LO transistors (M3, M4) and C_{p2} is the drain to gate parasitic capacitance of RF transcondutance stage transistor M1. Similarly, L2 inductance cancels out the parasitic capacitances of transistors (M5, M6) and M2.

In case of resistive load, the gain of the mixer can be increased by increasing R_L as indicated by Equation (1) but it also results in lesser headroom as depicted by Equation (5). In the proposed mixer, a constant current source M13 and M14 is used in place of resistive load. The

conversion gain of the mixer with constant current source is given by Equation (6).

$$A_{v} = \frac{2}{\pi} g_{m} \left(r_{o1} \| r_{o2} \right) \tag{6}$$

Where r_{o1} and r_{o2} are the output resistances of load transistors (M13, M14) and transconductance stage transistors (M1, M2), respectively, which implies that gain of the circuit is less dependent on load resistance R_L hence voltage headroom is less disturbed. Final IF output is taken at the source of common drain buffer stage transistors (M11-M12). Buffer Stage is used for impedance matching at load stage.

Two element LC matching is used at the LO stage as shown in Figure 4. Use of LC matching does not allow flexibility for choosing quality factor Q or bandwidth of the signal but this is not the issue at LO stage as LO signal does not carry any information and it acts only as switching signal for LO stage transistors. Further LC matching is simpler than three elements matching as it uses only two elements for matching purpose.

For impedance matching of RF port, three element T matching is used as shown in Figure 5. Three element type matching provides flexibility in choosing quality factor which is essential for matching of input RF signal.

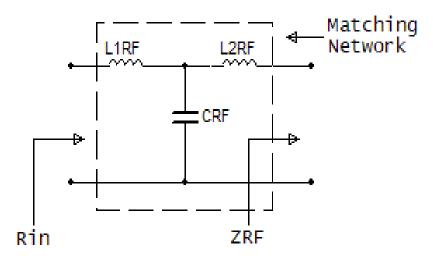


Figure 5. T matching circuit used at RF stage.

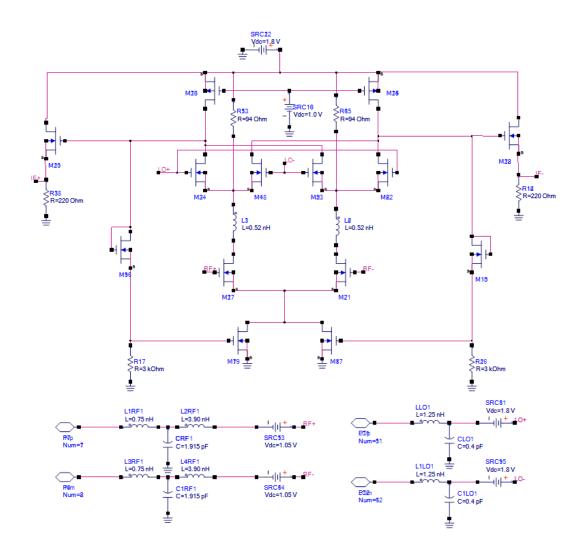


Figure 6. Proposed mixer after accommodating matching circuits at RF and LO ports.

Complete schematic of proposed mixer circuit after accommodating matching circuits at LO and RF port is shown in Figure 6.

3. Simulation Results

The proposed mixer is simulated using ADS software with 0.18 μ m CMOS process technology with 0 dBm LO power at 1.8 V DC supply voltage. RF frequency (f_{RF}) is taken equals to centre frequency of band 1 that is equal to 3.432 GHz. As per WiMedia recommendations, the

receiver sensitivity for 1024 Mb/s should be -63.5 dBm^2 . So input RF power (P_RF) is varied from -63.5 dBm to higher values to observe the gain compression phenomenon. Typical overall gain of front end RF filters and Low noise Amplifier (LNA) placed prior to mixer in receiver, is assumed as 8 dB¹⁸ so operating RF input power level for mixer simulation is chosen as -55.5 dBm (-63.5 dBm + 8 dBm), accommodating overall gain of front end filters and LNA.

Recommended channel bandwidth for WiMedia UWB system is 528 MHz so IF frequency is chosen equal

to half of channel band width *i.e.* 528/2 = 264 MHz. LO frequency (f_{LO}) in terms of RF frequency is given by Equation (7).

$$f_{LO} = f_{RF} \pm f_{IF} \tag{7}$$

Higher LO frequency is chosen as it provides better (lower) tuning range of LO. LO frequency is calculated as given by Equation (8).

$$f_{LO} = 3.432 \text{ GHz} + 264 \text{ MHz} = 3.696 \text{ GHz}$$
(8)

Simulated conversion gain as function of input RF power level as a result of gain compression simulation is shown in Figure 7. Conversion gain remains constant for lower values of input RF power level and gain starts decreasing at higher values of input RF power level, this is a very typical phenomenon in RF circuits, known as gain

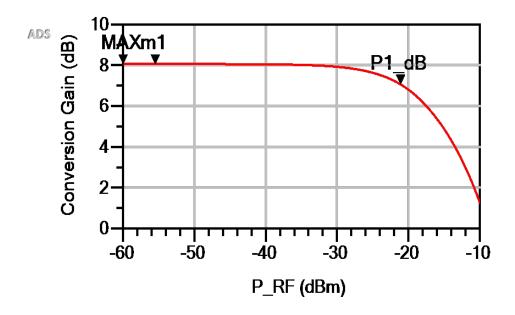


Figure 7. Simulated conversion gain versus input RF power (P_RF).

compression and it is very well validated by simulation results.

Mixer achieves flat maximum conversion gain as 8.057 dB at −60 dBm to −30 dBm input RF power levels. Linearity of the proposed mixer is measured with the parameter P1dB. It is defined as the input RF power level at which gain is reduced by 1dB from the linear (maximum) gain. P1dB of the proposed mixer is equal to −21.1 dB as shown in Figure 7. This value of P1dB is 34.4 (-21.1+55.5) dB away from operating power level (-55.5 dB) of RF input signal. This indicates that mixer shows linear behavior for large range of input power levels in terms of WiMedia specifications.

Variation of the ideal and simulated IF output power level (PIF) versus input RF power level (P_RF) as shown in Figure 8. It shows that simulated output IF power level starts decreasing at higher values of input RF power level, which is another validation of gain compression phenomenon in proposed mixer.

Variation of conversion gain versus input RF frequency is shown in Figure 9, which revalidate the value

of conversion gain of 8.057 dB at input RF frequency of 3.432 GHz. The value of conversion gain at lower and higher end of frequencies of band 1 of WiMedia system is 6.235 dB and 3.738 dB respectively.

Output IF power spectrum is shown in Figure 10. Output spectrum shows power of -47.443 dBm at required fundamental IF frequency of 264 MHz. This result is also in agreement with gain compression simulation results as observed in Figures 7 and 9 as value of conversion gain obtained at -55.5 dBm input RF power and at RF frequency of 3.432 GHz is 8.057 dB so output IF power =Input RF power level (-55.5 dBm) + conversion gain (8.057) = -47.443 dBm.

Proposed mixer shows third harmonic at 792 MHz at a power level of -200 dBm. This harmonic does not interfere much with desired IF frequency component as it is 152.557 dB (200-47.443) below the power level of fundamental IF component and also it is located well outside the frequency of operation of mode 1. Mixer shows no

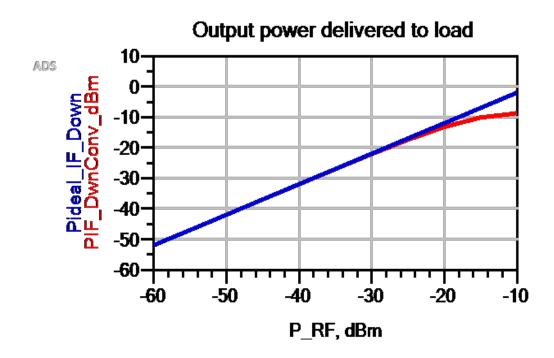


Figure 8. IF output power level (PIF) versus input RF power level (P_RF).

(highly reduced level of) second (even) harmonic due to its double balanced differential configuration.

For Intermodulation Distortion (IMD) simulation of the mixer, two RF frequencies should be chosen such that resultant third order intermodulation (IM) products, after mixing should lie within the IF bandwidth. For IMD simulation of proposed mixer, the two input RF frequencies are chosen as $f_1 = f_{RF} + f_{spacing}/2$ and $f_2 = f_{RF} - f_{spacing}/2$ with a spacing of $f_{spacing} = 50$ KHz. Two third order IMD frequencies generated are f_{USB} (upper side band third order IM product) $= 2f_1 - f_2$ and f_{LSB} (lower side band third order IM product) $= 2f_2 - f_1$. Two third order IM mix products thus generated are $f_{USB} - f_{LO} = 264.1$ MHz and $f_{LSB} - f_{LO} = 264.1$

= 263.9 MHz, which lie within the IF bandwidth as they are very close to required IF frequency of 264 MHz.

Third order Input Intercept Point (IIP3) is parameter to evaluate the linearity performance of the mixer in terms of IMD. IIP3 is the input power level corresponding to the point of intersection of linearly extrapolated values of IF power level and third order IM products power level. Results of IMD simulation of the proposed mixer are shown in Figure 11, which shows IIP3 of the proposed mixer as -10.880 dBm.

Simulation of Single Side Band (SSB) noise figure of the mixer versus input RF frequency is shown in Figure

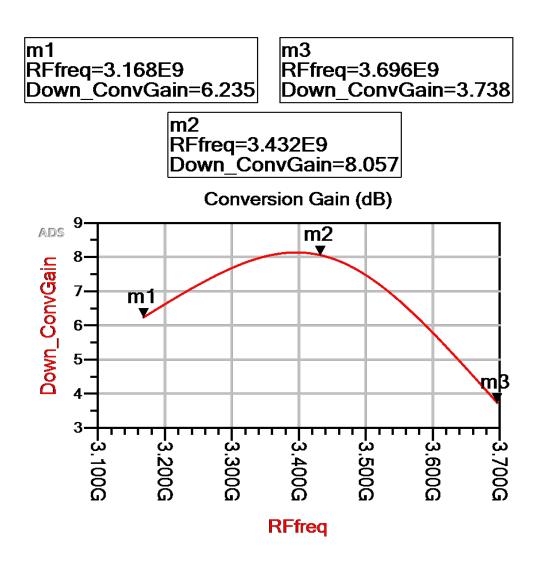


Figure 9. Simulated conversion gain versus input RF frequency.

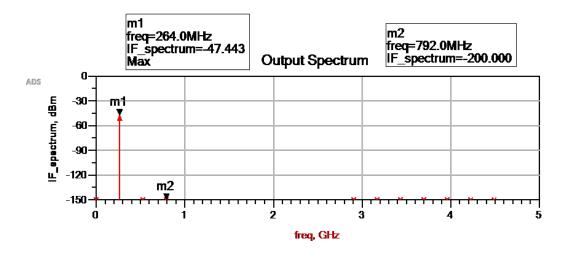


Figure 10. Simulated output IF power spectrum.

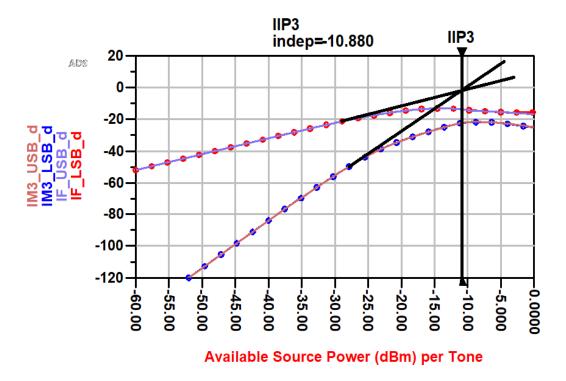


Figure 11. Simulated results of two tone IMD simulation.

12, which shows SSB noise figure of the proposed mixer as 6.515 dB at 3.432 GHz input RF frequency.

DSB noise figure of the mixer is 3 dB less than the SSB noise figure so DSB noise figure of the mixer is 6.515 - 3 =3.515 dB at 3.432 GHz input RF frequency

Input reflection coefficient of mixer is measured in terms of S₁₁ scattering parameter. Simulated result of S₁₁ of the proposed mixer is shown in Figure 13, which shows the value of S_{11} as -22.926 dB at the desired RF frequency of 3.432 GHz. $\boldsymbol{S}_{\scriptscriptstyle{11}}$ of the proposed mixer is well below the

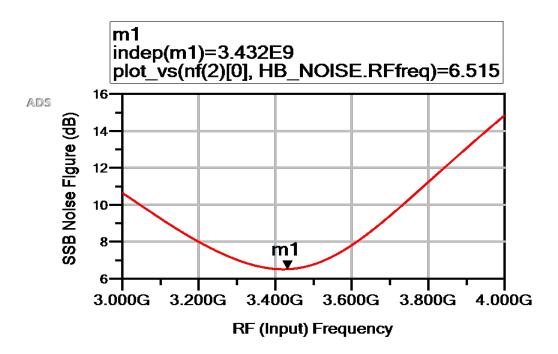


Figure 12. Simulated SSB noise figure versus input RF frequency.

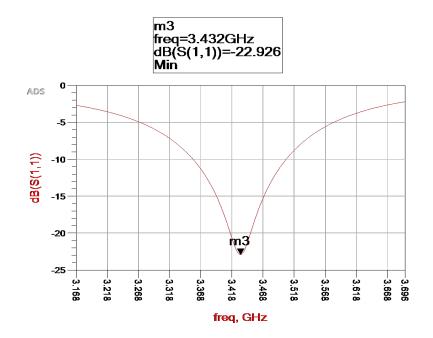


Figure 13. Simulated S_{11} of the proposed mixer.

minimum accepted value of -10 dB, which indicates that the proposed mixer is properly matched at RF port.

Simulated results of the transient analysis of the output IF frequencies (IF+ and IF-) of the proposed mixer are shown in Figure 14. Transient waveform shows some

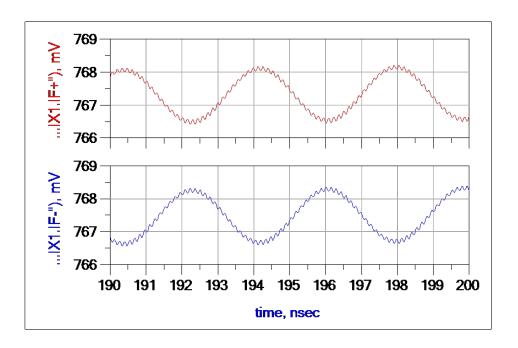


Figure 14. Transient analysis of output IF.

Table 1. Performance summary and comparisons of the proposed mixer with other state of the art works

Ref.	Techno- logy CMOS (μm)	Supply Voltage (V)	RF Frequency (GHz)	IF Frequency (MHz)	Conversion Gain (dB)	IIP3 (dBm)	Noise figure (dB)	S ₁₁ (dB) (min.)
14	0.18	1.8	5.8	100	7.5	-5	7.6 (DSB)	_
6	0.18	1	1-6	100	7	0	13.5	_
9	0.18	0.8	0.2-13	264	9.9	-10	11.7 (DSB)	_
10	0.18	0.5	3.1-3.628	528	2.17-3.25	-5.71	5.12-5.93	~ -12
7	0.18	0.8	6-10	100	6.4±2.8	-1.3	21.8 (min)	~ -19
11	0.13	1.2	1-10	100-1000	3~8	<i>-7</i> ∼ <i>-4</i>	11.3~15	~ -16
This Work	0.18	1.8	3.432	264	8.057	-10.88	3.515 (DSB)	-22.926

jitter due to noise effect but no clipping is observed in the waveform which indicates avaiabilty of sufficient headroom across the transistors.

Results of the mixer are summerized and compared with other state of art works as shown in Table 1. It can be seen that propsed mixer achieves a high conversion gain and low value of noise figure with a very low value of S_{11} .

4. Conclusion

This paper presents a design of down converter mixer for heterodyne receiver for band 1 WiMedia system at RF frequency of 3.432 GHz and IF of 264 MHz. Mixer is simulated in 0.18 µm CMOS technology using keysight ADS software with 1.8 V dc supply voltage. Mixer achieves a high conversion gain of 8.057 dB and suitable linearity in terms of P1dB of -21.1 dBm and IIP3 of -10.88 dBm as a consequence of use of current injection technique. Use of switch bias technique enables the mixer to achieve a low value of DSB noise figure of 3.515 dB. A very low value of S₁₁ of -22.926 dB at RF frequency of 3.432 GHz indicates that proposed mixer is suitably matched at input RF port using T type matching network. Resonating inductor is used to cancel the effect of parasitic capacitances for better tuning of the mixer. So the proposed mixer is useful for RF front end receiver for band 1 WiMedia system.

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