ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645
Indian Journal of Science and Technology, *Vol 11(5), DOI: 10.17485/ijst/2018/v11i5/117302, February 2018*

A Simulated Annealing-based Optimization Approach for Minimizing the THD in Asymmetric Cascaded Multilevel Inverter

José Araque*, Ramón Alvarez and Javier E. Sierra

Faculty of Engineering, Universidad de Sucre, Cra. 28 # 5-267, Sincelejo, Colombia;
jose.araque@unisucre.edu.co, ramon.alvarez@unisucre.edu.co, javier.sierra@unisucre.edu.co

Abstract

Objectives: This paper focuses on the reduction of harmonic content in the voltage output waveform of a 31 level asymmetric monophasic cascaded multilevel inverter using the Simulated Annealing Optimization (SAO) algorithm. **Method**: The SAO algorithm was used to find the appropriate switching angles for the stages of the converter using MATLAB. First, the technique employed was simulated and evaluated; then, a prototype of the multilevel inverter was developed for validating the results obtained in simulation. **Findings**: The output waveform, the harmonic profile graphic, and THD evolution were obtained both the simulation and the prototype. The SAO algorithm allowed to calculate the appropriate switching angles for the asymmetric multilevel inverter, permitting to obtain a low THD (less than 5%), using a relatively low number of semiconductors compared with the symmetric topology. The SAO algorithm also allowed finding the solution of transcendental equations system through a heuristic approach, avoiding the local minima problem presented in traditional methods. **Novelty /Improvement:** The proposed method (SAO) avoids the potential issues with local minima present in traditional methods for the switching angles computation in cascaded multilevel inverters.

Keywords: Multilevel Inverter, Simulated Annealing, THD

1. Introduction

Nowadays the conversion of DC sources as battery banks, photovoltaic panels and fuel cells among others, in an AC output waveform is a critical process that requires the use of inverter circuits with high efficiency in the conversion process. The conventional inverters possess many disadvantages such as high Total Harmonic Distortion (THD), high voltage change rates (dv/dt), high switching stress and ElectroMagnetic Interferences (EMI). In recent years multilevel inverters have become an alternative to traditional two and three level inverters, especially in low and mid power applications due to having the capability of operating at high power using the medium voltage rated switches. The general concept behind of multilevel inverters involves a large number of switches based on power semiconductors such as MOSFET or IGBT that transform the electrical energy provided by direct voltage sources into small steps, achieving an AC waveform with a low

**Author for correspondence*

harmonic content[1,2]. There are three major topologies of a multilevel inverter: the Neutral Point Clamped (NPC) which was patented in 1980[3], Flying Capacitor (FC) multilevel inverter, created in the 90's[4], and Cascaded multilevel inverter or Cascaded H Bridge (CHB), developed in 1975[5]. Between these topologies, the cascaded multilevel inverter is the most used today because of its low number of switches compared with other inverters, besides, the CHB inverter is more "modular" and expandable than others[1]. Nevertheless, one of the drawbacks of multilevel inverters is the need to compute the switching angles of the power semiconductors, because of the complexity of its commutation schemes and the major number of switches than traditional inverters. In the calculation of switching angles, a transcendental equation system must be resolved[6]. Some iterative methods as Resultant Theory and Newton Raphson are commonly employed and have been widely studied[7–13]. The issue with these methods is that it does need good initial guess and might not converge at some points, causing a problem of local minima. The heuristic based methods (Genetic Algorithms, Particle Swarm Optimization, Simulated Annealing among others) offer an interesting alternative for solving the issue of finding the solutions of the transcendental equations because allow to see it as an optimization problem. Various of these methods have been used successfully[14–18].

In this work, the Simulated Annealing Optimization method is used to find the optimal solution to transcendental equation system that allows obtaining the switching angles for power semiconductors in a 31 level converter, reducing the THD to less than 5% (IEEE 519-1992 normative). The paper is organized as follows: Section 2 describes the 31 levels cascaded multilevel inverter with asymmetric topology. Section 3 discusses the Simulated annealing algorithm. Section 4 deals with optimization problem statement. Section 5 gives the simulation results and prototype followed by the conclusion.

2. 31 Level Asymmetric CHB Multilevel Inverter

Figure 1 shows the general scheme of monophasic CHB multilevel inverter. Each stage of the inverter has an independent DC power supply. Depending on the voltage of these power supplies and the appropriate commutation scheme, we can have two possibilities: Symmetric and Asymmetric converter.

If the value of power supplies is equal for every stage, the inverter is called "symmetric". The number of output levels can be found by:

$$N = 2s + 1 \qquad (1)$$

where, N is the number of output levels and s is the number of stages. For example, in Figure 1, if the power supplies are the same for each stage (i.e. Vcc1=Vcc2=Vcc3=Vcc4=Vcc), it is possible to obtain N=9 output levels. Figure 2 shows the typical output waveform in blue and the fundamental harmonic in red, whereas Table 1 shows the switching pattern of this configuration for a half cycle. The other half cycle can be easily obtained by the symmetry of the sine wave.

On the other hand, if the power supplies are conveniently different, it is possible to achieve a major number of levels using the same number of semiconductors that the symmetric case. If the proportion between a power supply and the previous one is 2:1, i.e. if *Vccn=2Vccn-1*, the inverter is called "asymmetric". The number of output levels can be determined by:

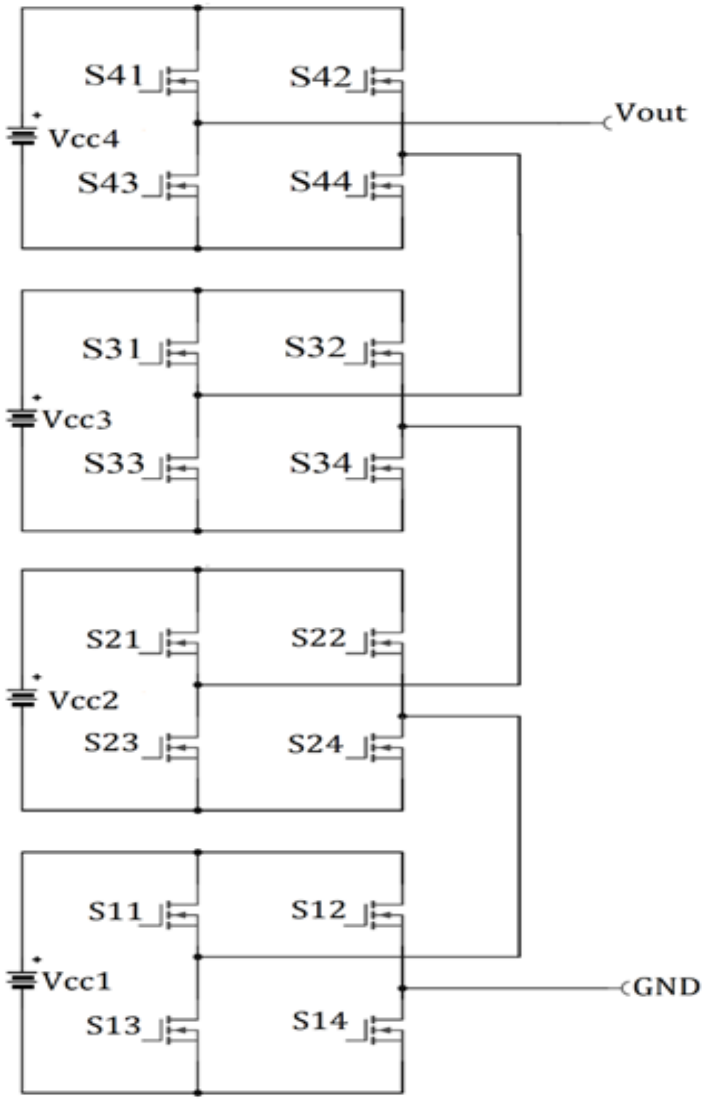

Figure 1. Four stage monophasic CHB multilevel inverter.

$$N = 2^{s+1} - 1 \quad (2)$$

where, N is the number of output level and s is the number of stages. For example, in Figure 1, if the power supplies have 2:1 ratio (i.e. Vcc2=2·Vcc1, Vcc3=2·Vcc2, and Vcc4=2·Vcc3), it is possible to obtain N=31 output levels with the same number of the power semiconductor. Note that in this configuration, *Vcc4=8·Vcc1*. Figure 3 shows the typical output waveform in blue and the fundamental harmonic in red, whereas Table 2 shows the switching pattern of this configuration for a half cycle. The other half cycle can be easily obtained by the symmetry of the sine wave.

As can be seen in Table 2, the asymmetric configuration allows obtaining a staircase waveform very close to the sinusoidal waveform as long as the power semiconductors on each stage get fired in the precise angle (or time). This angles can be found in many ways. The

Table 1. Switching pattern for the four stage CHB Symmetric multilevel inverter

Stage 1 On switches	Stage 2 On switches	Stage 3 On switches	Stage 4 On switches	Output level
S13, S14	S23, S24	S33, S34	S43, S44	0V
S11, S14	S23, S24	S33, S34	S43, S44	+Vcc
S11, S14	S21, S24	S33, S34	S43, S44	+2Vcc
S11, S14	S21, S24	S31, S34	S43, S44	+3Vcc
S11, S14	S21, S24	S31, S34	S41, S44	+4Vcc
S11, S14	S21, S24	S31, S34	S43, S44	+3Vcc
S11, S14	S21, S24	S33, S34	S43, S44	+2Vcc
S11, S14	S23, S24	S33, S34	S43, S44	+Vcc
S13, S14	S23, S24	S33, S34	S43, S44	0V

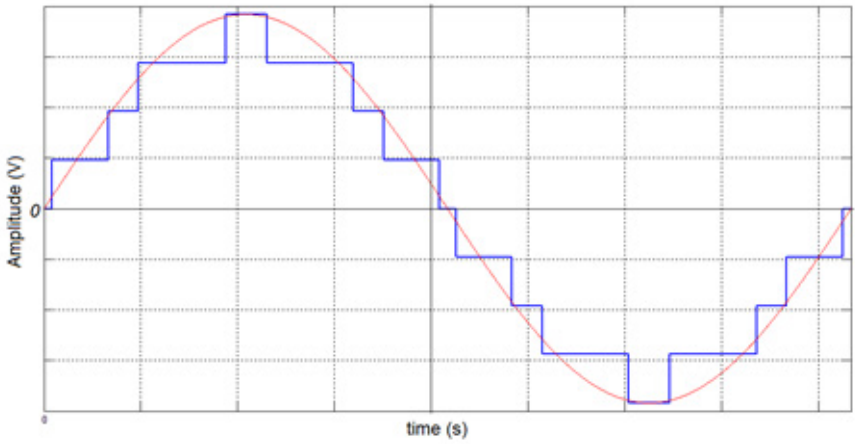

Figure 2. Typical output for the four stage CHB Symmetric multilevel inverter.

most common method is called Selective Harmonic Elimination (SHE)[19], that consists in to solve a transcendental equation system, which describes mathematically the staircase waveform and whose solution gives us the angles of the firing of the power devices. The output voltage waveform is stepped as shown in Figure 2 and Figure 3 and can then be expressed as:

$$Vout = \sum_{n=1}^{\infty} \frac{4Vcd}{n\pi} \left[\sum_{k=1}^{s} cos(n\theta_k) \right] sen(n\omega t) \quad (3)$$

Table 2. Switching pattern for the four stage CHB Asymmetric multilevel inverter

Stage 1 On switches	Stage 2 On switches	Stage 3 On switches	Stage 4 On switches	Output level
S13, S14	S23, S24	S33, S34	S43, S44	0V
S11, S14	S23, S24	S33, S34	S43, S44	+Vcc
S13, S14	S21, S24	S33, S34	S43, S44	+2Vcc
S11, S14	S21, S24	S33, S34	S43, S44	+3Vcc
S13, S14	S23, S24	S31, S34	S43, S44	+4Vcc
S11, S14	S23, S24	S31, S34	S43, S44	+5Vcc
S13, S14	S21, S24	S31, S34	S43, S44	+6Vcc
S11, S14	S21, S24	S31, S34	S43, S44	+7Vcc
S13, S14	S23, S24	S33, S34	S41, S44	+8Vcc
S11, S14	S23, S24	S33, S34	S41, S44	+9Vcc
S13, S14	S21, S24	S33, S34	S41, S44	+10Vcc
S11, S14	S21, S24	S33, S34	S41, S44	+11Vcc
S13, S14	S23, S24	S31, S34	S41, S44	+12Vcc
S11, S14	S23, S24	S31, S34	S41, S44	+13Vcc
S13, S14	S21, S24	S31, S34	S41, S44	+14Vcc
S11, S14	S21, S24	S31, S34	S41, S44	+15Vcc
S13, S14	S21, S24	S31, S34	S41, S44	+14Vcc
S11, S14	S23, S24	S31, S34	S41, S44	+13Vcc
S13, S14	S23, S24	S31, S34	S41, S44	+12Vcc
S11, S14	S21, S24	S33, S34	S41, S44	+11Vcc

Table 2 Continued

S13, S14	S21, S24	S33, S34	S41, S44	+10Vcc
S11, S14	S23, S24	S33, S34	S41, S44	+9Vcc
S13, S14	S23, S24	S33, S34	S41, S44	+8Vcc
S11, S14	S21, S24	S31, S34	S43, S44	+7Vcc
S13, S14	S21, S24	S31, S34	S43, S44	+6Vcc
S11, S14	S23, S24	S31, S34	S43, S44	+5Vcc
S13, S14	S23, S24	S31, S34	S43, S44	+4Vcc
S11, S14	S21, S24	S33, S34	S43, S44	+3Vcc
S13, S14	S21, S24	S33, S34	S43, S44	+2Vcc
S11, S14	S23, S24	S33, S34	S43, S44	+Vcc
S13, S14	S23, S24	S33, S34	S43, S44	0V

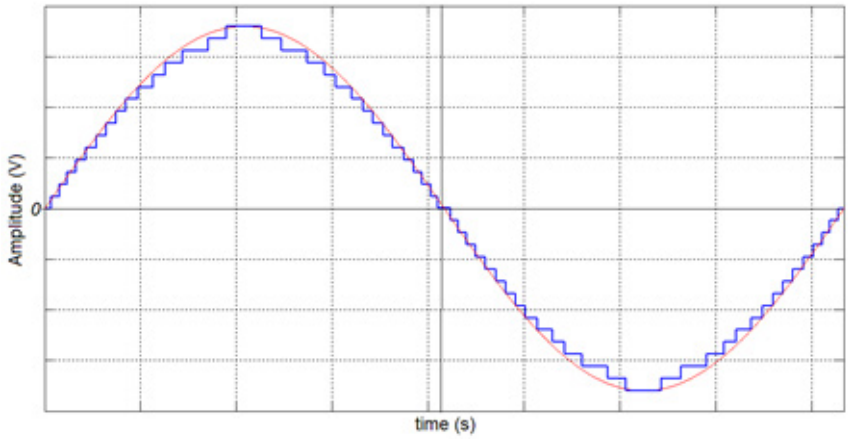

Figure 3. Typical output for the four stage CHB Asymmetric multilevel inverter.

where:

n is the odd harmonic order (1, 3, 5, 7, 9, …).

s is the inverter stages number.

k is a positive integer (1, 2, 3, 4, 5, …, s).

is the kth switching angle and must satisfy:

$$\theta_1 < \theta_2 < \ldots < \theta_1 < \pi/2 \quad (4)$$

From Equation (3), the amplitude of the odd harmonics, including the fundamental component can be expressed as:

$$h_n = \frac{4Vcd}{n\pi}\sum_{k=1}^{s}\cos(n\theta_k) \quad (5)$$

Expanding the above equation, we have:

$$h_n = \frac{4Vcd}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \quad (6)$$

The switching angles $\{\theta_1, \theta_2, \ldots, \theta_s\}$ can be selected such that the total harmonic distortion of voltage is minimal. The transcendental equation system generated by Equation (6) must be solved in such way that the fundamental harmonic (h_1) to be the desired value and all of the other harmonics to be equal 0. The multilevel inverter considered in this paper has a Vcc=12V, so Vcc2=24V, Vcc3=48V and, Vcc4=96V.

3. Simulated Annealing Optimization (SAO)

SAO is a probabilistic method proposed by Kirkpatrick, Gelett, and Vecchi in 1983[20], with the aim to find the global minima of a cost function which can have many local minima. SAO algorithm works by imitating a physical process by which a solid is cooled slowly until eventually its molecular structure is frozen and passes to minimal energy configuration.

The SAO algorithm starts with a random estimation of the values of the cost function variables. Heating allows modifying randomly the value of the variables. A higher heat implies best random variations. The cost function returns the output f, associated with a variable set. If the output decreases, then the new variable set replaces the old one. If the output increases, then the output is accepted, as long as[21]:

$$r \leq e^{[f(P_{old})-f(P_{new})]/T} \quad (7)$$

where, r is a random number and T is a representation of temperature. If the Equation (7) is not satisfied, then the new set of variables is rejected. Therefore, even if the new set of variables leads to a worse cost, this can be accepted with a certain probability. The new set of variables is found taken a random step from the old set of variables:

$$P_{new} = d \cdot P_{old} \quad (8)$$

where, d is uniformly distributed around of *Pold*. This control variable establishes the step size so that the beginning the algorithm is forced to make big changes in the value of the variables. Occasionally, the changes move the algorithm away for the optimal, which forces to the algorithm to explore new regions of the search space. After a certain number of iterations, the new sets of variables do not longer give place to more low costs. At this point, the values of T and d are decreased by a certain percentage and the algorithm is repeated. The algorithm is stopped when T=0. The decrement of T is called cooling schedule. There are many possibilities for the cooling schedule. If the initial temperature is T_0 and Tf is the final temperature, then the temperature in the n step is as follows:

$$T_n = f(T_0, T_N, N, n) \quad (9)$$

where, f is decremented with the time. Some cooling schedules are:

-Linearly decrescent:

$$T_n = T_0 - n(T_0 - T_N)/N. \quad (10)$$

-Geometrically decrescent:

$$T_n = 0.99T_{n-1} \quad (11)$$

-Hayjek optimal:

$$T_n = c/\log(1+n) \quad (12)$$

where, c is the smallest variation required to exit from a local minimum.

In the SAO algorithm, the temperature usually drops slowly so the algorithm has a chance to find the right minimum before to try to go to the lowest point of the search surface.

4. Optimization Problem Statement

As described in section 2, it is necessary to find the appropriate values of the firing angles θ_k that permit to obtain a stepped waveform similar to a sine wave. This can be seen as an optimization problem, where the SAO algorithm must minimize the THD satisfying the equation (4), reducing all the harmonic components h_n except the fundamental harmonic h_1, which is the component that interests us. So the optimization problem can be considered as follows:

To minimize:

$$THD\% = \sqrt{\left(\frac{1}{h_1^2}\right)\sum_{n=3}^{\infty}(h_n^2)} \cdot 100 \quad (13)$$

where:

h_1 is the fundamental harmonic amplitude.

h_n is the *nth* harmonic amplitude, for n odd.

Satisfying the transcendental equation system obtained from Equation (6) as follows:

$$\begin{cases} \cos(\theta_1 \cdot t) + \cos(\theta_2) + \cos(\theta_3) + \cdots + \cos(\theta_{15}) = m \\ \cos(3\cdot\theta_1) + \cos(3\cdot\theta_2) + \cos(3\cdot\theta_3) + \cdots + \cos(3\cdot\theta_{15}) = 0 \\ \cos(5\cdot\theta_1) + \cos(5\cdot\theta_2) + \cos(5\cdot\theta_3) + \cdots + \cos(5\cdot\theta_{15}) = 0 \\ \cos(7\cdot\theta_1) + \cos(7\cdot\theta_2) + \cos(7\cdot\theta_3) + \cdots + \cos(7\cdot\theta_{15}) = 0 \\ \cos(9\cdot\theta_1) + \cos(9\cdot\theta_2) + \cos(9\cdot\theta_3) + \cdots + \cos(9\cdot\theta_{15}) = 0 \\ \cos(11\cdot\theta_1) + \cos(11\cdot\theta_2) + \cos(11\cdot\theta_3) + \cdots + \cos(11\cdot\theta_{15}) = 0 \\ \cos(13\cdot\theta_1) + \cos(13\cdot\theta_2) + \cos(13\cdot\theta_3) + \cdots + \cos(13\cdot\theta_{15}) = 0 \\ \cos(15\cdot\theta_1) + \cos(15\cdot\theta_2) + \cos(15\cdot\theta_3) + \cdots + \cos(15\cdot\theta_{15}) = 0 \end{cases} \quad (14)$$

where:

$m = \frac{\pi \cdot V_1}{4 \cdot Vcc}$, V_1 is the peak amplitude of the fundamental and Vcc is the value of the power supply in the first stage of inverter.

subject to the following constraints:

$$h_1 = 169.7V$$

$$h_n = 0 \; for \; n > 1 \; odd$$

$$0 < \theta_1 < \theta_2 < \theta_3 < \cdots \theta_{15} < \pi/2$$

5. Simulation and Prototype

The optimization algorithm SAO was developed in Mat lab® and a model of the asymmetric multilevel inverter was implemented on Simulink as can be seen in Figure 4. The simulations were carried out to obtain the optimized parameters. To verify the simulation results, a prototype of the multilevel inverter was developed and the

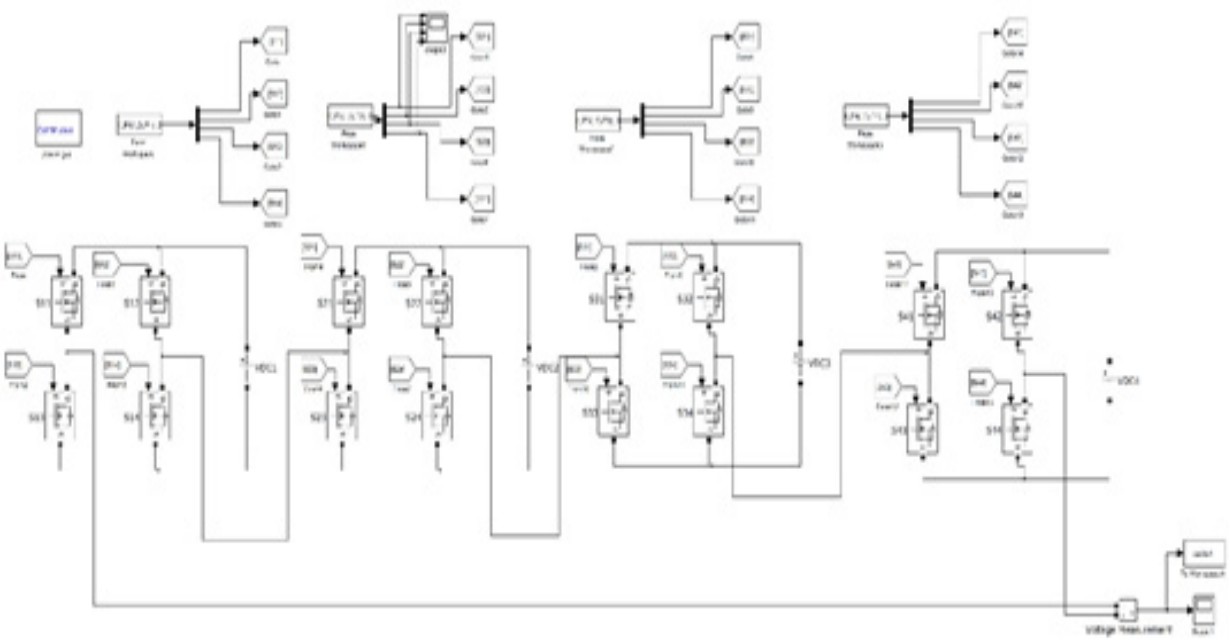

Figure 4. Simulink model of CHB multilevel inverter.

switching angles calculated by the SAO algorithm were programmed on a PIC18F4550 MCU. Figure 5 shows the block diagram of the developed system whereas Figure 6 shows the assembly of the experiment. A data acquisition system based on the Agilent DSO3202-A digital oscilloscope has been used to perform the visualization and analysis of the waveform obtained, as well as the measurement of the THD value.

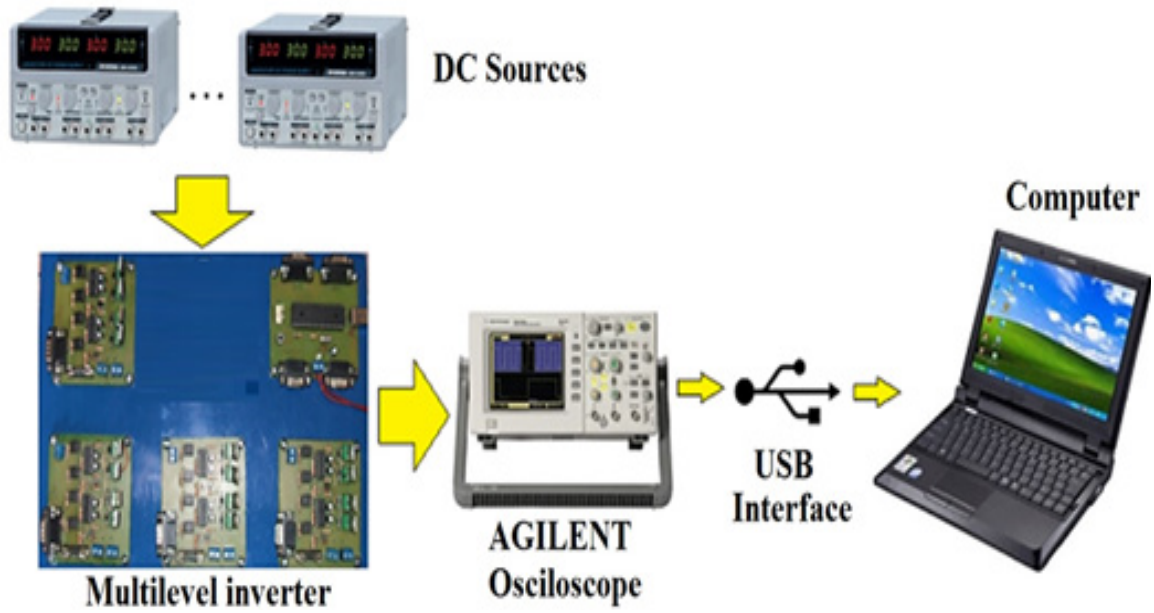

Figure 5. Block diagram of the prototype.

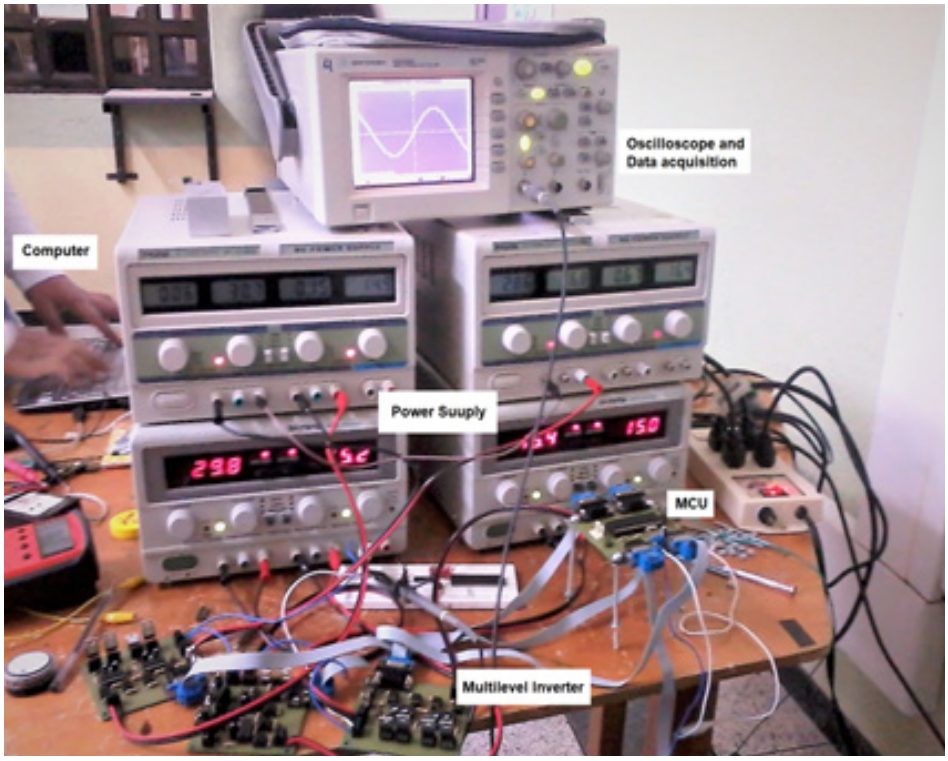

Figure 6. Experimental setup for 31 level CHB multilevel inverter.

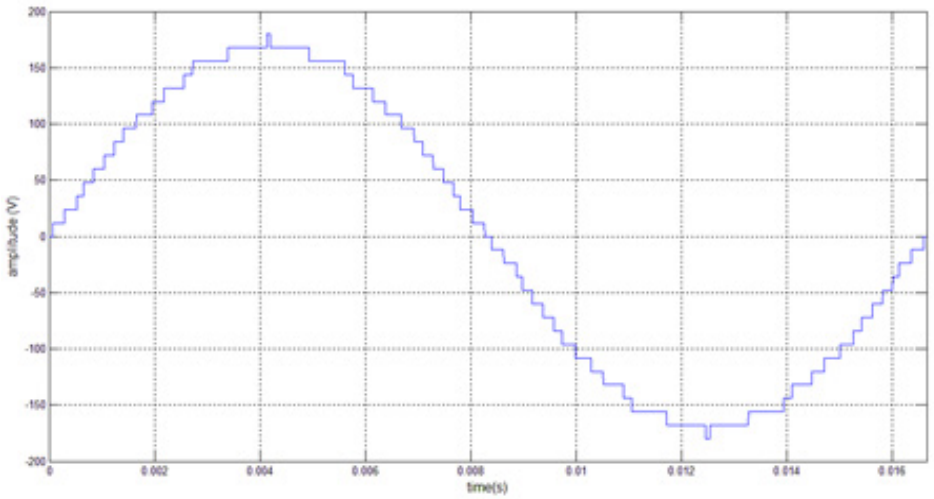

Figure 7. Simulated output waveform of the 31 level CHB asymmetric multilevel inverter.

Table 3 summarizes the optimal firing angles obtained by SAO algorithm (in degrees), whereas Figure 7 shows the output waveform of the 31 level asymmetric multilevel inverter with Vcc=12V, Vcc2=24V, Vcc3=48V, and

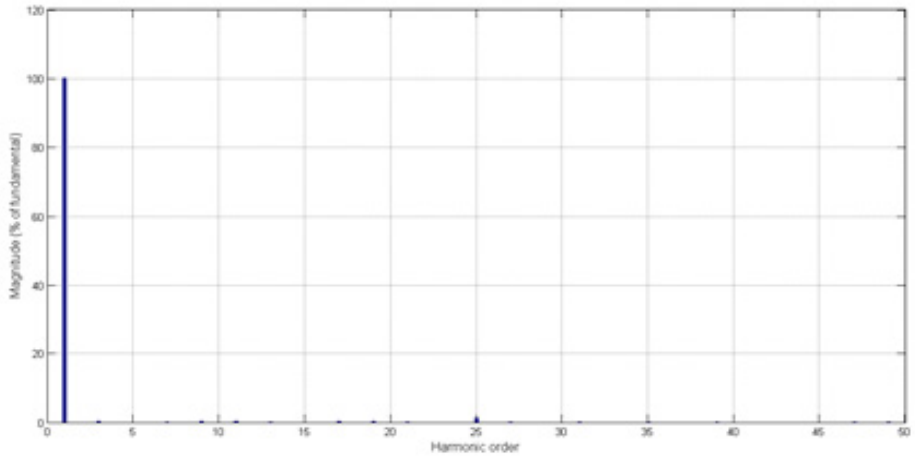

Figure 8. Harmonic profile of the simulated 31 level CHB asymmetric multilevel inverter.

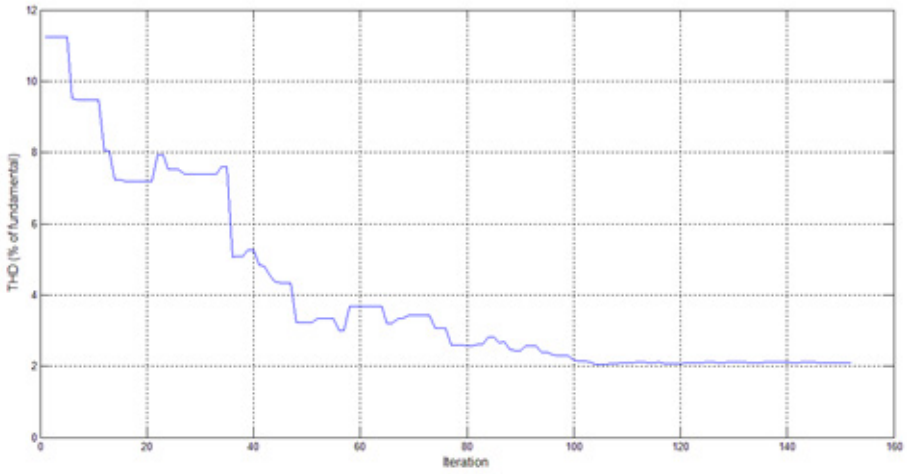

Figure 9. THD evolution vs. Iterations of SAO algorithm.

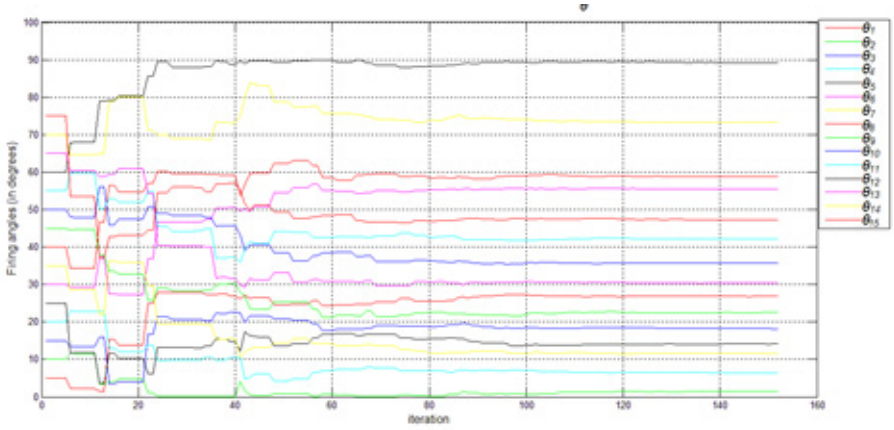

Figure 10. Firing angles evolution vs. Iterations of SAO algorithm.

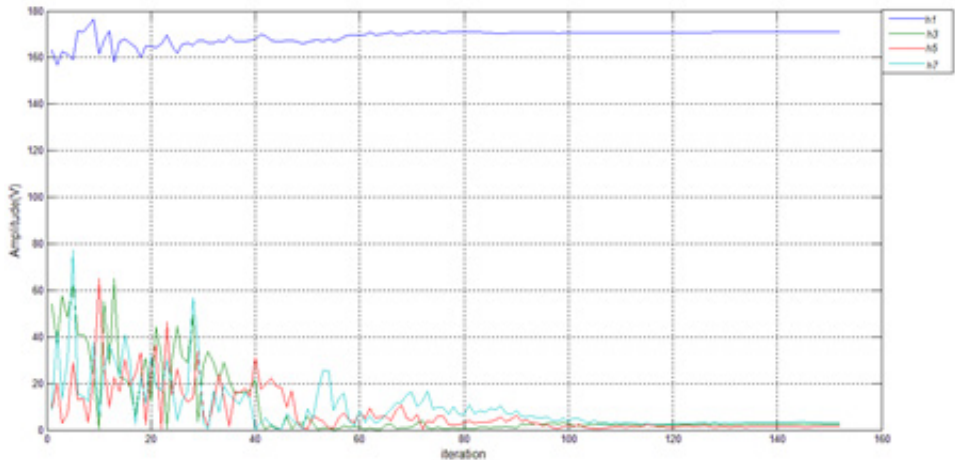

Figure 11. Harmonics evolution vs. Iterations of SAO algorithm.

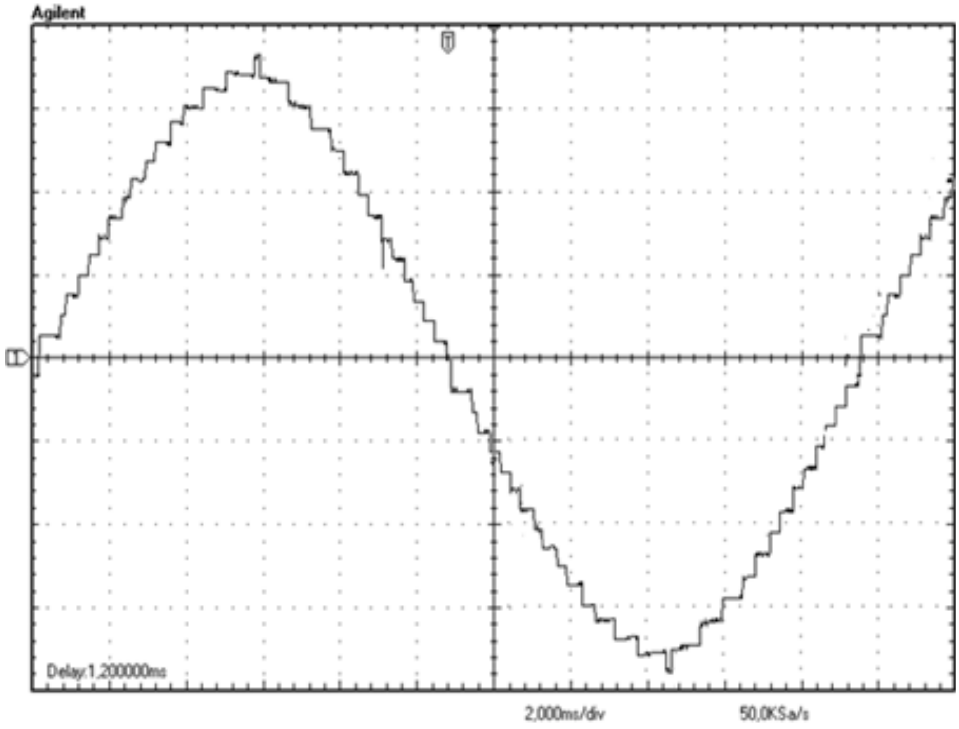

Figure 12. Real output waveform of the 31 level CHB asymmetric multilevel inverter.

Vcc4=96V. Figure 8 makes evident the reduction of harmonic content and, therefore the minimization of THD. Figure 9 shows the evolution of THD throughout iterations of SAO algorithm, achieving a THD=2.1%, whereas Figure 10 shows the evolution of firing angles. Figure 11 shows the evolution of first four harmonics. Figure 12 shows the real waveform obtained in the prototype, whereas Figure 13 presents the harmonic profile. In this case, a THD=2.26% was obtained.

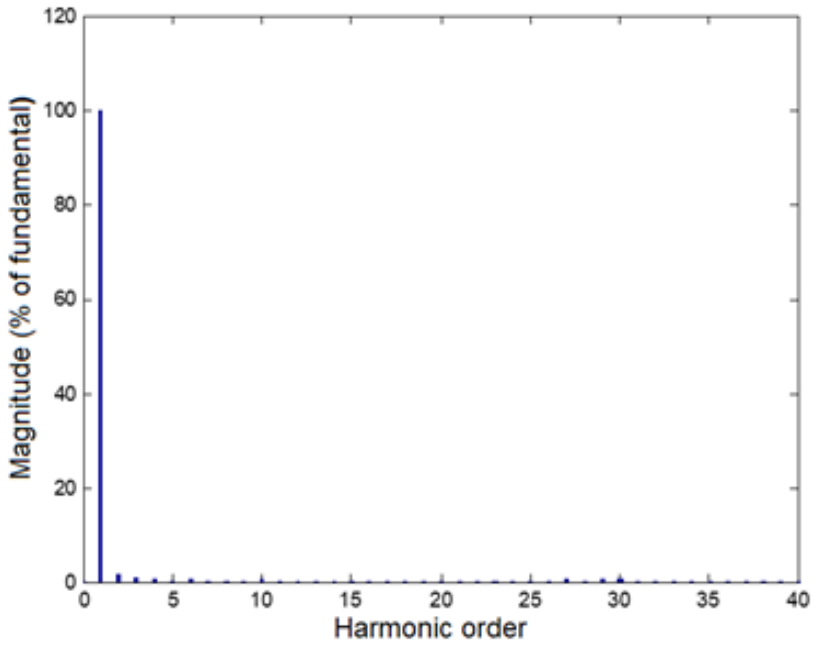

Figure 13. Harmonic profile of the 31 level CHB asymmetric multilevel inverter

Table 3. Firing angles obtained by SAO algorithm (in degrees)

θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}	θ_{13}	θ_{14}	θ_{15}
1.41	6.38	11.53	14.1	18.17	22.51	26.82	30.35	35.7	42.21	47.2	55.17	58.81	73.29	89.23

6. Results and Discussion

As can be seen in Figures 7 and 12, the output waveform obtained by the SAO algorithm is very close to a sine wave and its harmonic content is significantly low, as shown in Figures 8 and 13. The SAO algorithm allowed to obtain a THD of 2.1% in the simulation and a THD of 2.27% in the prototype, satisfying the IEEE 519-1992 normative (THD<5%). In Figure 9 it can see how the THD evolves throughout the algorithm iterations and it achieves a minimum value at the last iterations. The same can be seen in Figures 10 and 11 where the firing angles and the harmonics find the optimal values with each SAO algorithm iteration.

7. Conclusion

In this work, the SAO algorithm was used to find the optimal firing angles in a 31 level multilevel inverter with the aim to minimize the THD, achieving values of 2.1% (simulation) and 2.27% (prototype). The stepped output waveform has a low harmonic content due to the high number of levels and the use of asymmetric topology. Nevertheless, the use of this topology can be difficult in practice due to the value of power supplies necessary for each stage of the inverter. The use of the SAO algorithm allows that it is not necessary to approach the solution of the transcendental equations formally since this algo-

rithm explores the search space from several points of the solution and does not focus on finding an exact solution but the optimal solution to the problem. Finally, it is important to remark that the SAO algorithm is a heuristic based method. This implies that it can give slightly different solutions in each execution but always it satisfies the optimization problem.

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