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Optimization of THD in a Cascaded Multilevel Inverter based on Multiple-Carrier Pulse Width Modulation and Simulated Annealing

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Abstract

Objectives: This paper deals with the reduction of THD (Total Harmonic Distortion) in the voltage output waveform of a four-stage monophasic cascaded multilevel inverter with Multiple-Carrier Sine Pulse Width Modulation (MCSPWM) using the Simulated Annealing Optimization (SAO) technique. **Method**: The SAO algorithm was employed to calculate the appropriate firing angles for the switching devices of the inverter by mean of finding the best symmetry of the triangular wave, its frequency and the amplitude of the sine wave used in the modulation through of MATLAB. The monophasic multilevel inverter was simulated and evaluated using de SAO algorithm, then, a prototype was implemented for validating the results. **Findings**: The output waveform of the converter for multiple scenarios, the graphic of the harmonic content and the optimized modulation parameters were obtained in both the simulation and the prototype. The Simulated Annealing algorithm allowed to find the appropriate firing angles for the four-stage multilevel inverter, adjusting the optimal parameters of triangular and sine signals used in MCSPWM modulation, leading to obtaining a low harmonic content in the output waveform (THD less than 5%), using a low number of switching devices. **Novelty/Improvement:** The proposed technique (Simulated Annealing) permits to find the optimal parameters of modulation waveforms through a heuristic approach avoids the possible issues with local minima. Also, the method applied optimizes the number of necessary switching devices.

Keywords: Multilevel Inverter, Multiple Carrier SPWM, Simulated Annealing, THD

1. Introduction

Currently, the conversion of DC power supplies as batteries, photovoltaic cells, wind turbines, among others, in an AC source is a necessary process that requires the use of DC/AC converter circuits with high efficiency. The conventional AC/DC converters have important disadvantages such as high THD, high voltage change rates, high switching voltages, and electromagnetic interferences.

In the last years, multilevel inverters have emerged as an alternative to traditional H-bridge inverters, principally in low and mid power applications because of the capability of working at high power using commutation devices with small operation voltages. The general idea of multilevel inverters consists in a large number of switching devices based on power semiconductors such as MOSFET transistors, which convert the electrical energy provided by DC voltage sources into small steps, achieving an AC output waveform with a low THD[1,2].

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The three main topologies of multilevel inverters are: The Neutral Point Clamped, Flying Capacitor multilevel inverter, and cascaded multilevel inverter or Cascaded "H" Bridge (CHB). Nowadays, the cascaded multilevel inverter is the most used due to its low number of semiconductors employed; besides, this inverter presents a "modular" topology and is more expandable than others[1]. One of the major difficulties of multilevel inverters is the need to find the firing angles of the power semiconductors, due to the complexity of its commutation patterns and its high number of switching devices. There are various methods such as the selective harmonic elimination that requires the solution of a transcendental equation system[3], for example, using iterative methods as Resultant Theory and Newton Raphson[4–7]. Another commutation scheme that has been widely employed is called multiple carriers SPWM that consists in the comparison between a reference sine wave and various triangular waves (one for each level of the inverter). The parameters of these waveforms and its variation determine the quality of the output. There are diverse methods reported in the literature[8–13] which search to calculate the commutation patterns for the inverter, but one of the possible issues with these methods is that they need a good initial guess and might not converge at some points. By another side, some heuristic based methods (Genetic Algorithms, Particle Swarm Optimization, Simulated Annealing among others) offer an interesting alternative to find the most appropriate parameters of the sine wave carrier and reference triangular waves because allow to see it as an optimization problem. Various of these methods have been used successfully for conventional H-bridge inverter and multilevel inverter[14–18], however, we found a lack of interest in the application of Simulated Annealing optimization for multiple-carrier SPWM.

In this work, we use the Simulated Annealing Optimization method to find the optimal parameters of the modulation scheme (MCSPWM) that allows obtaining the switching angles for power semiconductors in a four-stage multilevel inverter, reducing the THD to less than 5% (IEEE 519-1992 normative). This paper is organized as follows: Section 2 describes the cascaded multilevel inverter and the modulation strategy employed. Section 3 discusses the simulated annealing algorithm. Section 4 deals with optimization problem statement. Section 5 gives the simulation results and prototype followed by the conclusion.

2. Four-Stage Multilevel Inverter

Figure 1 shows the general sketch of the monophasic CHB multilevel inverter. Each stage (also called cell) of the inverter is made of four semiconductor-based switching devices, like MOSFET or IGBT, in a configuration called H-bridge. These stages are connected in series, so the output voltage of each one adds up, achieving an output waveform that depends on the individual signal of each stage. Each stage in the inverter has an independent DC power supply. In this case, all of the power supplies have the same voltage. This configuration is called "symmetric converter", and the number of output levels can be found by:

$$N = 2s + 1 \tag{1}$$

Where N is the number of output levels and s is the number of stages in the inverter. In Figure 1, the DC power supplies have the same value for each stage (i.e. Vcc1 = Vcc2 = Vcc3 = Vcc4 = Vcc), so, according to Equation (1), if s = 4, then the inverter has N = 9 output levels. Figure 2 shows the typical output waveform (in black) and the fundamental harmonic (in red) for stepped modulation, whereas in Figure 3 we can see the typical output waveform for MCSPWM modulation (in black) and the fundamental harmonic (in red).

2.1 MCSPWM Modulation

Multiple-Carrier Sinusoidal Pulse-Width Modulation (MCSPWM) is a technique that consists of comparing a sinusoidal reference signal at the fundamental frequency and a series of triangular-shape waves (one for each cell on the converter). The modulation index, m, the frequency and the shape of the triangular signals can determinate

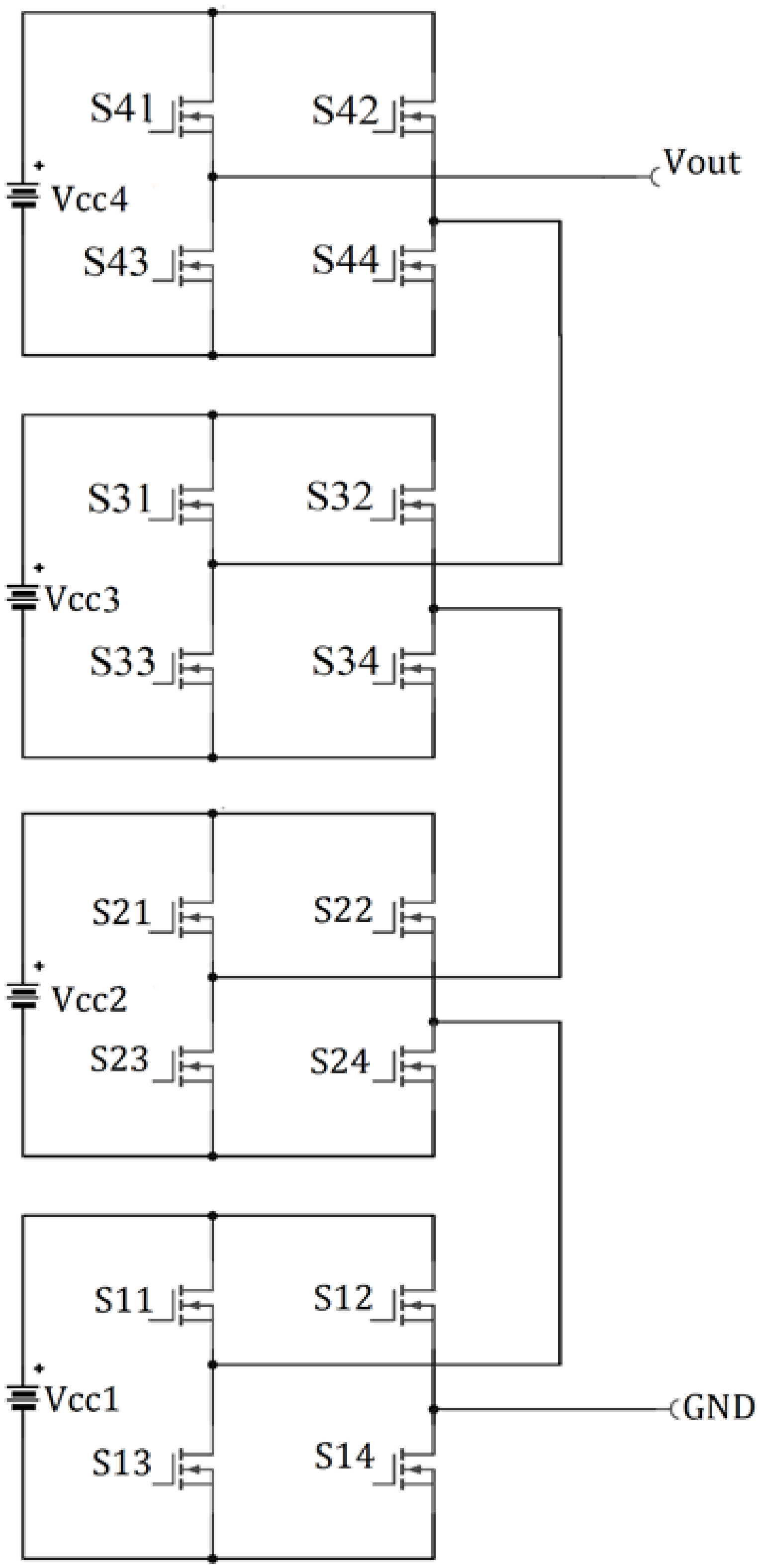

Figure 1. Four stage monophasic CHB multilevel inverter.

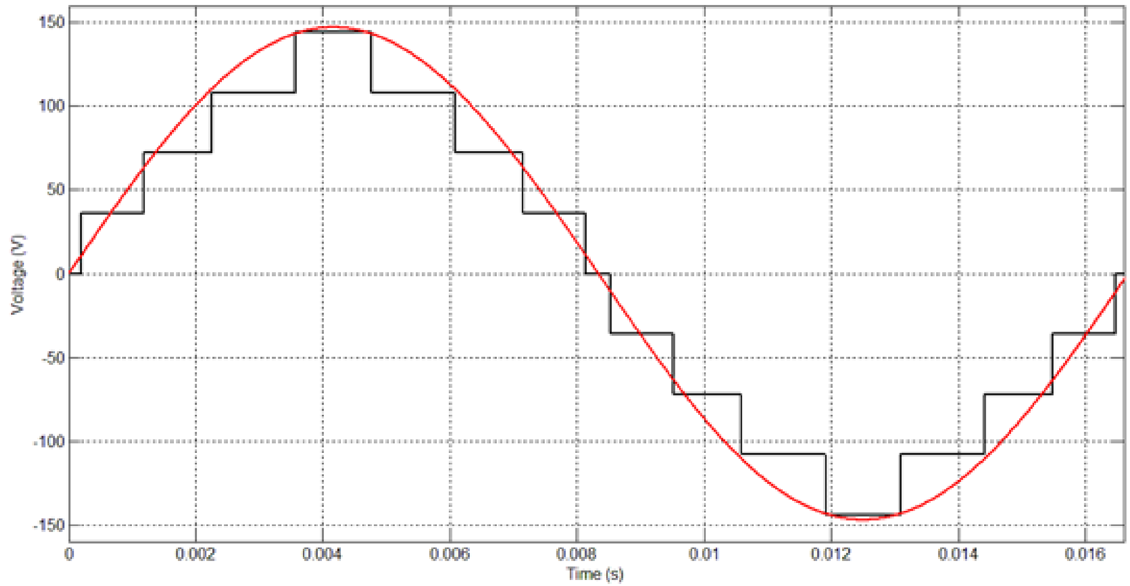

Figure 2. Typical output for the four-stage CHB symmetric multi-level inverter.

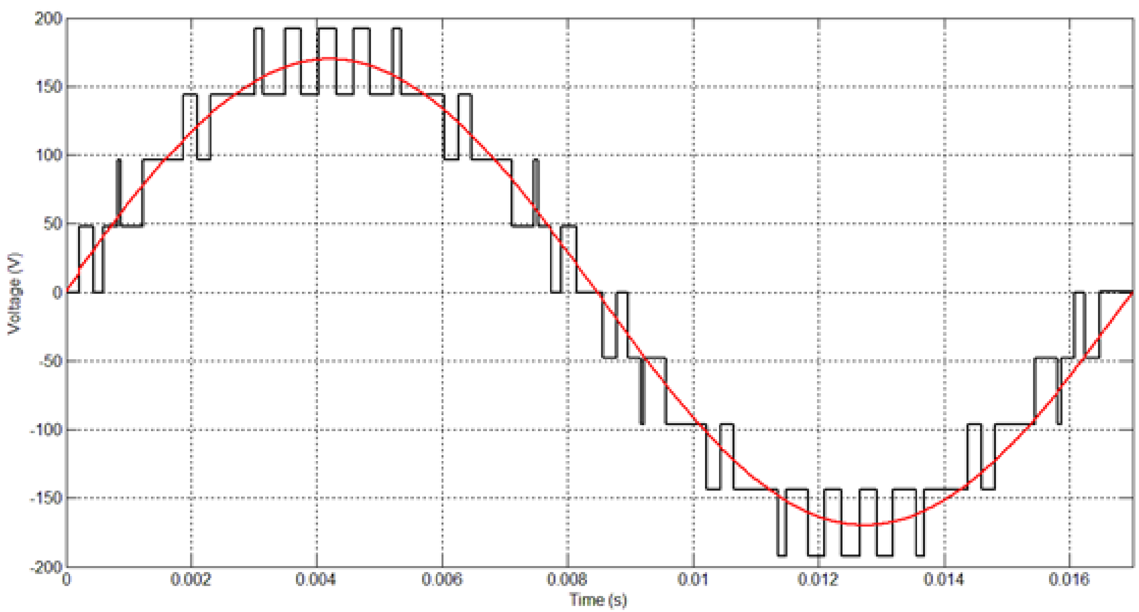

Figure 3. Typical output for the four-stage CHB with MCSPWM modulation.

the quality of the output waveform. Figure 4 shows the MCSPWM modulation for a half cycle, Figure 5 depicts the output of each stage in the converter and in Figure 6 we can appreciate the output waveform as result of adding each output of the stages.

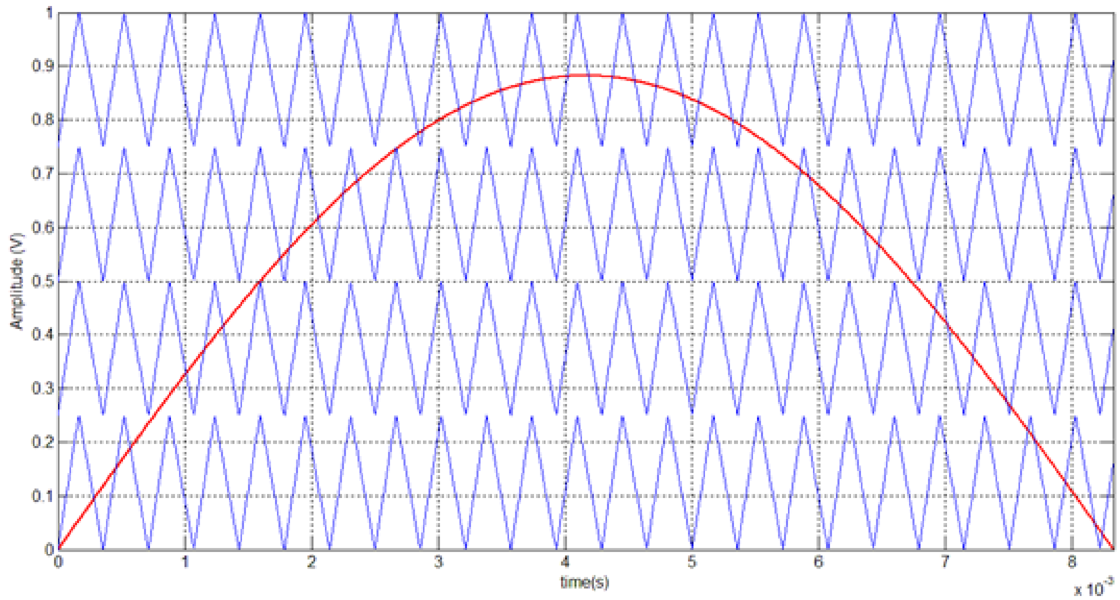

Figure 4. Reference signal (red) and triangular carriers (blue) in the MCSPWM modulation.

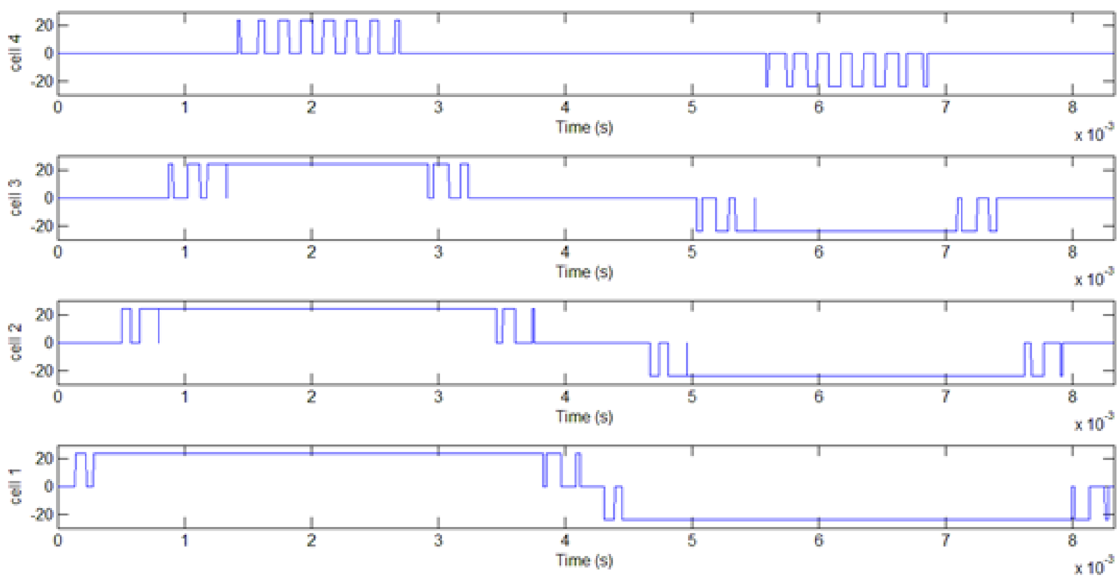

Figure 5. Individual outputs for each cell on the inverter.

3. Simulated Annealing Optimization

Simulated Annealing Optimization (SAO) is a probabilistic method that was proposed by[19]. The aim of the SAO algorithm is to find the global minima of a cost function which can have many local minima. SAO algorithm works through the imitation of a thermodynamic physical phe-

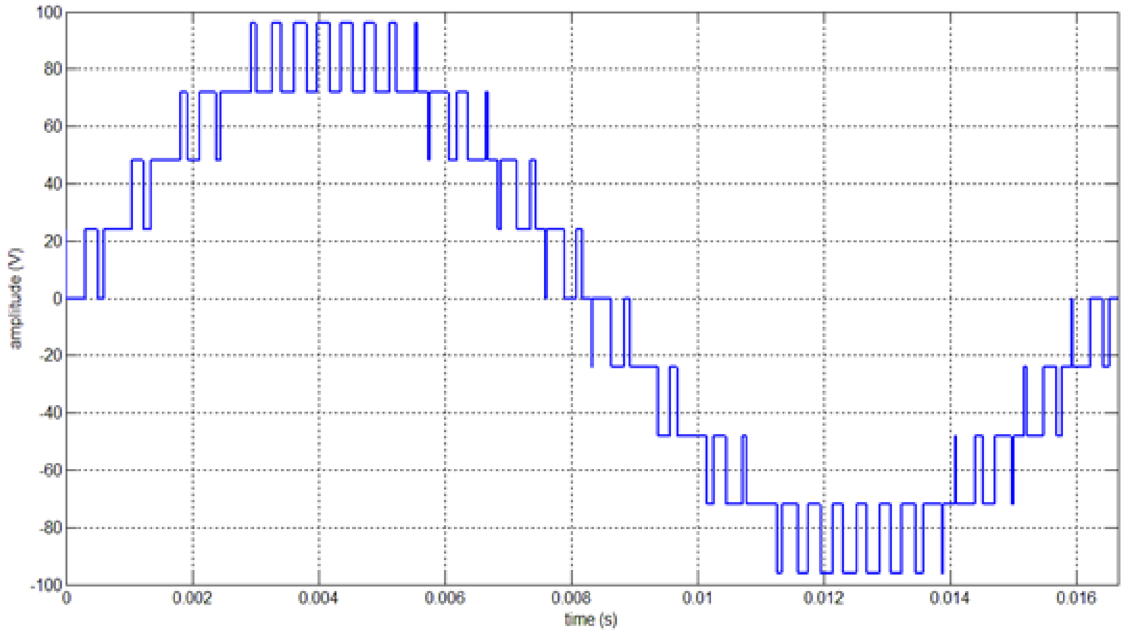

Figure 6. MCSPWM output waveform.

nomenon by which a solid material is cooled slowly until eventually its molecular structure is frozen and achieves the minimal energy configuration.

The SAO algorithm works as follows: It starts with a random approximation of the values of the cost function variables. The process of heating permits changes randomly the value of the variables. A higher heat involves best random variations. The cost function returns the output f, associated with a variable set. If the output decreases, then the new variable set replaces the old one. If the output increases, then the output is accepted, while the following relationship is fulfilled[20]:

$$r \leq e^{[f(P_{old})-f(P_{new})]/T} \tag{2}$$

Here, r is a random number and T is the temperature. If the Equation (2) is not satisfied, then the algorithm rejects the new set of variables. Thus, even if the new set of variables means a worse cost, it can be accepted with a certain probability. The new set of variables is calculated taken a random step from the last set of variables:

$$P_{new} = d \cdot P_{old} \tag{3}$$

Where d is uniformly distributed around of P_{old}. This control variable sets the step size so that the beginning the algorithm is obliged to do big changes in the value of the variables. Sporadically, the changes move the algorithm away for the optimal, which leads to the algorithm to explore new regions of the search space. After a certain time, it is impossible to obtain more low costs. At this moment, the values of T and d are decreased and the algorithm is running again, until T = 0. The drop in temperature is known as the "cooling schedule". The temperature in the n step can be calculated like this:

$$T_n = f(T_0, T_N, N, n) \tag{4}$$

Where T_0 is the initial temperature and Tf is the final temperature and f is decremented with the time. Some of the most used cooling schedules are:

Linearly decrescent:

$$T_n = T_0 - n(T_0 - T_N)/N. \tag{5}$$

Geometrically decrescent:

$$T_n = 0.99T_{n-1} \tag{6}$$

Hayjek optimal:

$$T_n = c/\log(1+\mathrm{n}) \tag{7}$$

Where c is the smallest variation required to exit from a local minimum.

4. Optimization Problem Statement

As described in Section 2, in the MCSPWM it is necessary to find the appropriate shape and frequency of the triangular signals and the amplitude of the sine reference signal with the aim to obtain an output waveform with low harmonic content and a correct fundamental voltage. The THD and fundamental voltage of the output, in this case, depends on the modulation index m, the number of pulses and its position. These variables will be the variable set of the cost function.

The modulation index, *m*, is the rate between the amplitude of the sine reference and the triangular carriers. The number of pulses depends on the frequency of triangular signals, and the pulse position is determined by the symmetry of the triangular signals, i.e. the relationship between the rising time (tr) and the falling time (tf) of the triangular waveform, as can be seen in Figure 7, where three examples are presented for different symmetry parameters. Here, the triangular signals are drawn in blue, whereas a portion of the sine signal is drawn in red. The pulse that results of the comparison is drawn in black.

In MATLAB exists a function that allows generating a triangular signal with the possibility of varying its symmetry, the function is called "sawtooth" and its syntax is as follows:

Sawtooth (T, width)

The function above generates a sawtooth signal with period 2π for the elements of time vector T. The parameter "width" is a scalar parameter between 0 and 1 that determines the fraction between 0 and 2π at which the maximum of the signal occurs. The function increases from -1 to 1 on the interval 0 to width × 2π, then decreases linearly from 1 back to -1 on the interval width × 2π to 2π. If width = 0,5 the triangular waveform is symmetric, i.e. *tr = tf*.

The optimization problem can be considered as follows:

To minimize:

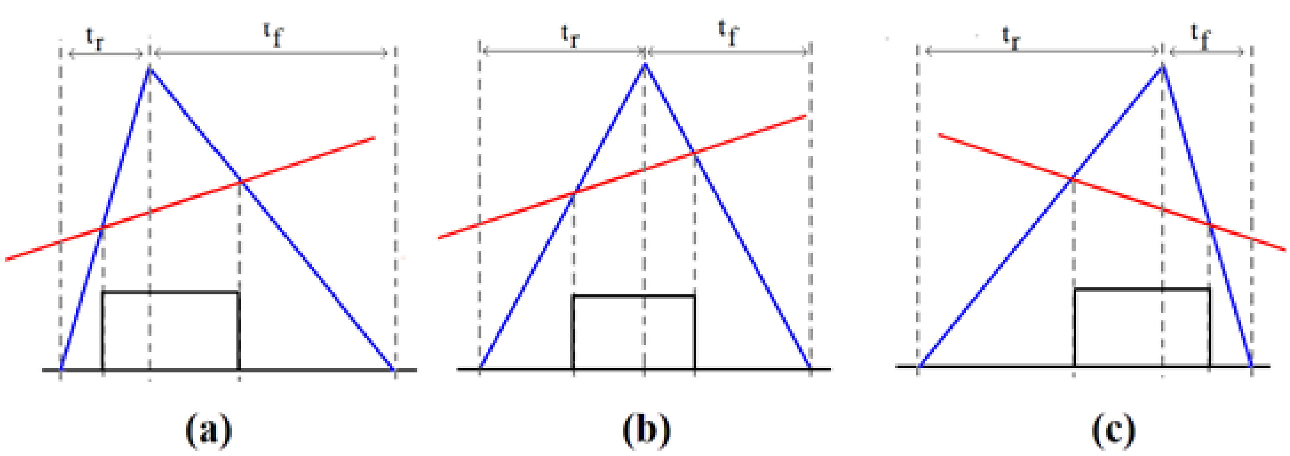

Figure 7. Variation in the pulse position for different symmetry parameter of the triangular signal: a) tr<tf, b) tr = tf, c) tr>tf.

$$THD\% = \sqrt{\left(\frac{1}{h_1^2}\right)\sum_{n=3}^{\infty}(h_n^2) \cdot 100} \qquad (8)$$

Where:

h_1 is the fundamental harmonic amplitude.

h_n is the *nth* harmonic amplitude, for *n* odd.

Satisfying the following constraints:

h_1 =169.7 Vp.

Fc = 3 KHz.

M =1.

Width = 1.

5. Simulation and Prototype

The Simulated Annealing Optimization algorithm (SAO) was developed in MATLAB and a model of the multilevel inverter was implemented on Simulink, as can be seen in Figure 8. For implementing the optimization problem proposed previously, the simulannealbnd tool of MATLAB was used. The general syntax is as follows:

X = simulannealbnd (PROBLEM). This function finds the minimum for PROBLEM, which is a structure that has the following structure:

Objective: It is the objective function. In this case, it corresponds to the THD shown in equation 13.

x0: Starting point of the set of variables.

lb: Lower bound on *X*.

ub: Upper bound on *X*.

Options: Options structure created with saoptimset function.

rngstate: It is the state of the random number generator

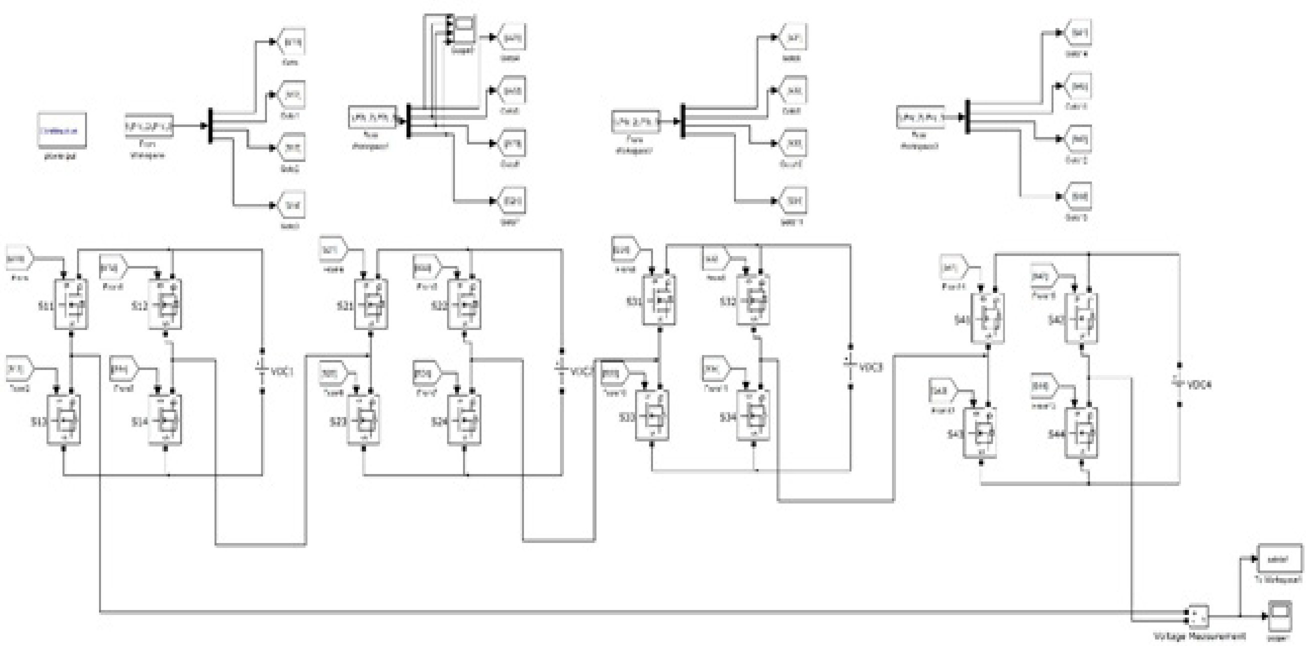

Figure 8. Simulink model of CHB multi-level inverter.

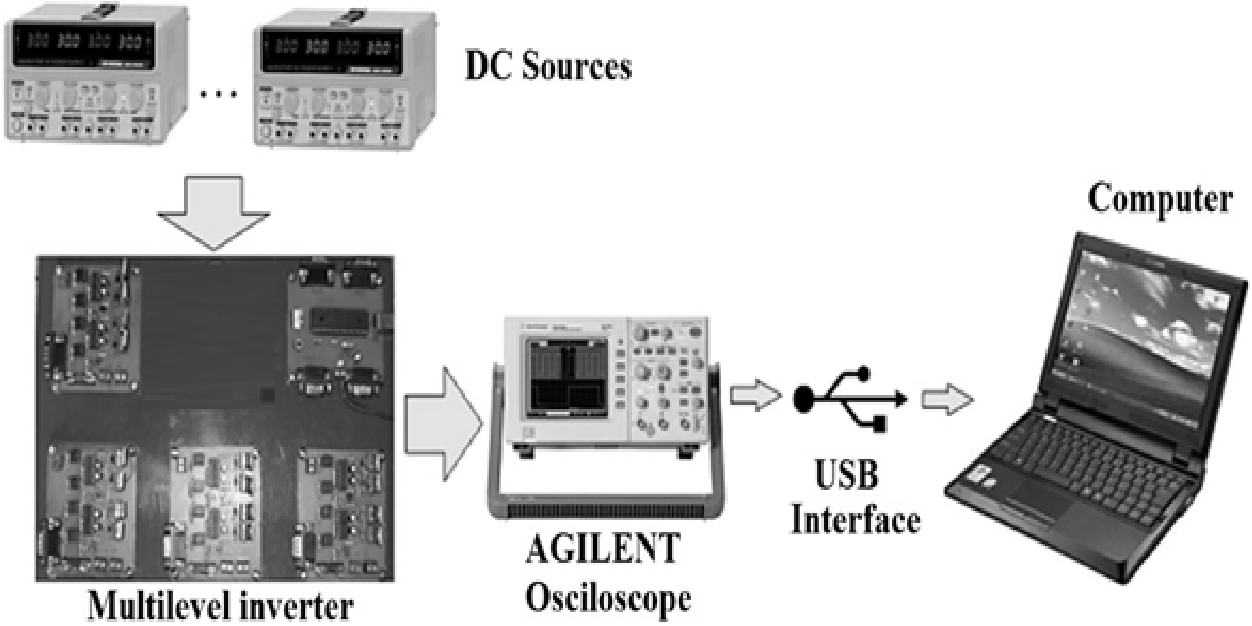

Figure 9. Block diagram of the prototype.

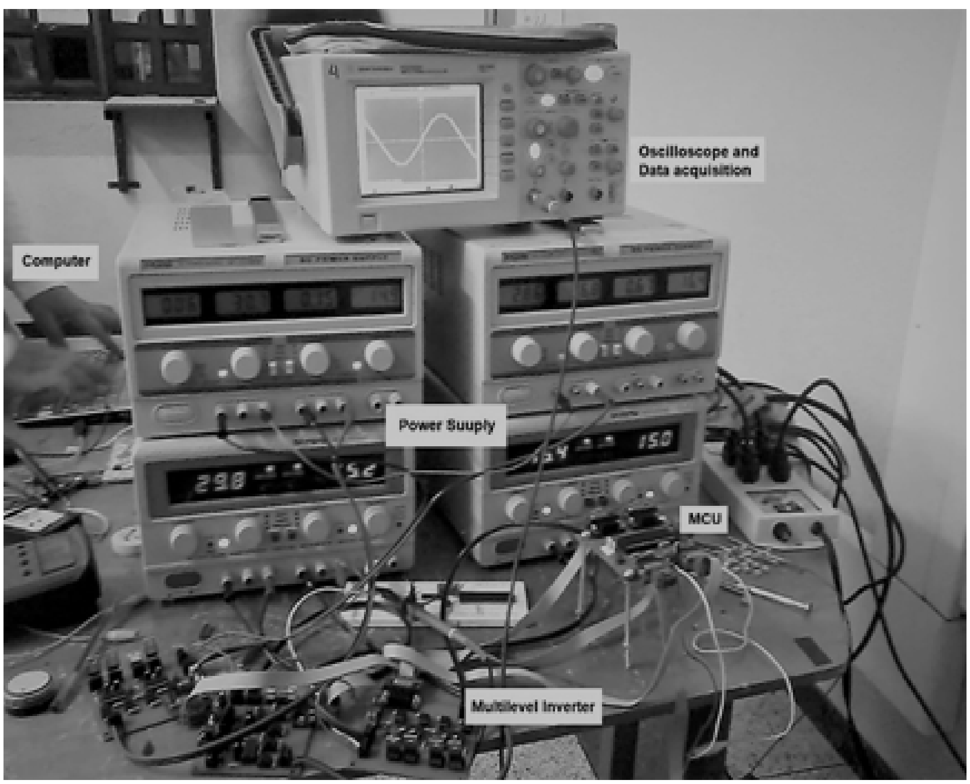

Figure 10. Experimental setup for 31 level CHB multi-level inverter.

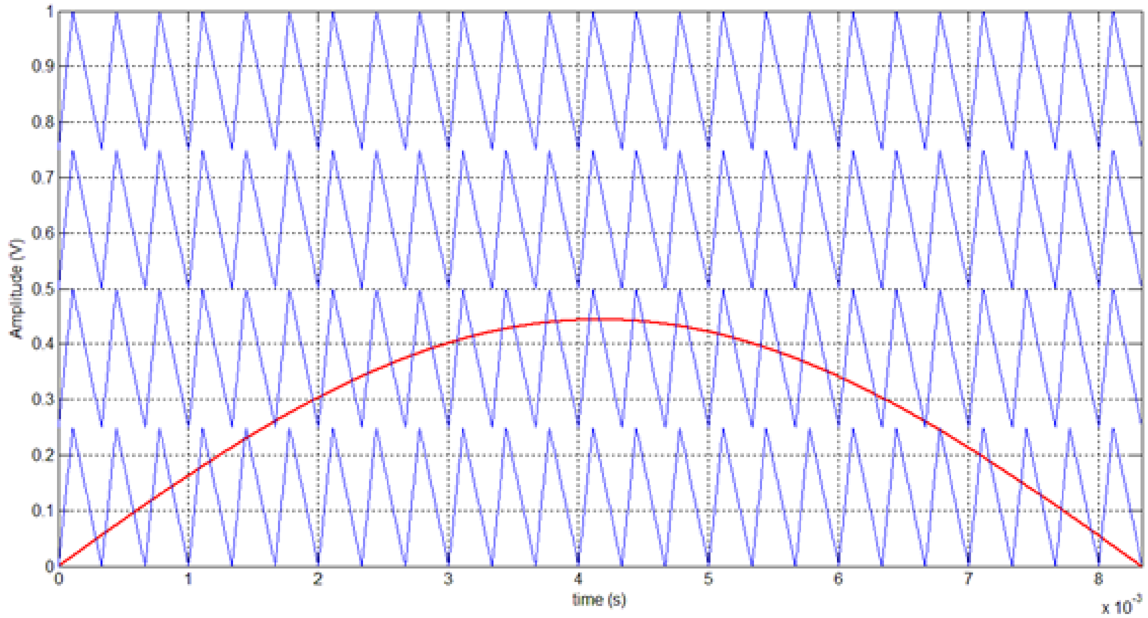

Figure 11. Optimized modulation signals for 2 stage inverter (sine reference in red, triangular carriers in blue).

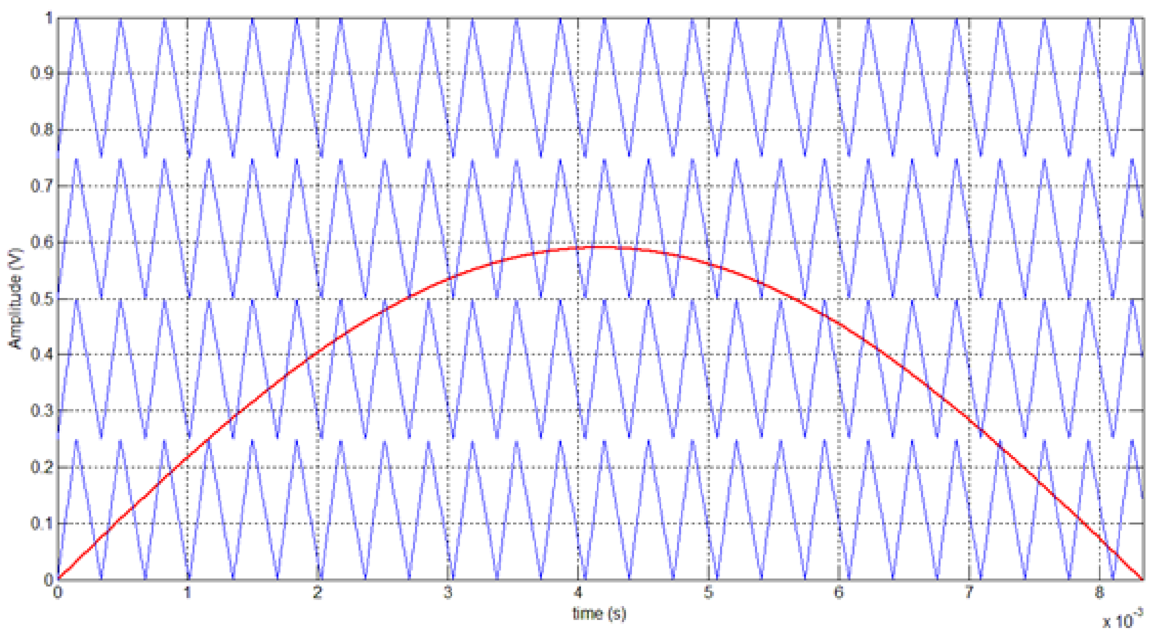

Figure 12. Optimized modulation signals for 3 stage inverter (sine reference in red, triangular carriers in blue).

The set of variables X for the SAO algorithm consists of three parameters: The sine reference amplitude, the triangular carriers and its frequency. All of these parameters were normalized in a range of 0 to 1.0.

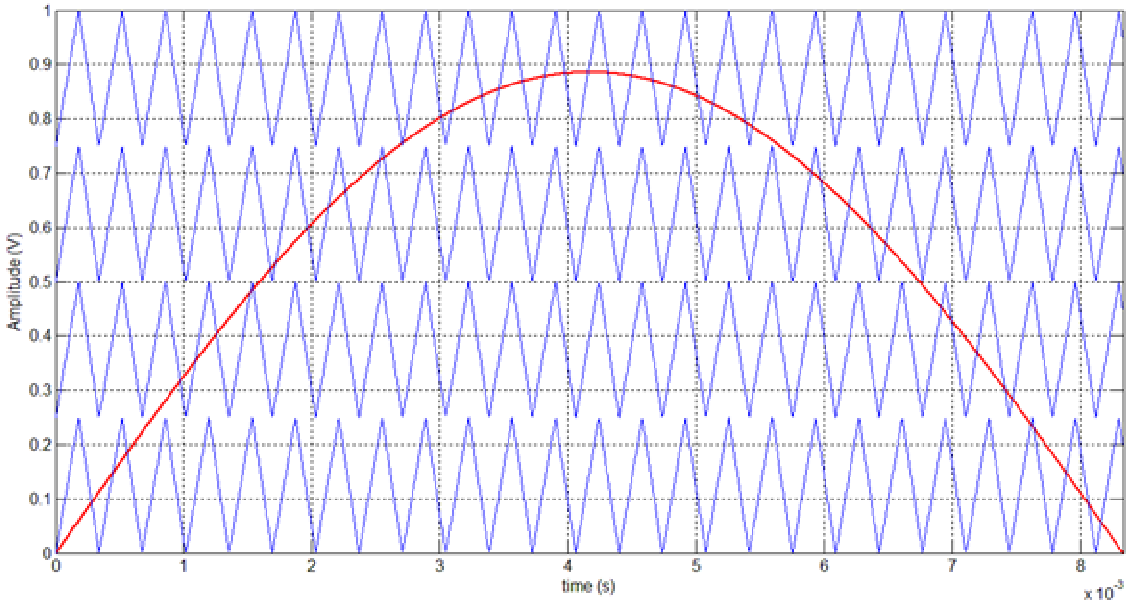

Figure 13. Optimized modulation signals for 4 stage inverter (sine reference in red, triangular carriers in blue).

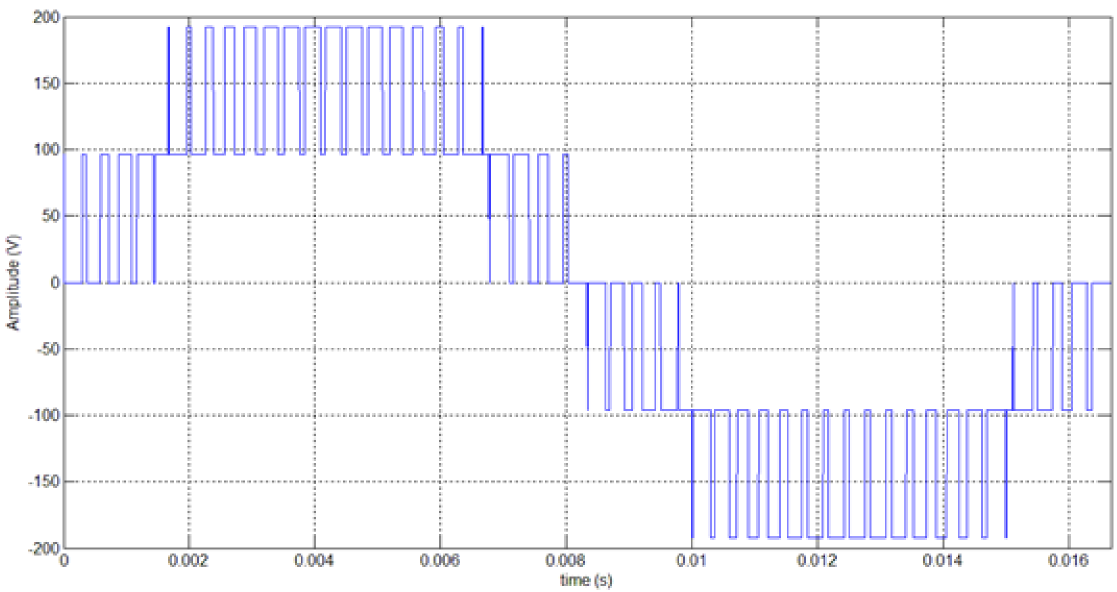

Figure 14. Optimized output waveform of 2-stage inverter.

The simulations were made to find the optimized parameters. To validate the simulation results, a prototype of the multilevel converter was implemented and the firing angles calculated by the SAO algorithm were loaded on a PIC18F4550 device. In Figure 9 we can see the block diagram of the system, whereas Figure 10 shows

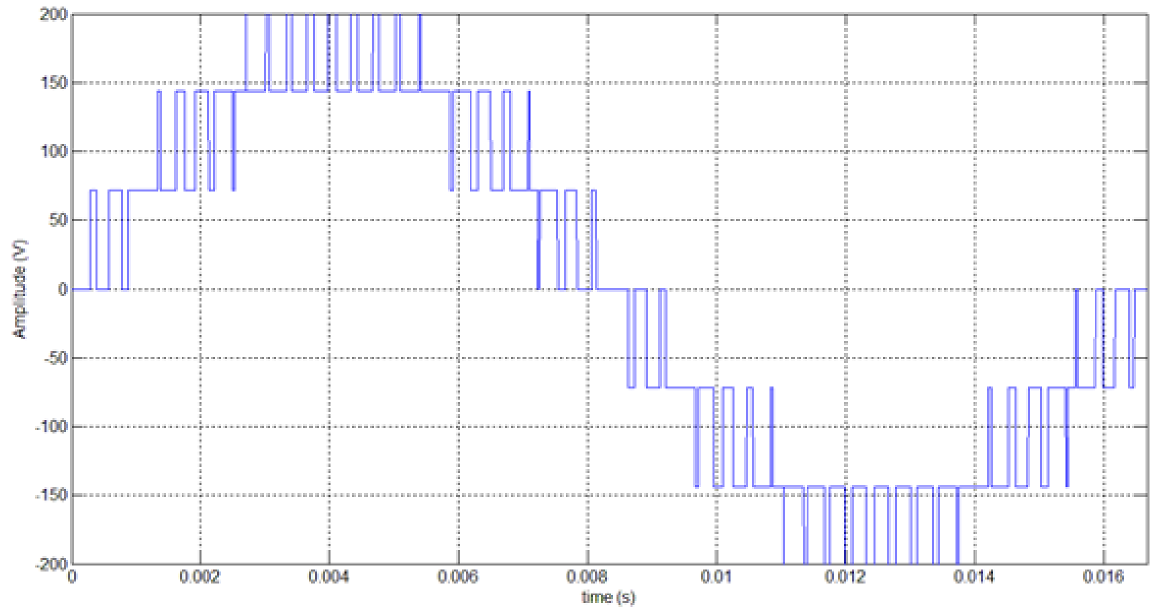

Figure 15. Optimized output waveform of 3-stage inverter.

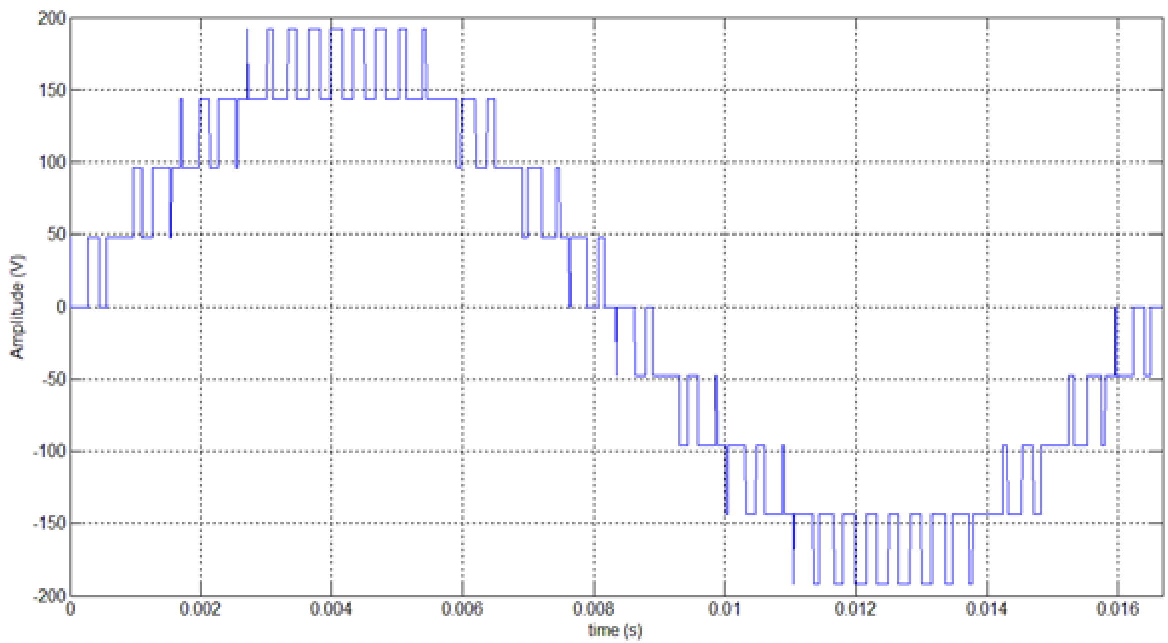

Figure 16. Optimized output waveform of 4-stage inverter.

the setting of the prototype. The Agilent DSO3202-A digital oscilloscope was used for data acquisition, analysis, and output waveform visualization.

With the aim to reduce the number of stages in the converter, and therefore, the number of switching devices, the amplitude of the DC supplies can be selected in the

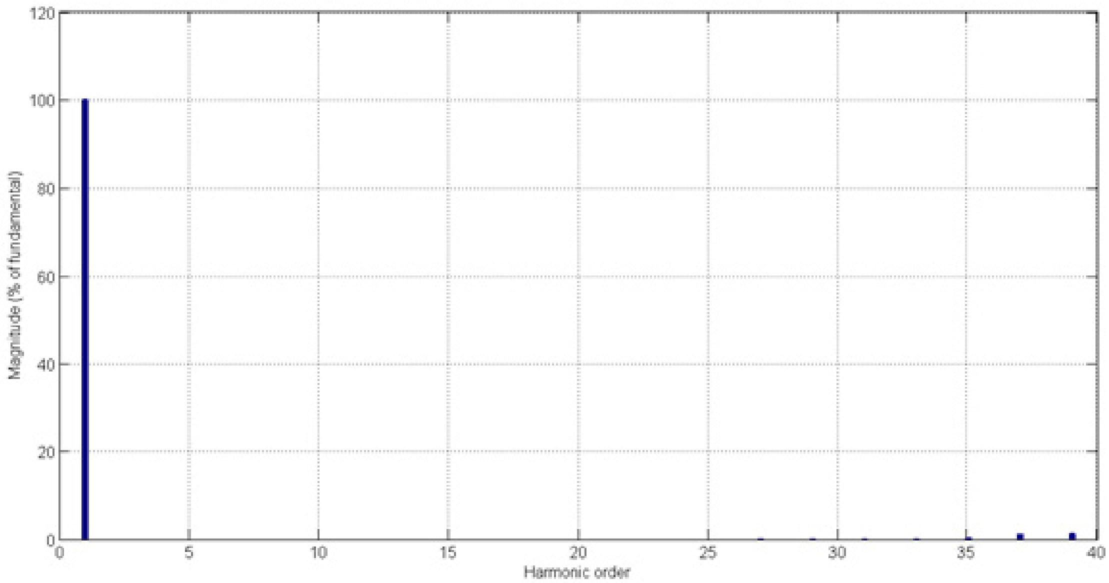

Figure 17. Harmonic profile for 2 stage inverter.

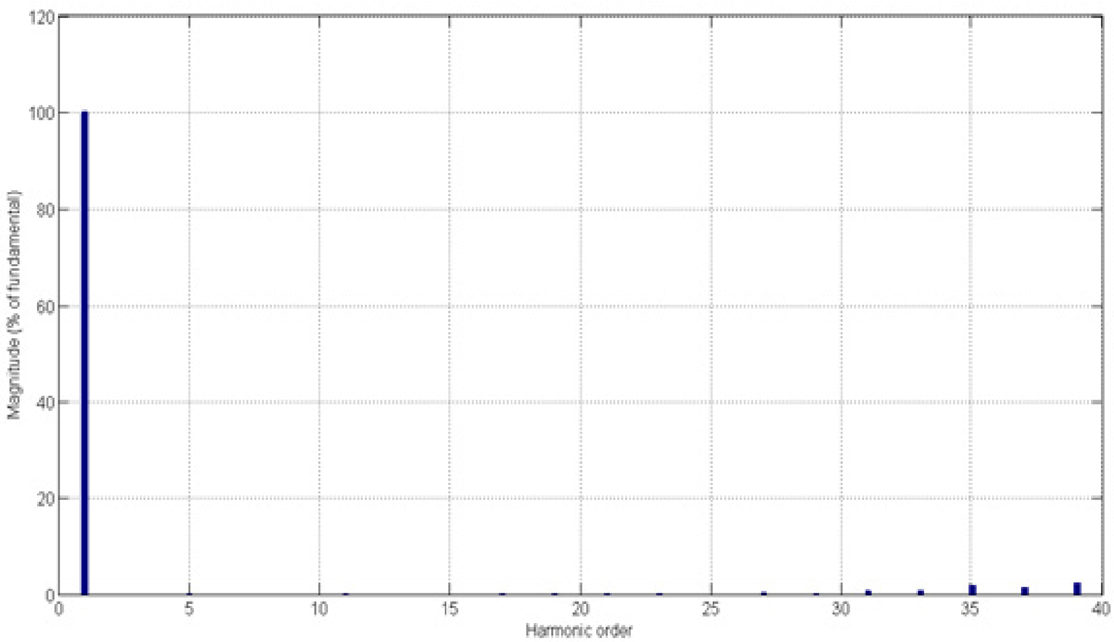

Figure 18. Harmonic profile for 3 stage inverter.

manner that the SAO algorithm can optimize the modulation index for a particular value of the DC sources.

Figures 11-13 show the optimized signals (sine reference and triangular carriers) for the 2, 3 and 4 stage converters, with 96V, 72V and 48V DC power supplies respectively. Figures 14-16 show the optimized output waveforms for the 2, 3 and 4 stage converters, and Figures 17-19 display the harmonic profile for each one of the

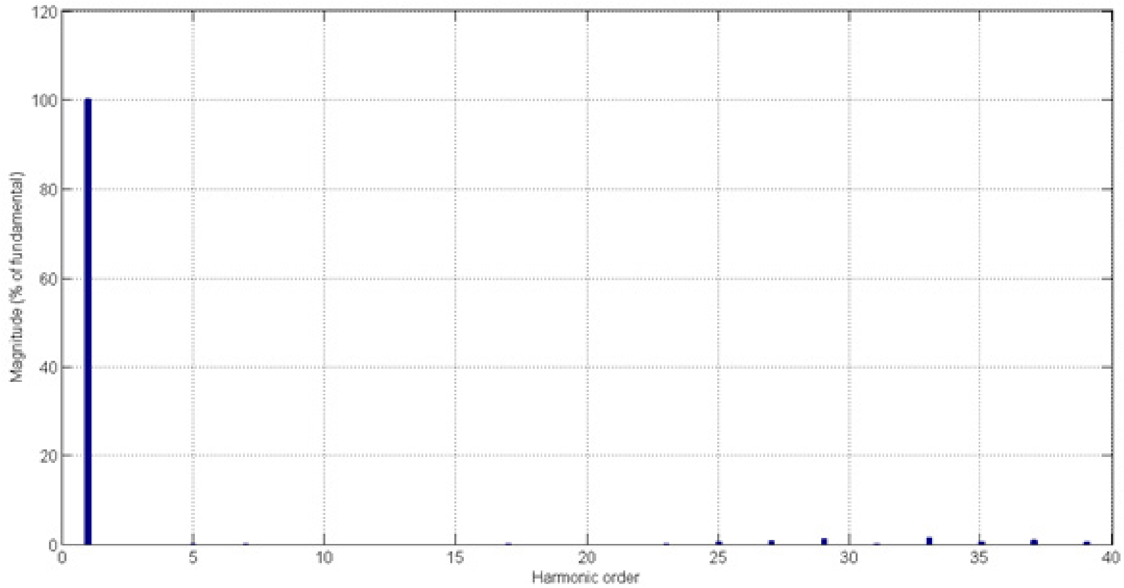

Figure 19. Harmonic profile for 4 stage inverter.

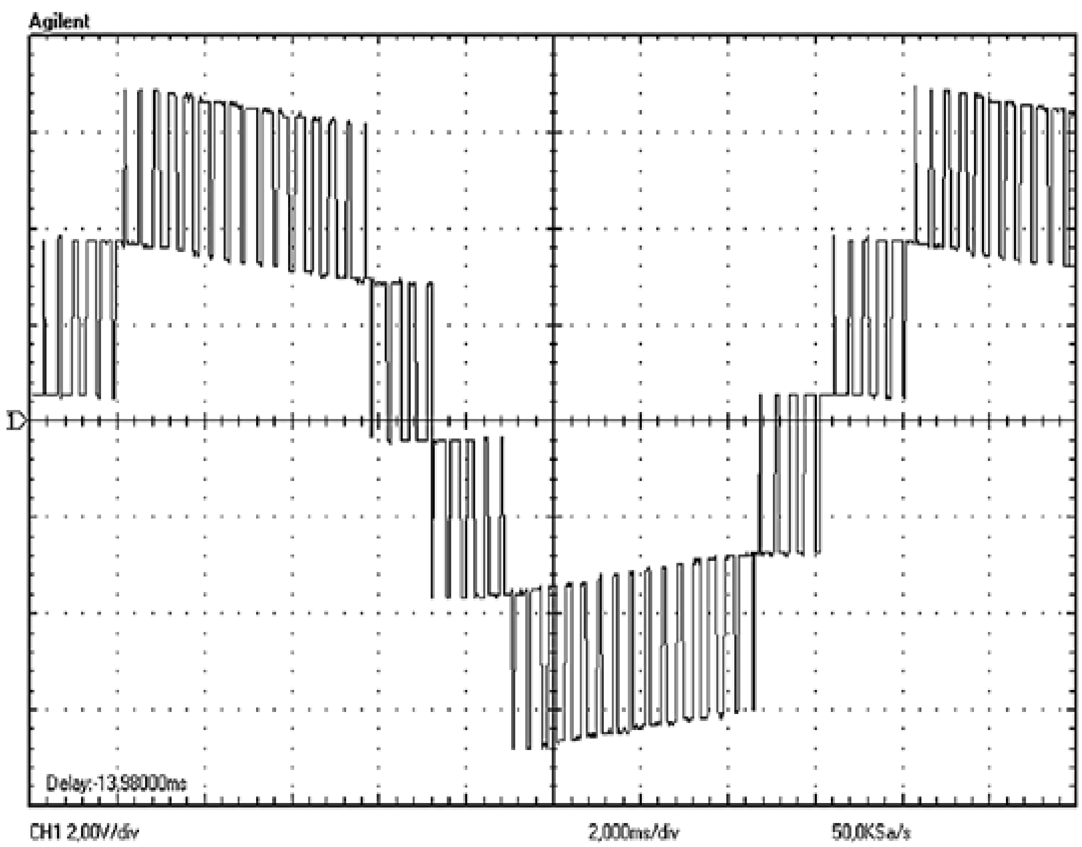

Figure 20. Practical optimized output waveform for 2 stage inverter.

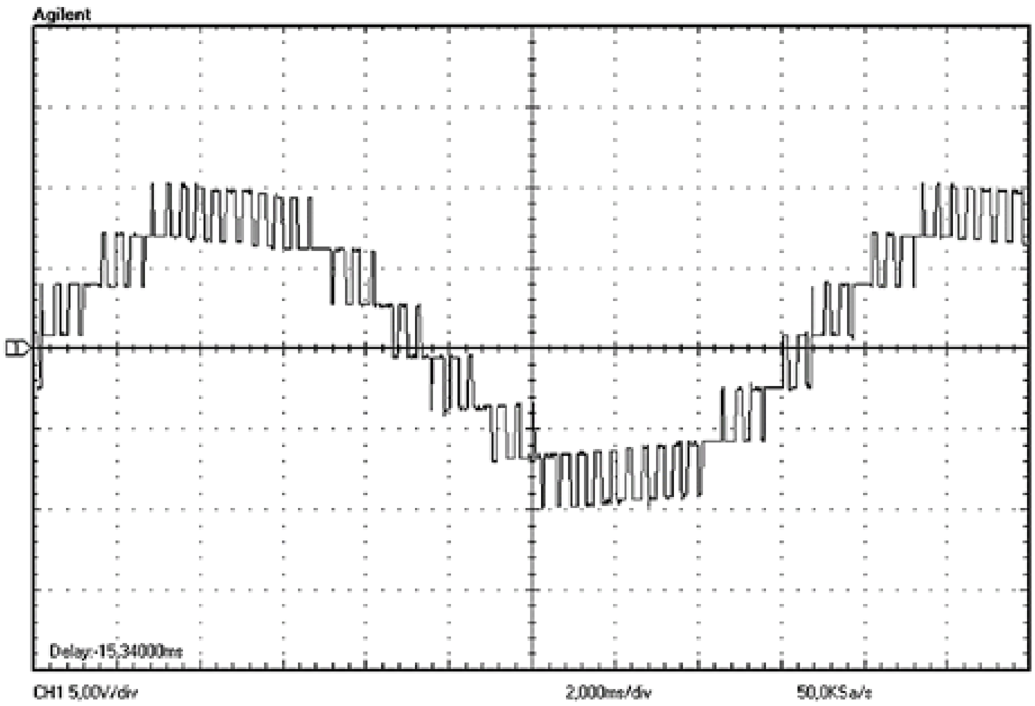

Figure 21. Practical optimized output waveform for 3 stage inverter.

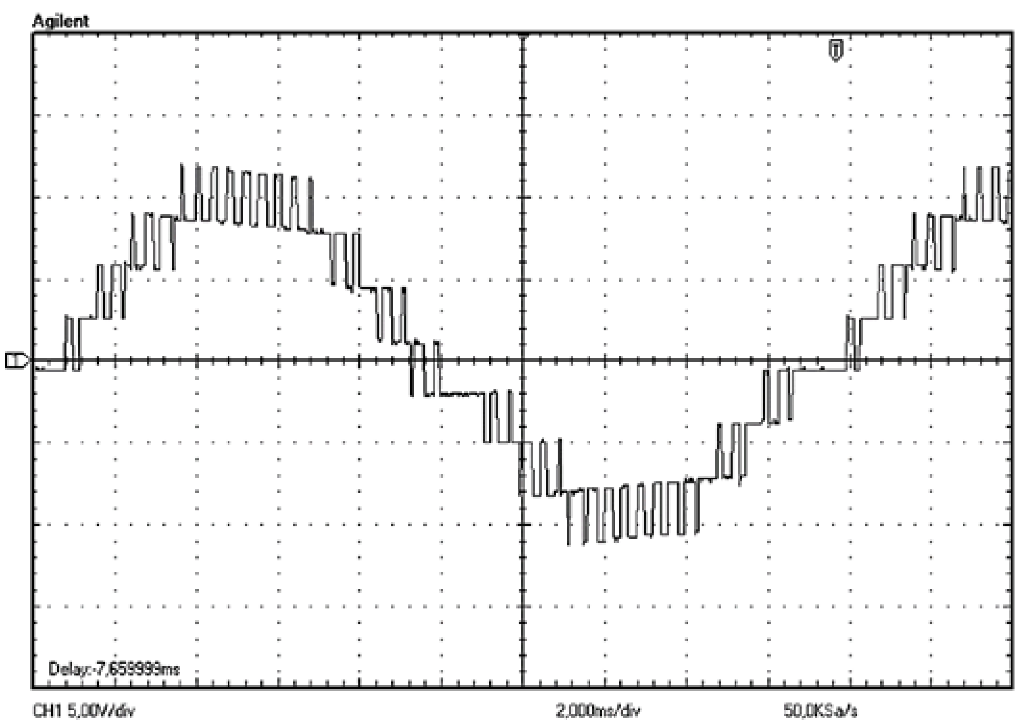

Figure 22. Practical optimized output waveform for 4 stage inverter.

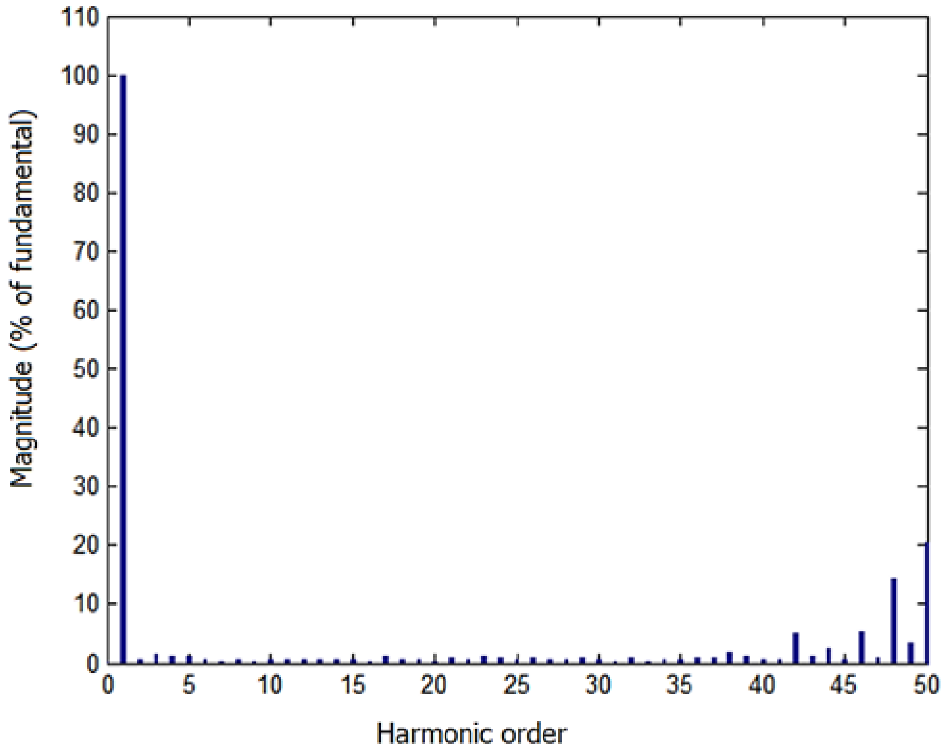

Figure 23. Optimized harmonic profile for 2 stage inverter.

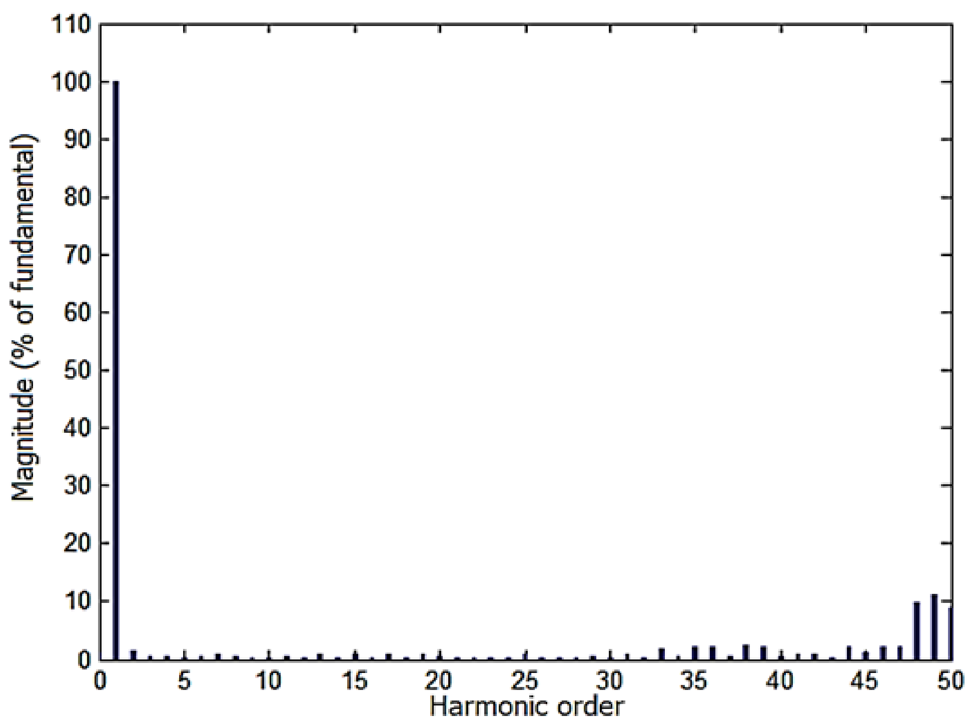

Figure 24. Optimized harmonic profile for 3 stage inverter.

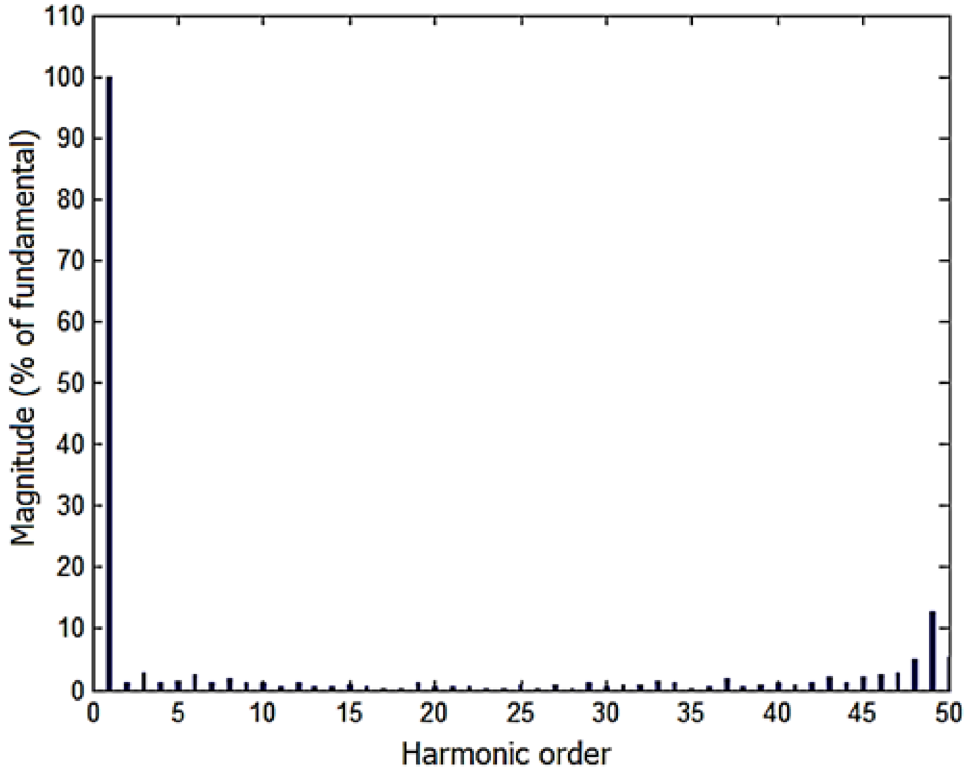

Figure 25. Optimized harmonic profile for 4-stage inverter.

Table 1. Summary of results for both simulation and prototype

Number of stages	% THD (Simulation)	% THD (Prototype)	Amplitude of fundamental (Vp) (Simulation)	Amplitude of fundamental (Vp) (Prototype)
2	2,36	3,9	170,19	164
3	4,14	5,39	169,87	169,7
4	3,13	4,6	170	168,29

converters. The practical output waveforms obtained with the prototype in each case is presented in Figures 20-22 whereas Figures 23-25 shows the real harmonic profile for the 2, 3 and 4 stage converters. Finally, Table 1 summarizes the results obtained with SAO algorithm, both the simulation and the prototype.

6. Results and Discussion

As seen in Figures 11-13, the SAO algorithm was able to find the optimal parameters for the sine reference signal and triangular carrier signals. The output waveforms obtained for the 2, 3 and 4 stages converter displayed in

Figures 14-16 which show how the output signal is close to a sine wave. Comparing the output waveforms of the prototype in Figures 20-22 with the simulation results it is evident that they are consistent and very close to the simulation model. Respect to the harmonic profiles that can be seen in Figures 17-19 for the simulation and Figures 23-25, for the prototype and the data summarized in Table 1, we can see that the 2-stage converter reached the lowest THD (2, 36% in simulation, 3,9% in the prototype). It's a very interesting result because of that in this case; the converter has the lowest number of semiconductor devices. Nevertheless, all the three cases reached a THD<5% in the simulation.

7. Conclusion

In this work, the Simulated Annealing algorithm was used to find the optimal parameters of SPWM modulation scheme, in particular, the modulation index through the optimal amplitude of the sine reference signal, and the symmetry and frequency of the triangular carrier signals, achieving values of 2,36% (simulation) and 3,9% (prototype). The MCSPWM modulation allows obtaining output waveforms with a low harmonic content and a precise fundamental voltage. Nevertheless, the use of this modulation scheme can be difficult in practice due to the value of DC power supplies required for each cell of the inverter and the high commutation frequency necessary for the power switching devices. On the other hand, the little differences between the simulation and prototype results can be explained because of that the simulation models do not consider the whole real parameters of commutation devices. Finally, it is important to remark that the Simulated Annealing algorithm is a heuristic method. This means that it can give slightly different solutions in each run.

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