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Investigations on Performance Metrics of FINFET based 8- Bit Low Power Adder Architectures Implemented using Various Logic Styles

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Abstract

Objectives: To reduce the leakage power dissipation and minimize the propagation delay, a Fin FET based 8-bit adder architecture is constructed. The performance metrics of these structures are calculated over a range of temperatures and are compared with the MOSFET based 8-bit adder architecture. Various logic styles are utilized for constructing the adder. **Method/Analysis:** A Ripple carry adder structure is employed. The existing adder architecture is constructed using 90nm MOSFET technology. The proposed adder architecture is constructed using 32nm FINFET technology. The various logic styles employed are Complementary Metal-Oxide Semiconductor logic (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission Gate logic (TG) and Gate Diffusion Input logic (GDI). Cadence Virtuoso is used for designing purpose and simulation is performed using Spectre. **Findings**: Key performance metrics like static power, dynamic power, leakage power, delay and power delay product are calculated. The dynamic power of MOSFET architecture ranges from 7.42μW to 882.6μW. The dynamic power of FINFET architecture ranges from 0.407nW to 156.2nW. The static power (inputs at high logic level) of MOSFET architecture ranges from 0.001μW to 945.76μW. The static power (inputs at high logic level) of Fin FET architecture ranges from 0.725pW to 170.4nW. The static power (inputs at low logic level) of MOSFET architecture ranges from 0.94nW to 1.68mW. The static power (inputs at low logic level) of Fin FET architecture ranges from 0.127pW to 305.3nW. The leakage power (inputs at high logic level) of MOSFET architecture ranges from 1.27nW to 134.7μW. The leakage power (inputs at high logic level) of Fin FET architecture ranges from 0.36pW to 24.77nW. The leakage power (inputs at low logic level) of MOSFET architecture ranges from 0.54nW to 139.9μW. The leakage power (inputs at low logic level) of Fin FET architecture ranges from 0.15nW to 227.6nW. The delay of MOSFET architecture ranges from 0.344μs to 0.46μs. The delay of Fin FET architecture ranges from 0.19μs to 0.28μs. The power delay product of MOSFET architecture ranges from 2.66 to 405.99. The power delay product of Fin FET architecture ranges from 0.83 to 29.67. **Novelty/Improvements:** The FINFET adder architecture proved to be effective in reducing the propagation delay and leakage power dissipation. This may find usage in high performance devices like microchips and supercomputers.

Keywords: Complementary Pass-transistor Logic, Gate Diffusion Input, Low Power Adder, Transmission Gate, CMOS, FINFET

1. Introduction

In recent years, the leakage power has become predominant power dissipation due to the scaling of the feature size to sub nanometer level. As the device feature size is scaled down, the threshold voltages are also scaled down to a minimum level, which exponentially increases the

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leakage during the standby mode especially when all NMOS devices are in cut-off state. Hence, it is mandatory to minimize the leakage power during the cut-off state of the transistors. Fin FET transistors are used to minimize the leakage power since the multi-gate structure of the Fin FET minimizes the leakage power during cut-off state.

Many techniques have been employed to overcome power dissipation issues. A novel technique of constructing such an adder is described in[1], where different logic styles like CMOS, CPL, TG are employed for designing a 1-bit FINFET added. Comparatively, the proposed TG-based full adder was the most successful design. The TG-based adder had the least power consumption. A similar technique was used in[2] where a 1-bit adder was designed using a Double Gate (DG) Fin FET at 45nm technology. It was observed that the adder designed using DG Fin FET has shown leakage power reduction from 1.594pW to 1.09pW and leakage current reduction from 652.4n A to 1.71n A as compared with the CMOS 1-bit full adder cell. An ultra-low power 32-bit adder was designed in[3] which made use of a 45nm Fin FET. In this study, the dynamic energy and static energy show an inverse behavior with the increase in supply voltage. This adder consumed only 10fJ for a single operation. The supply voltage provided was less than 100mV. A 1-bit full adder technique using Fin FET technology is presented in[4] where various performance metrics like dissipation power, Power Delay Product (PDP) and Energy Delay Product (EDP) were calculated. The proposed Fin FET architecture provided 97% decrease in power dissipation and 99% reduction in PDP and EDP.

Another pioneering adder technique is employed in[5] where a 32nm Fin FET structure is used and the circuit is designed using Cell Design Methodology (CDM). CDM technique employs less number of transistors in the critical path. These adders have a delay reduction of 54% to 95%, power delay product reduction of 33% to 76%, energy efficiency is improved from 78% to 84%. A 1-bit full adder cell is investigated in[6] where a GDI cell and DG structures are used. DG structures help in overcoming the effects of short channel effects. Independent Gate Control method is used in the circuit. GDI technique helps in the minimizing the number of transistors deployed. The proposed adder dissipated a power of 0.529μW and it had a delay of 32.82ps. In[7] various cell design like mirror adder, 14T adder, TG based adder and adder using pass transistor were simulated. The number of transistors in mirror adder is reduced from 14 to 10 and the proposed structure also has 25% reduced leakage power. The leakage current was significantly reduced using 14T added. The leakage current was reduced by a factor of 6 by using the TG model of adder. In pass transistor adder, the leakage current was reduced by a factor of 17. Compared to all the models, 14T adder was highly recommended.

Taking into consideration of the above, this paper contributes to the following:

- Realize 8-bit Ripple Carry Adder in 90nm MOSFET and 32nm Fin FET technology.
- Various logic styles like CPL, CMOS, TG, and GDI are employed.
- Performance metrics like Dynamic power, Static power, Leakage power, and Delay and Power delay product are measured.

2. Simulation Results and Discussion

The performance metrics are measured for every 25°C increase in temperature (-25°Cto 125°C). The width of a PMOS transistor in MOSFET adder is 480 nm. The width of a NMOS transistor in MOSFET adder is 120 nm. The length of both PMOS and NMOS transistor in MOSFET structure is 100 nm. The supply voltage is provided with 1V. The width of a PMOS transistor in Fin FET adder is 100 nm. The width of a NMOS transistor in Fin FET adder is 50 nm. The length of both PMOS and NMOS transistor in MOSFET structure is 32 nm. The supply voltage is provided with 500mV.

The Figure 1 depicts the schematic of 8-bit MOSFET adder implemented in CMOS logic. The Figure 2 repre-

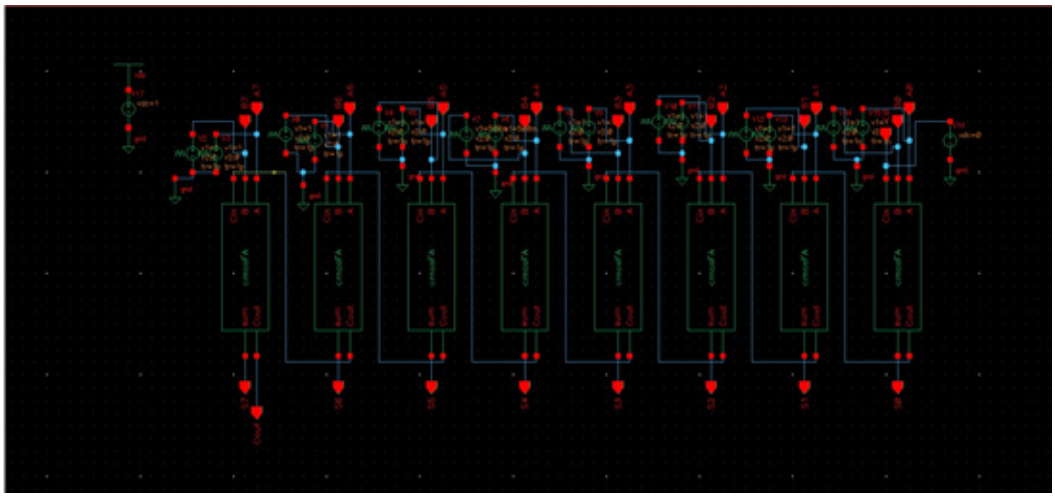

Figure 1. Schematic of 8-bit MOSFET adder in CMOS logic.

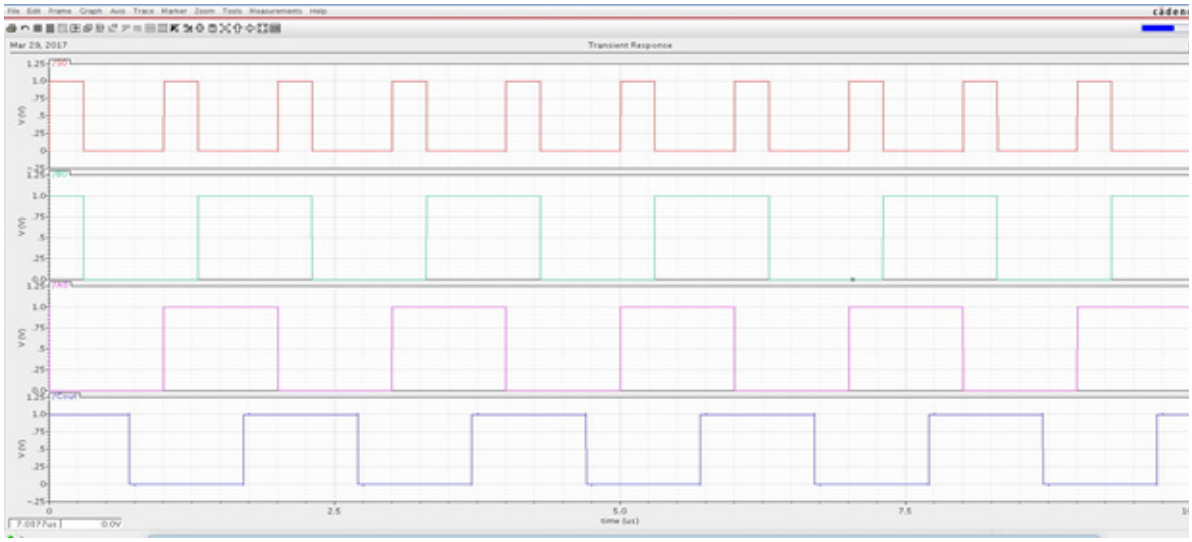

Figure 2. I/O waveform of 8-bit MOSFET adder in CMOS logic.

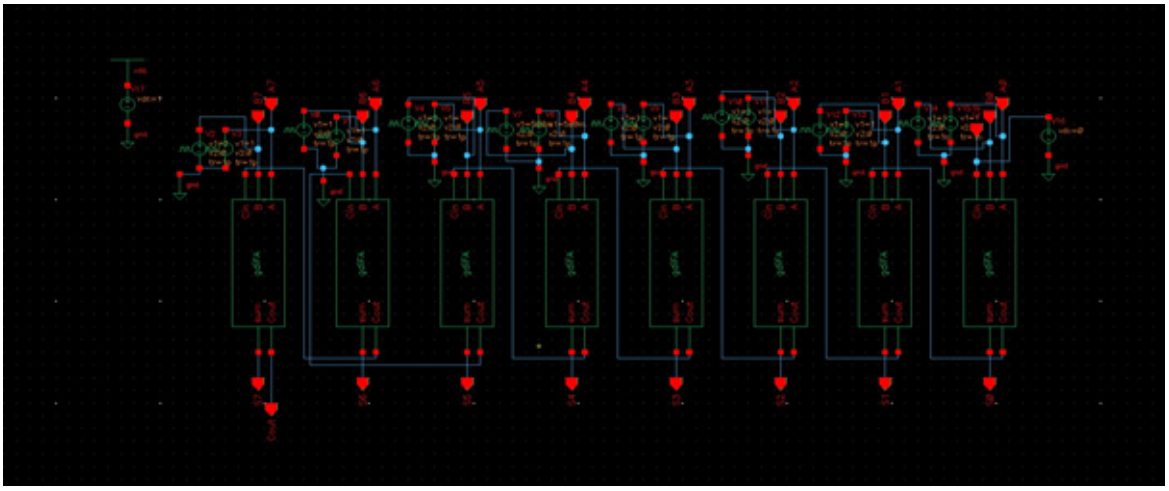

Figure 3. Schematic of 8-bit MOSFET adder in GDI logic.

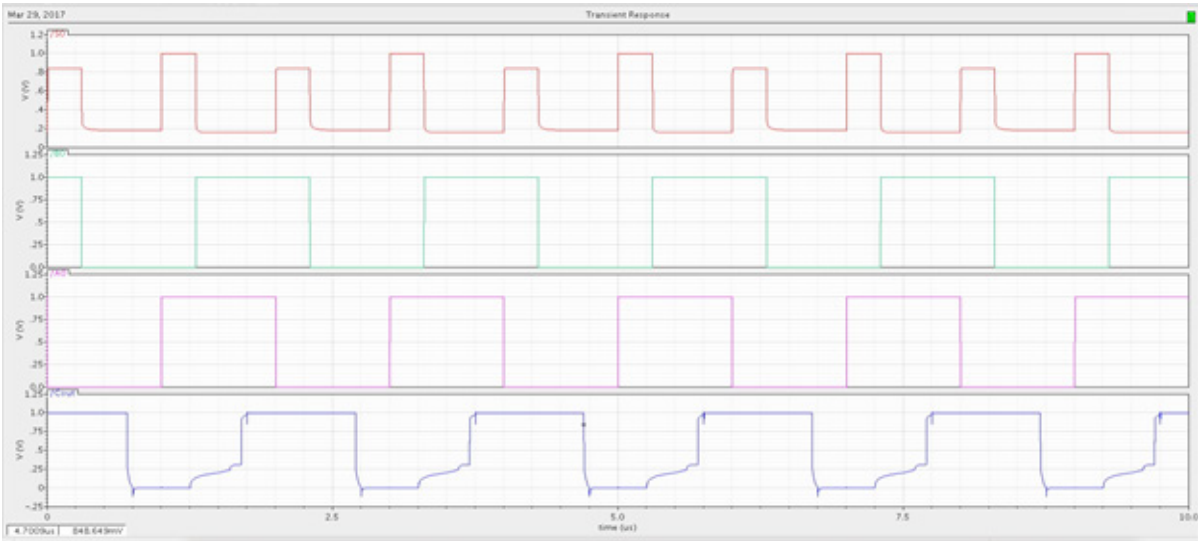

Figure 4. I/O waveform of 8-bit MOSFET adder in GDI logic.

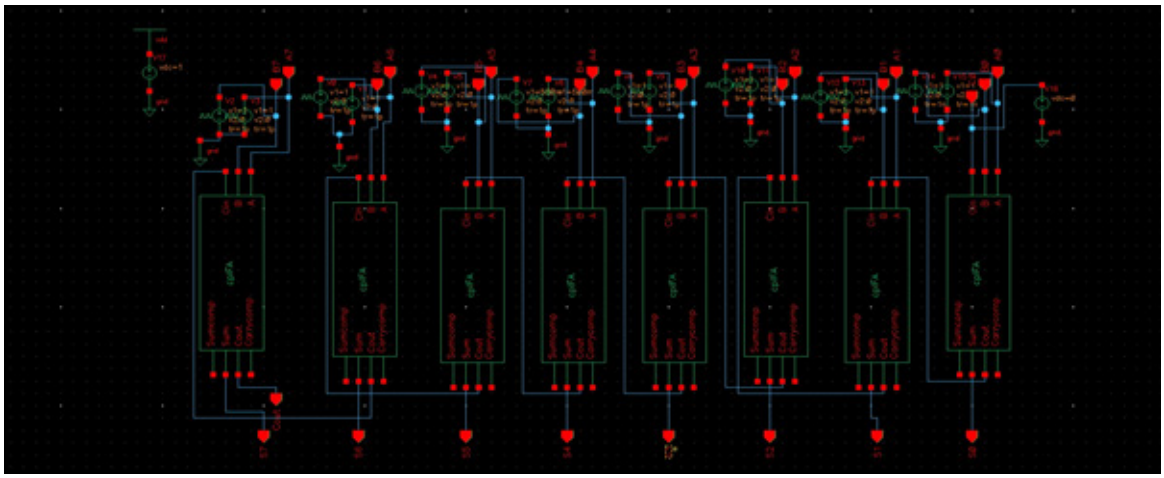

Figure 5. Schematic of 8-bit MOSFET adder in CPL logic.

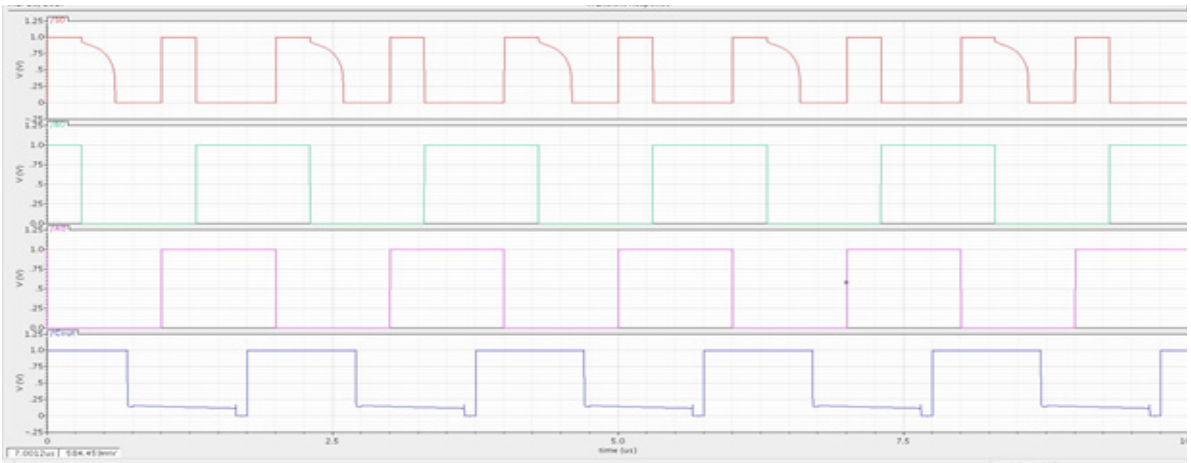

Figure 6. I/O waveform of 8-bit MOSFET adder in CPL logic.

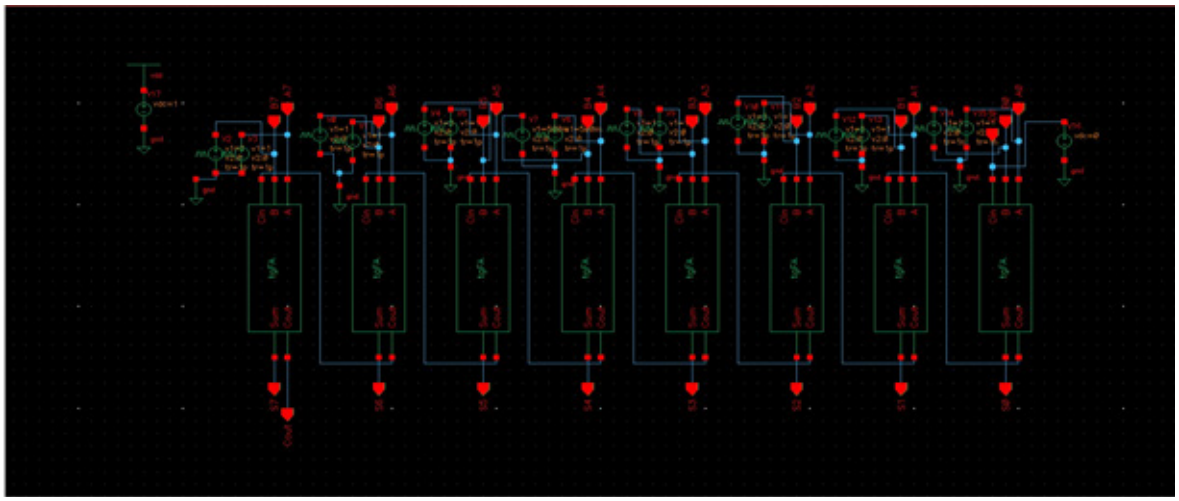

Figure 7. Schematic of 8-bit MOSFET adder in TG logic.

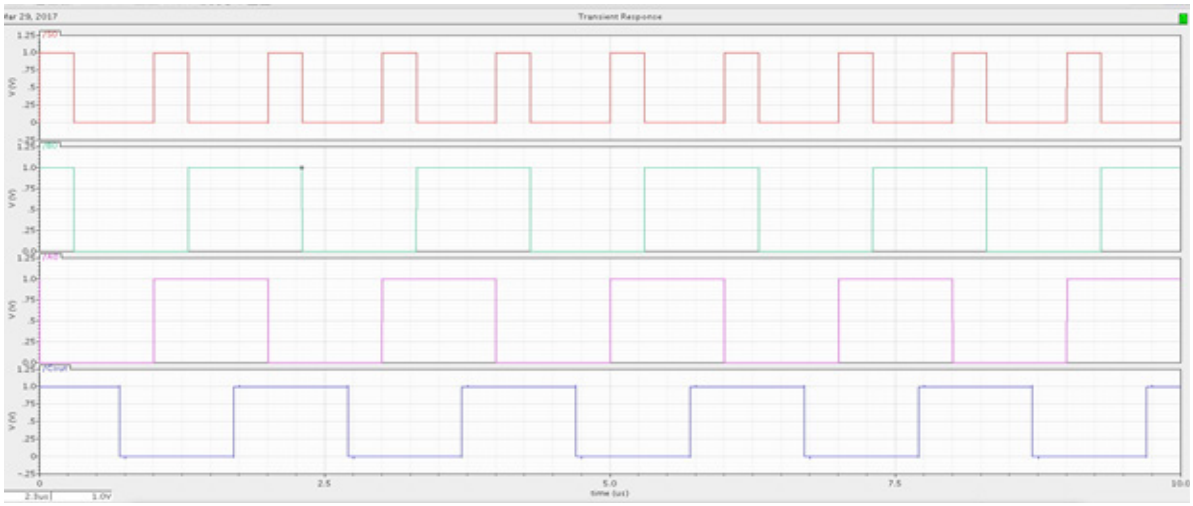

Figure 8. I/O waveform of 8-bit MOSFET adder in TG logic.

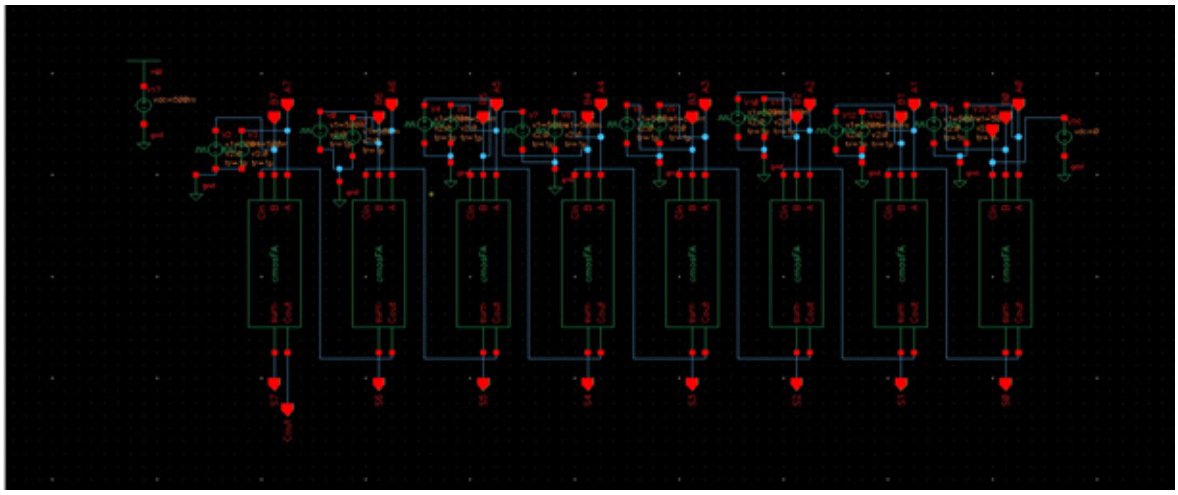

Figure 9. Schematic of 8-bit FinFET adder in CMOS logic.

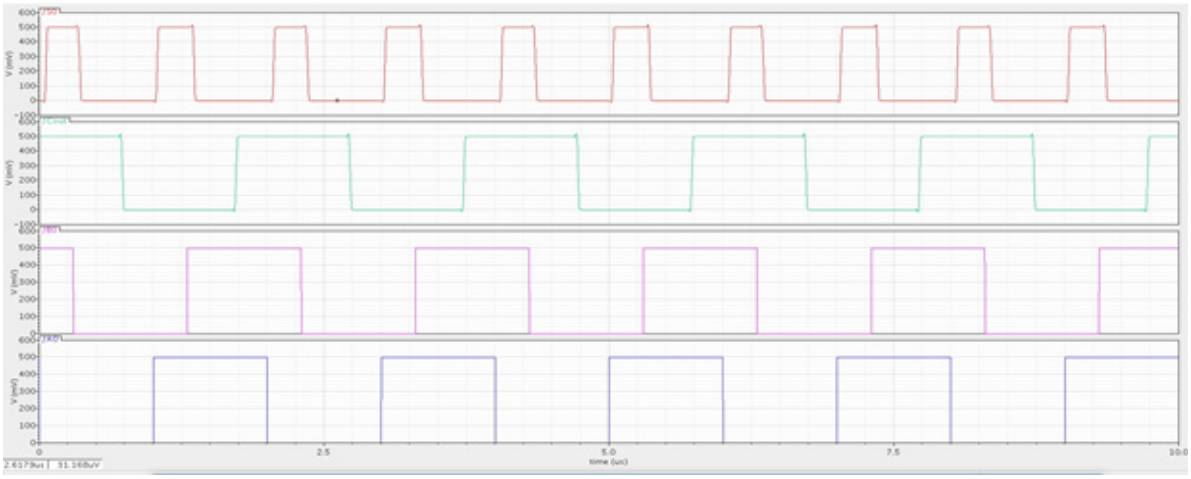

Figure 10. I/O waveform of 8-bit FinFET adder in CMOS logic.

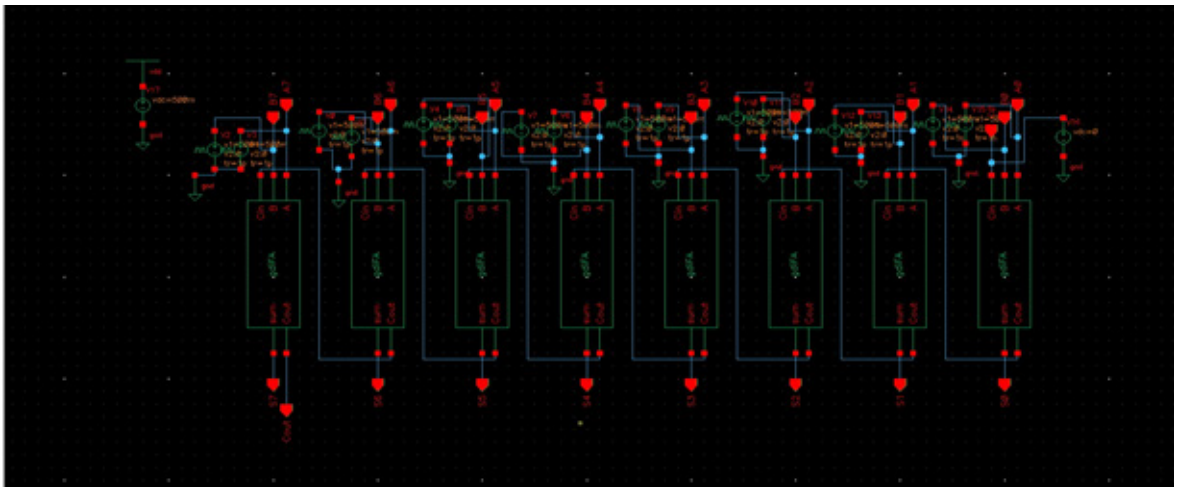

Figure 11. Schematic of 8-bit FinFET adder in GDI logic.

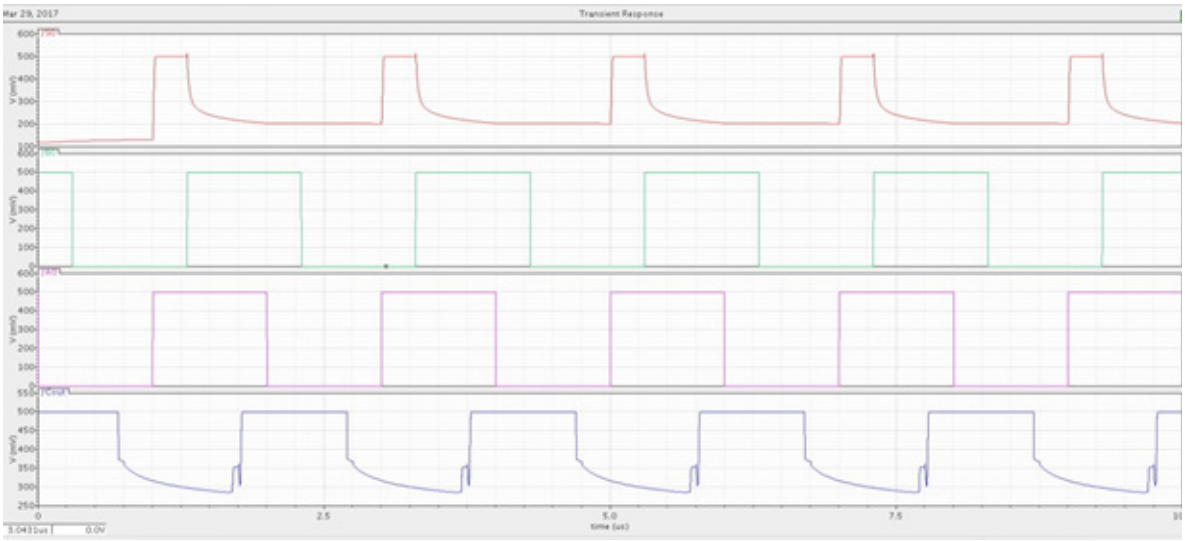

Figure 12. I/O waveform of 8-bit FinFET adder in GDI logic.

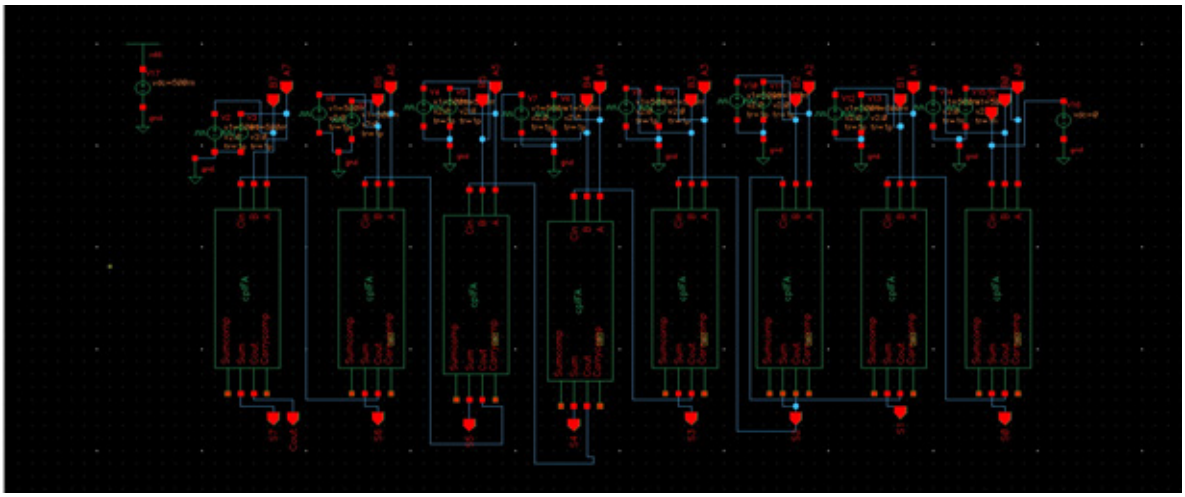

Figure 13. Schematic of 8-bit FinFET adder in CPL logic.

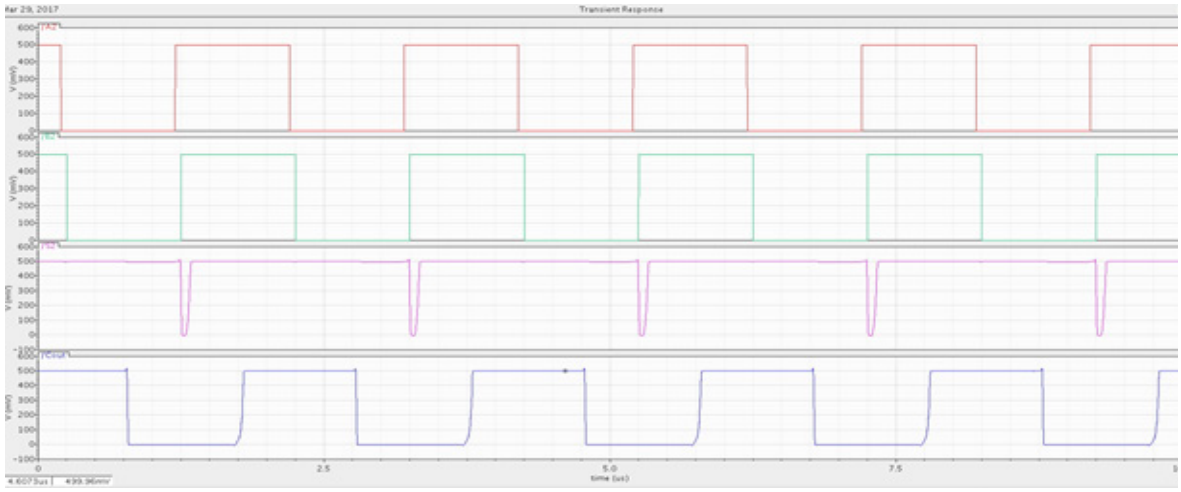

Figure 14. I/O waveform of 8-bit FinFET adder in CPL logic.

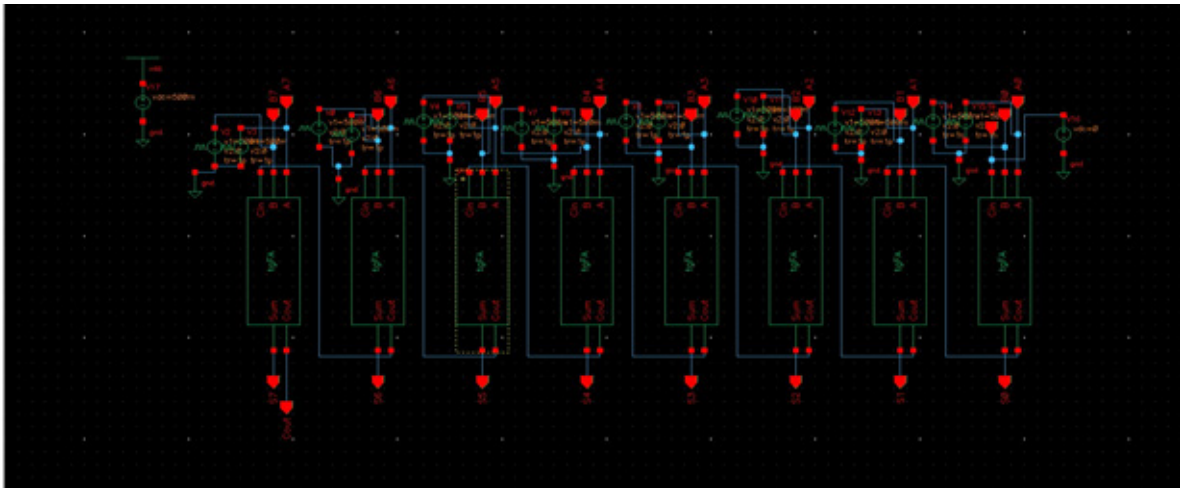

Figure 15. Schematic of 8-bit FinFET adder in TG logic.

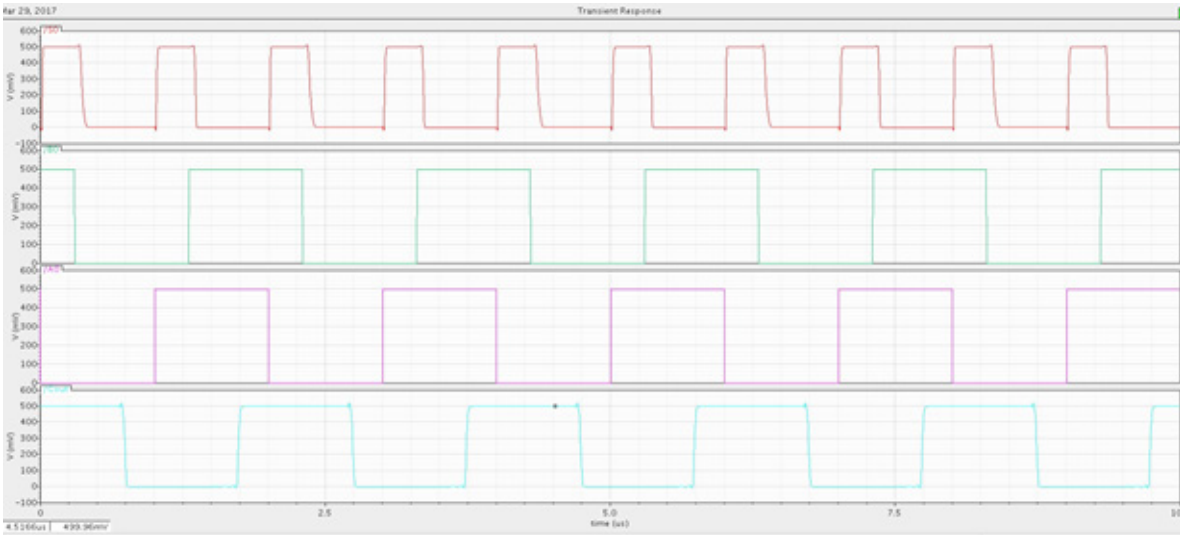

Figure 16. I/O waveform of 8-bit FinFET adder in TG logic.

Table 1. Performance metrics of 8-bit MOSFET adder in CMOS logic

Temperature		All 0's		All 1's			
	Dynamic Power	Static Power	Leakage Power	Static Power	Leakage Power	Delay	Power Delay Product
(Celsius)	(µW)	(µW)	(µW)	(µW)	(µW)	(µs)	
-25	6.41	0.469	2.42	0.001	3.601	0.41	2.62
0	8.76	0.613	4.071	0.0125	5.481	0.404	3.54
25	11.86	1.14	5.79	0.081	7.67	0.4	4.63
50	15.03	1.56	8.143	0.187	10.17	0.399	5.99
75	18.94	2.19	10.96	0.244	12.99	0.395	7.48
100	23.33	2.88	14.25	0.313	16.47	0.389	9.07
125	28.65	3.61	18.47	0.429	20.51	0.386	1.39

sents the Input / Output (I/O) waveform of this adder. Table 1 contains the information about variation of the performance metrics of this adder in accordance to the range of temperatures. Figure 3 depicts the schematic of 8-bit MOSFET adder implemented in GDI logic. The Figure 4 represents the Input / Output (I/O) waveform of this adder. Table 2 contains the information about variation of the performance metrics of this adder in accordance to the range of temperatures. Figure 5 depicts the schematic of 8-bit MOSFET adder implemented in CPL logic. The Figure 6 represents the Input / Output (I/O) waveform of this adder. Table 3 contains the information about variation of the performance metrics of this adder in accordance to the range of temperatures. Figure 7 depicts the schematic of 8-bit MOSFET adder implemented in TG logic. The Figure 8 represents the Input / Output (I/O) waveform of this adder. Table 4 contains the information about variation of the performance metrics of this adder in accordance to the range of temperatures. Figure 9 depicts the schematic of 8-bit Fin FET adder implemented in CMOS logic. The Figure 10 represents the Input / Output (I/O) waveform of this adder. Table 5 contains the information about variation of the performance metrics of this adder in accordance to the range of temperatures. Figure 11 depicts the schematic of 8-bit Fin FET adder implemented in GDI logic. The Figure 12 represents the Input / Output (I/O) waveform of this adder. Table 6 contains the information about variation of the performance metrics of this adder in accordance to the range of temperatures. Figure 13 depicts the schematic of

Table 2. Performance metrics of 8-bit MOSFET adder in GDI logic

Temperature		**All 0's**		**All 1's**			
	Dynamic Power	**Static Power**	**Leakage Power**	**Static Power**	**Leakage Power**	**Delay**	**Power Delay Product**
(Celsius)	**(µW)**	**(nW)**	**(µW)**	**(µW)**	**(nW)**	**(µs)**	
-25	13.68	0.94	0.54	0.024	1.27	0.344	4.71
0	10.36	0.23	0.82	0.032	4.01	0.346	3.58
25	8.59	1.17	1.15	0.049	10.83	0.35	3.01
50	7.72	6.83	1.53	0.086	24.97	0.351	2.702
75	7.37	4.71	1.97	0.151	49.98	0.355	2.61
100	7.3	2.12	2.47	0.254	96.8	0.358	2.6
125	7.42	25.68	3.01	0.447	157.8	0.359	2.66

Table 3. Performance Metrics of 8-bit MOSFET adder in CPL logic

Temperature		All 0's		All 1's			
	Dynamic Power	Static Power	Leakage Power	Static Power	Leakage Power	Delay	Power Delay Product
(Celsius)	(µW)	(mW)	(µW)	(µW)	(µW)	(µs)	
-25	882.6	1.68	139.9	945.76	134.7	0.46	405.99
0	807.3	1.59	147.88	752.3	119.8	0.457	368.99
25	727.56	1.25	151.98	678.65	108.6	0.45	327.41
50	643.28	1.1	149.7	605.1	98.03	0.449	283.04
75	587.71	1.05	98.88	543.8	88.15	0.448	263.2
100	541.14	1.03	48.54	491.4	80.43	0.443	239.7
125	496.56	1.006	21.76	446.2	74.78	0.44	218.05

Table 4. Performance metrics of 8-bit MOSFET adder in TG logic

Temperature		All 0's		All 1's			
	Dynamic Power	Static Power	Leakage Power	Static Power	Leakage Power	Delay	Power Delay Product
(Celsius)	(µW)	(µW)	(µW)	(µW)	(µW)	(µs)	
-25	11.56	0.027	9.75	3.2	3.2	0.36	4.16

Table 4 Continued

0	16.29	0.34	14.34	4.87	5.01	0.366	5.96
25	22	0.38	20.33	6.68	7.1	0.38	8.36
50	28.55	0.44	27.02	8.91	9.75	0.385	10.99
75	36.07	0.877	34.26	11.28	12.81	0.4	14.42
100	44.57	1.53	42.06	13.93	16.57	0.408	18.18
125	54.18	2.89	50.42	16.85	21.17	0.42	22.74

Table 5. Performance metrics of 8-bit FinFET adder in CMOS logic

Temperature		**All 0's**		**All 1's**			
	Dynamic Power	**Static Power**	**Leakage Power**	**Static Power**	**Leakage Power**	**Delay**	**Power Delay Product**
(Celsius)	**(nW)**	**(nW)**	**(nW)**	**(pW)**	**(nW)**	**(µs)**	
-25	2.98	0.226	1.121	0.725	1.69	0.28	0.83
0	4.08	0.278	1.889	5.79	2.55	0.26	1.06
25	5.41	0.527	2.708	37.67	3.56	0.25	1.35
50	7.01	0.762	3.78	92.13	4.72	0.22	1.54
75	8.81	1.01	5.116	113.17	6.054	0.19	1.67
100	10.87	1.338	6.65	151.67	7.63	0.18	1.95
125	13.27	1.671	8.581	198.7	9.536	0.15	1.99

Table 6. Performance metrics of 8-bit FinFET adder in GDI logic

Temperature		**All 0's**		**All 1's**			
	Dynamic Power	**Static Power**	**Leakage Power**	**Static Power**	**Leakage Power**	**Delay**	**Power Delay Product**
(Celsius)	**(nW)**	**(pW)**	**(nW)**	**(pW)**	**(pW)**	**(µs)**	
-25	4.04	0.27	0.15	7.31	0.368	0.235	0.94
0	2.94	0.069	0.23	9.47	1.18	0.239	0.71
25	2.53	0.034	0.33	14.69	3.2	0.24	9.61
50	2.28	2.01	0.45	25.47	7.38	0.243	0.55
75	2.17	1.393	0.68	44.92	14.76	0.2477	0.53
100	2.15	0.626	0.72	75.51	28.62	0.248	0.529
125	2.189	7.59	0.89	133.51	46.66	0.25	0.54

Table 7. Performance metrics of 8-bit FinFET adder in CPL logic

Temperature		All 0's		All 1's			
	Dynamic Power	Static Power	Leakage Power	Static Power	Leakage Power	Delay	Power Delay Product
(Celsius)	(nW)	(nW)	(nW)	(nW)	(nW)	(µs)	
-25	156.2	305.3	25.77	170.4	24.77	0.19	29.67

Table 3 Continued

0	142	291.1	27.19	134.9	22.08	0.196	27.83
25	127.8	227.2	27.69	120.7	19.8	0.2	25.56
50	113.6	198.8	27.33	106.5	17.89	0.21	23.86
75	106.5	191.7	18.17	99.4	16.25	0.22	23.43
100	99.4	184.6	8.73	85.2	14.83	0.225	22.36
125	85.2	177.5	3.9	78.1	13.63	0.23	19.59

Table 8. Performance metrics of 8-bit FinFET adder in TG logic

Temperature		**All 0's**		**All 1's**			
	Dynamic Power	**Static Power**	**Leakage Power**	**Static Power**	**Leakage Power**	**Delay**	**Power Delay Product**
(Celsius)	**(nW)**	**(nW)**	**(nW)**	**(nW)**	**(nW)**	**(μs)**	
-25	52.1	0.125	44	14.65	14.87	0.222	11.4
0	73.45	1.622	64.67	21.95	22.57	0.225	16.52
25	99.1	2.03	92.02	30.57	32.25	0.23	22.79
50	128.95	2.037	121.7	40.5	43.95	0.24	30.94
75	162.82	3.97	154.42	51.25	58	0.243	39.56
100	200.82	7.225	189.77	62.92	74.8	0.248	49.8
125	244.5	13.05	227.6	76.22	95.73	0.25	61.12

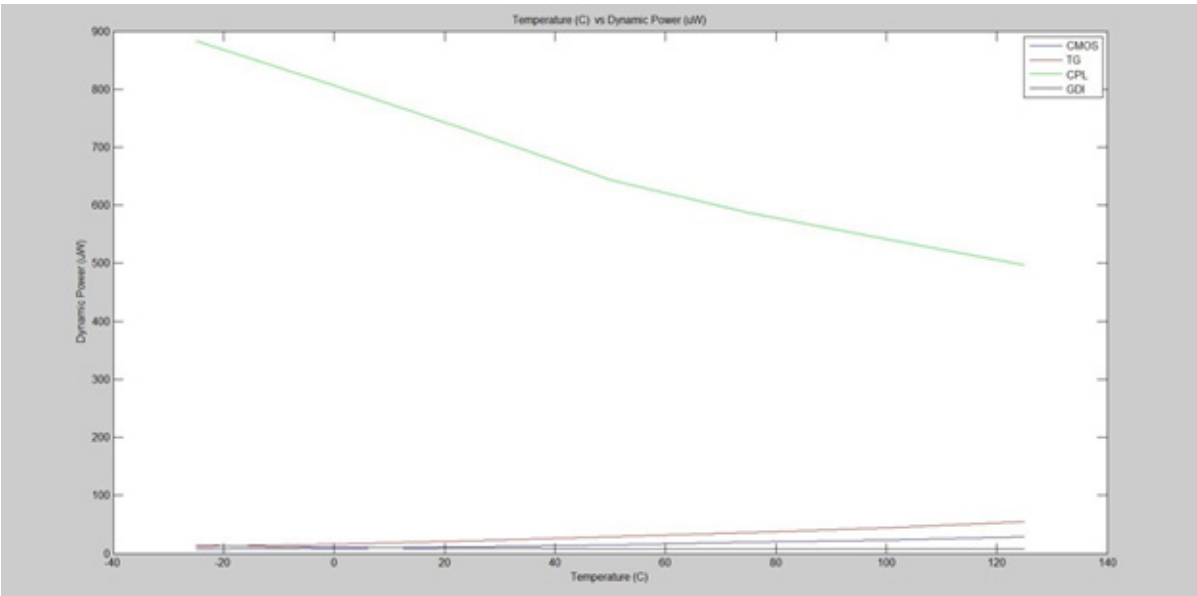

Figure 17. Dynamic power of 8-bit MOSFET adder.

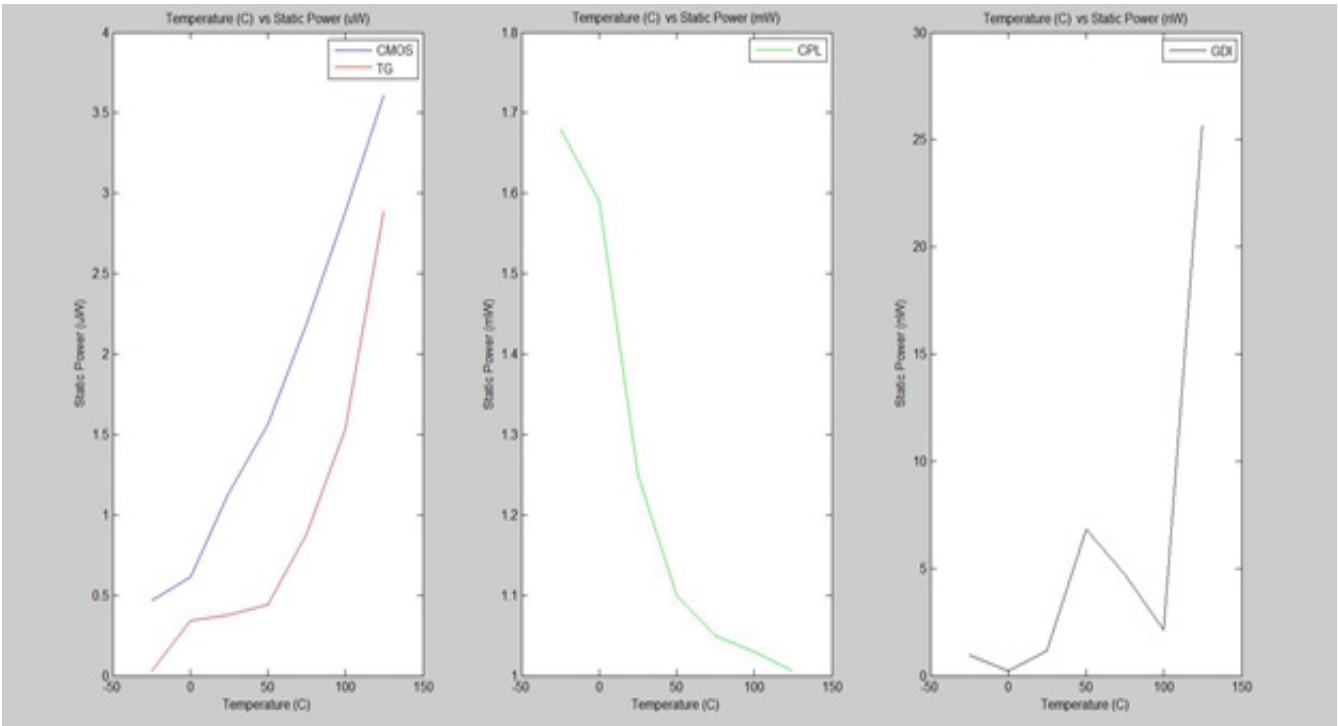

Figure 18. Static power (inputs at low logic level) of 8-bit MOSFET adder.

8-bit Fin FET adder implemented in CPL logic. The Figure 14 represents the Input / Output (I/O) waveform of this adder. Table 7 contains the information about variation of the performance metrics of this adder in accordance to the

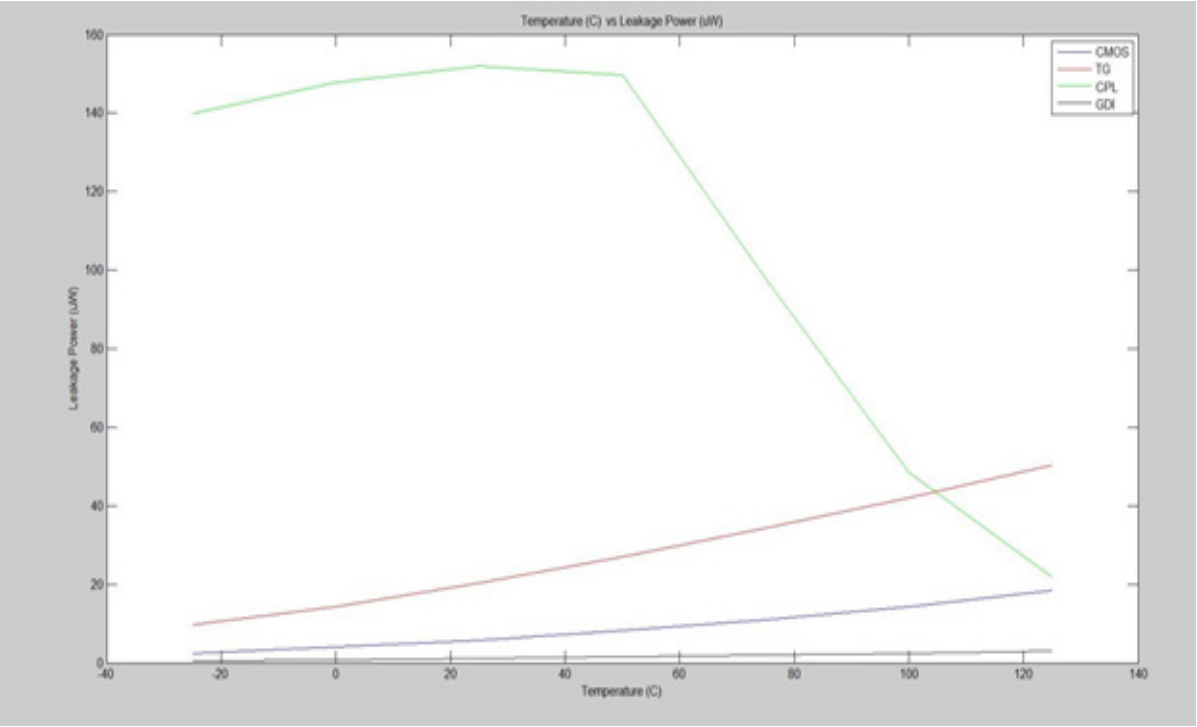

Figure 19. Leakage power (inputs at low logic level) of 8-bit MOSFET adder.

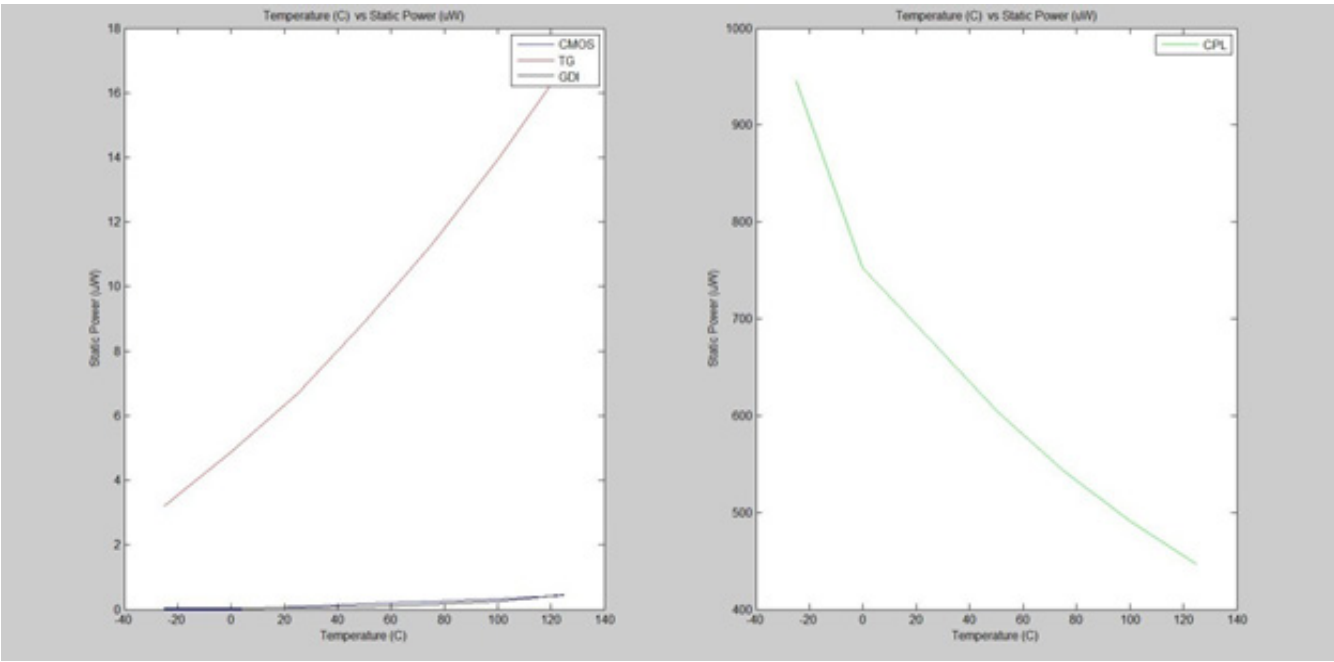

Figure 20. Static power (inputs at high logic level) of 8-bit MOSFET adder.

range of temperatures. Figure 15 depicts the schematic of 8-bit Fin FET adder implemented in TG logic. The Figure 16 represents the Input / Output (I/O) waveform of this adder. Table 8 contains the information about variation

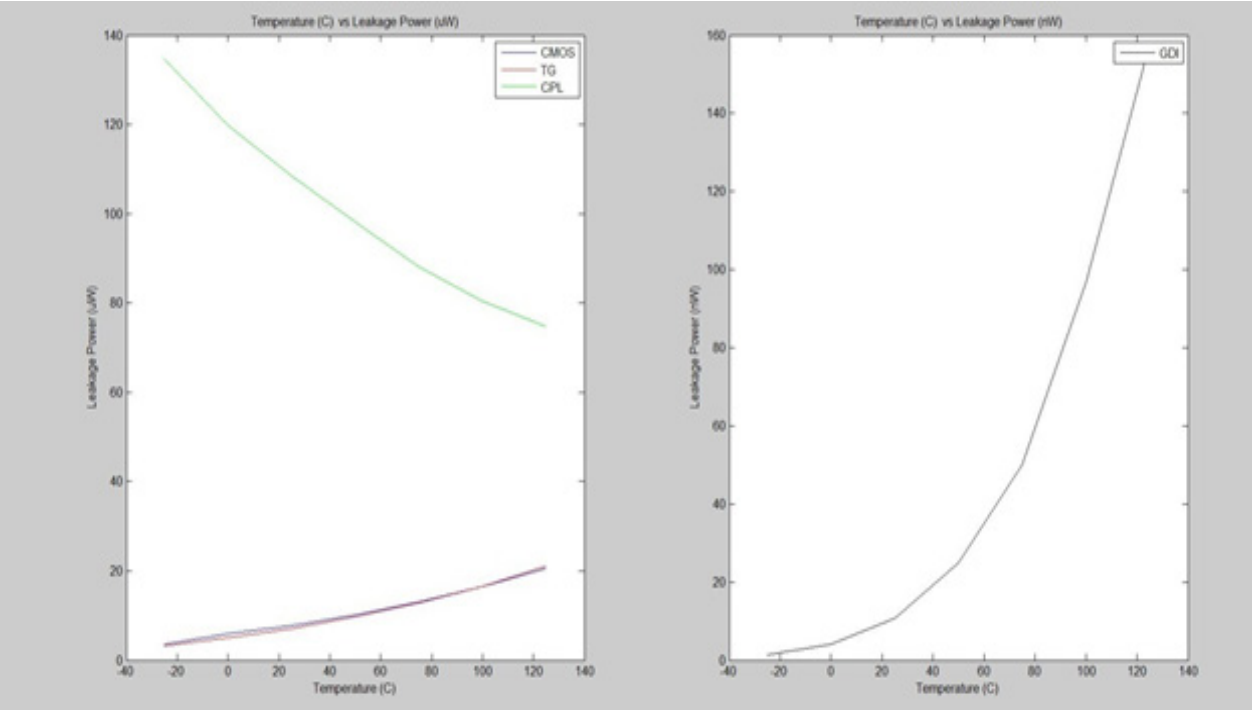

Figure 21. Leakage power (inputs at high logic level) of 8-bit MOSFET adder.

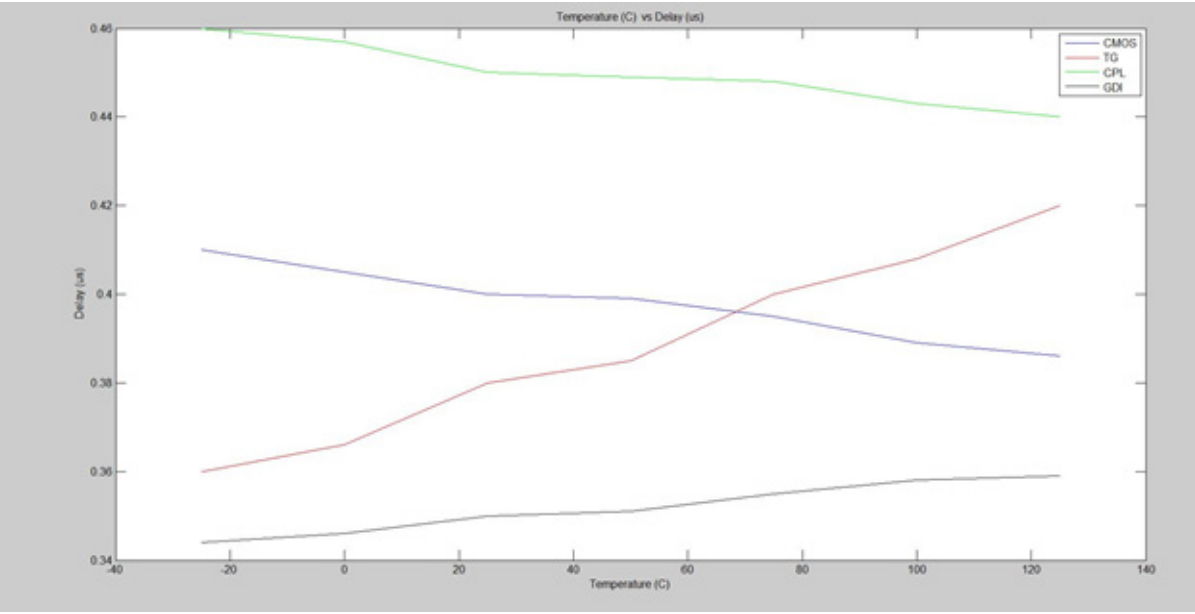

Figure 22. Propagation delay of 8-bit MOSFET adder.

of the performance metrics of this adder in accordance to the range of temperatures.

The dynamic power of 8-bit MOSFET adder (for all logic styles) is correlated with range of temperature val-

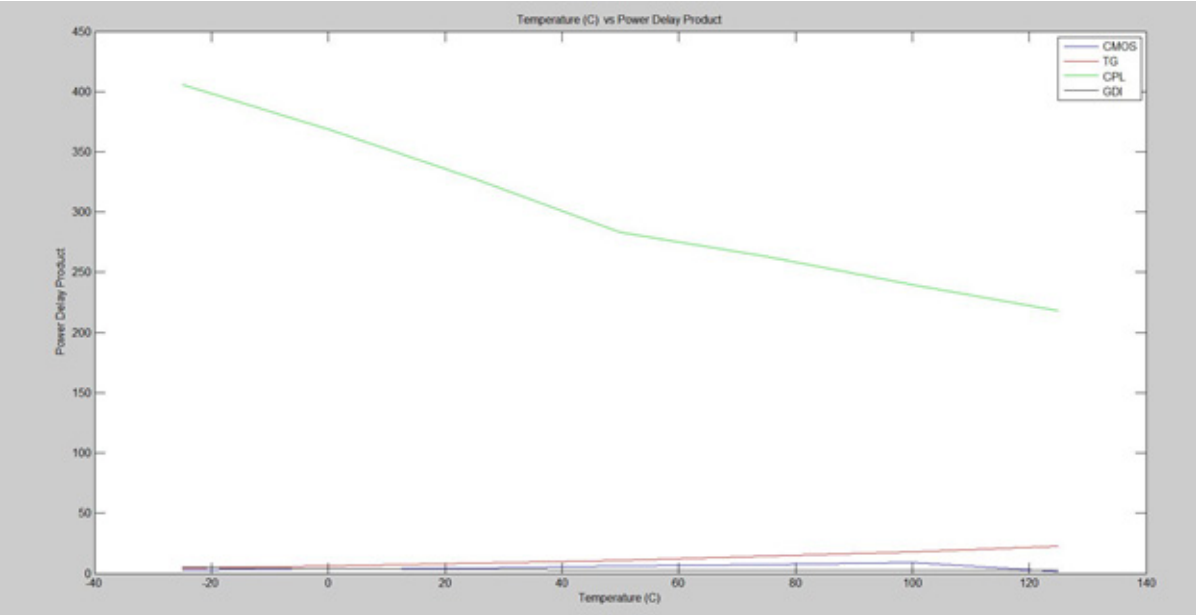

Figure 23. Power delay Product of 8-bit MOSFET adder.

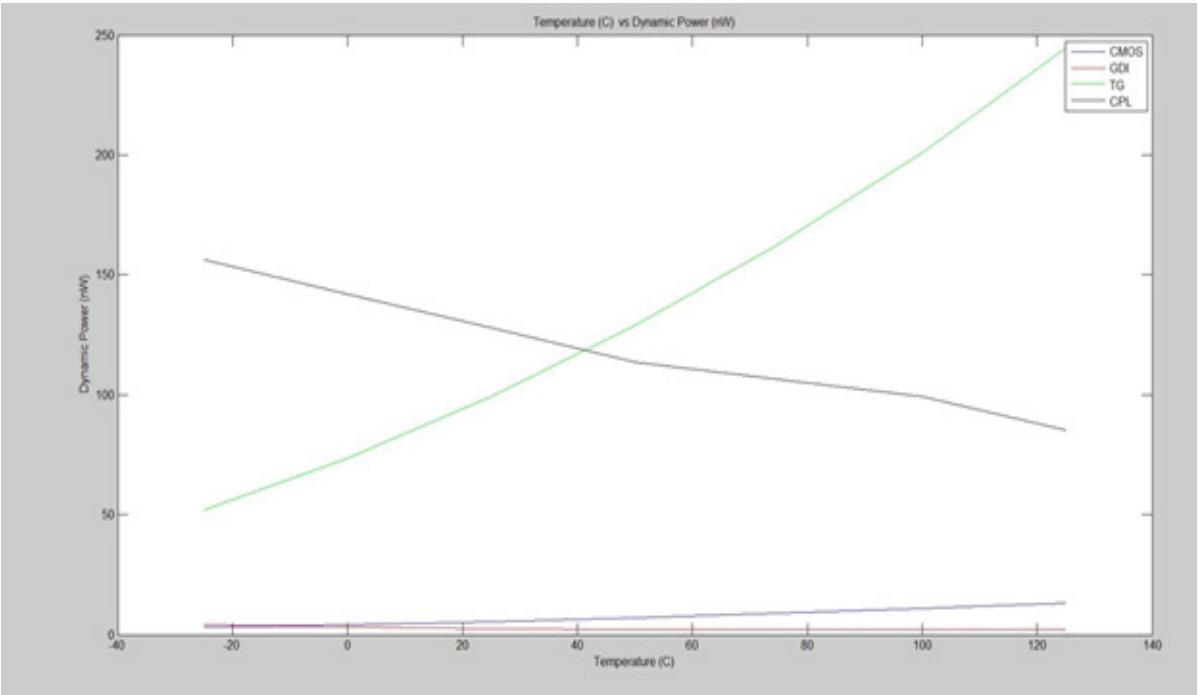

Figure 24. Dynamic power of 8-bit FinFET adder.

ues, is graphically represented in Figure 17. The static power (inputs at low logic level) of 8-bit MOSFET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 18. The

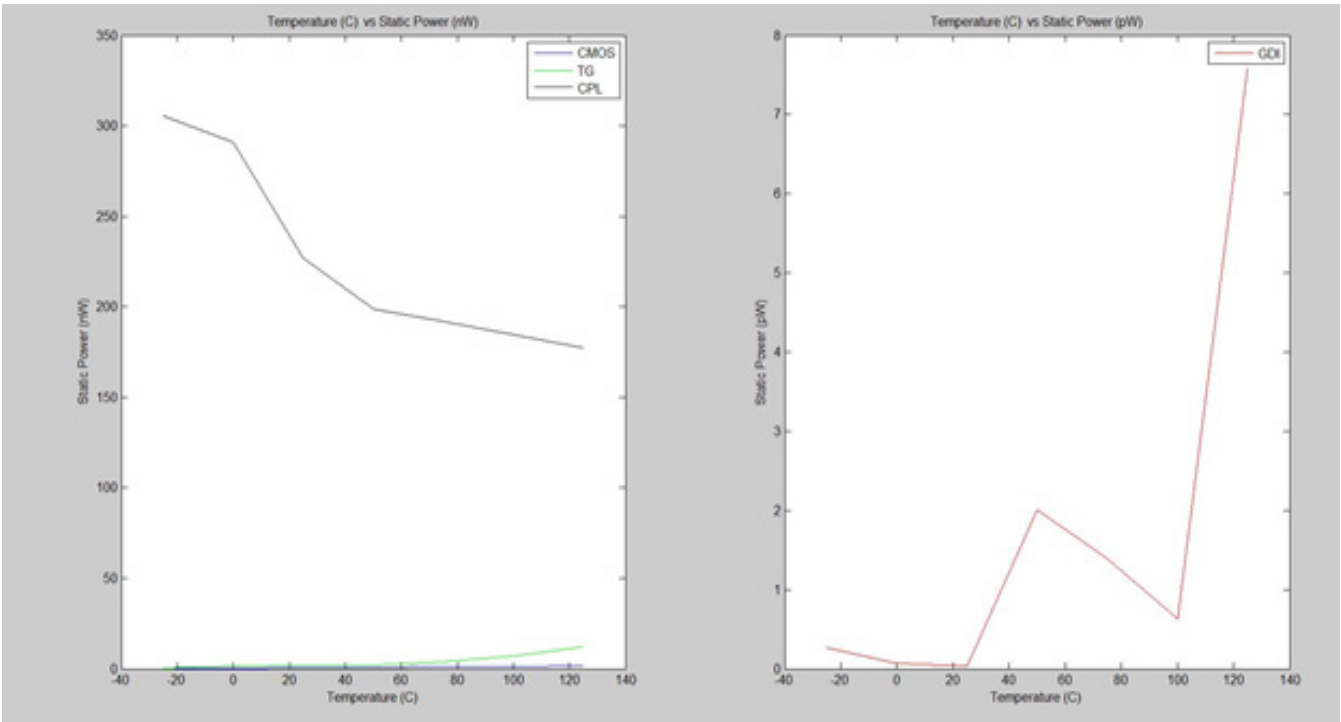

Figure 25. Static power (inputs at low logic level) of 8-bit FinFET adder.

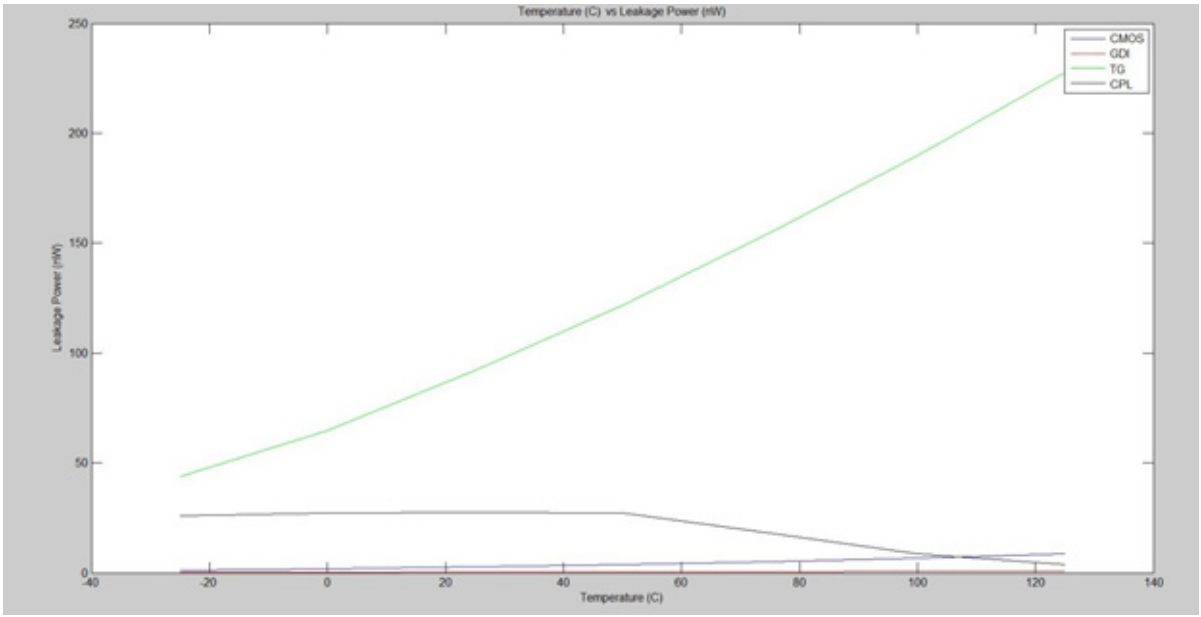

Figure 26. Leakage power (inputs at low logic level) of 8-bit FinFET adder.

leakage power (inputs at low logic level) of 8-bit MOSFET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 19. The static power (inputs at high logic level) of 8-bit

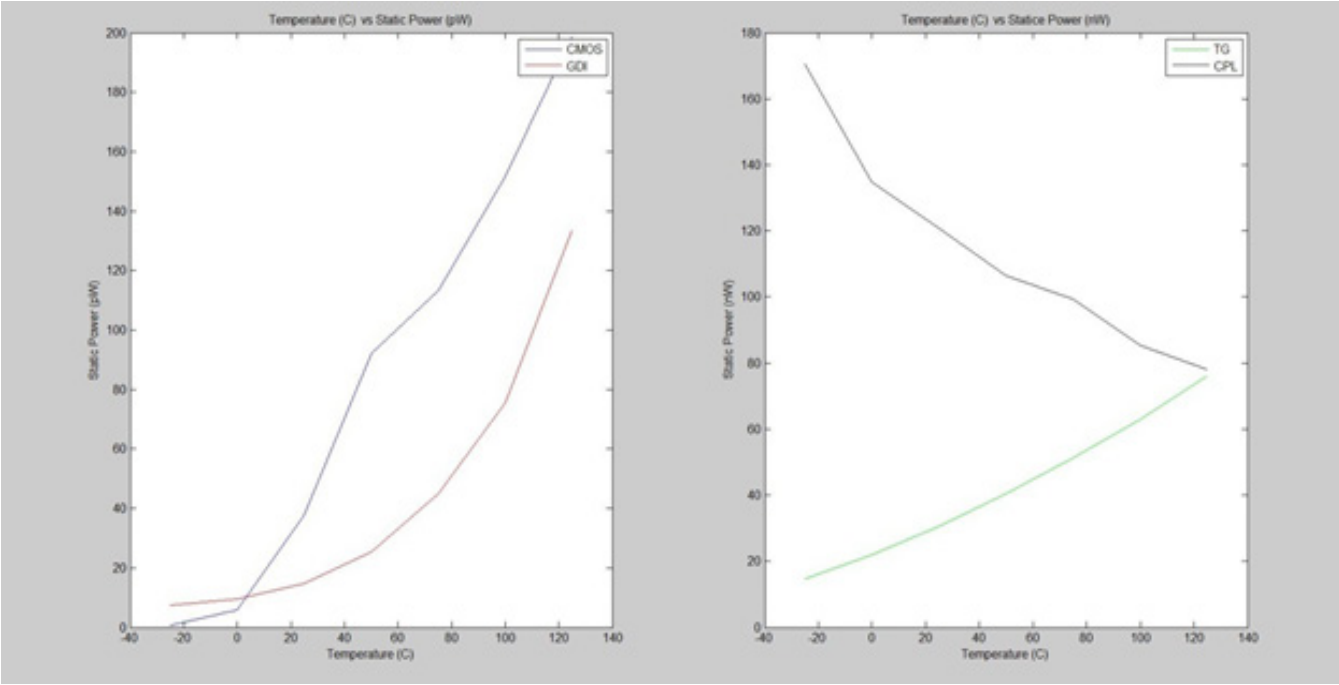

Figure 27. Static power (inputs at high logic level) of 8-bit FinFET adder.

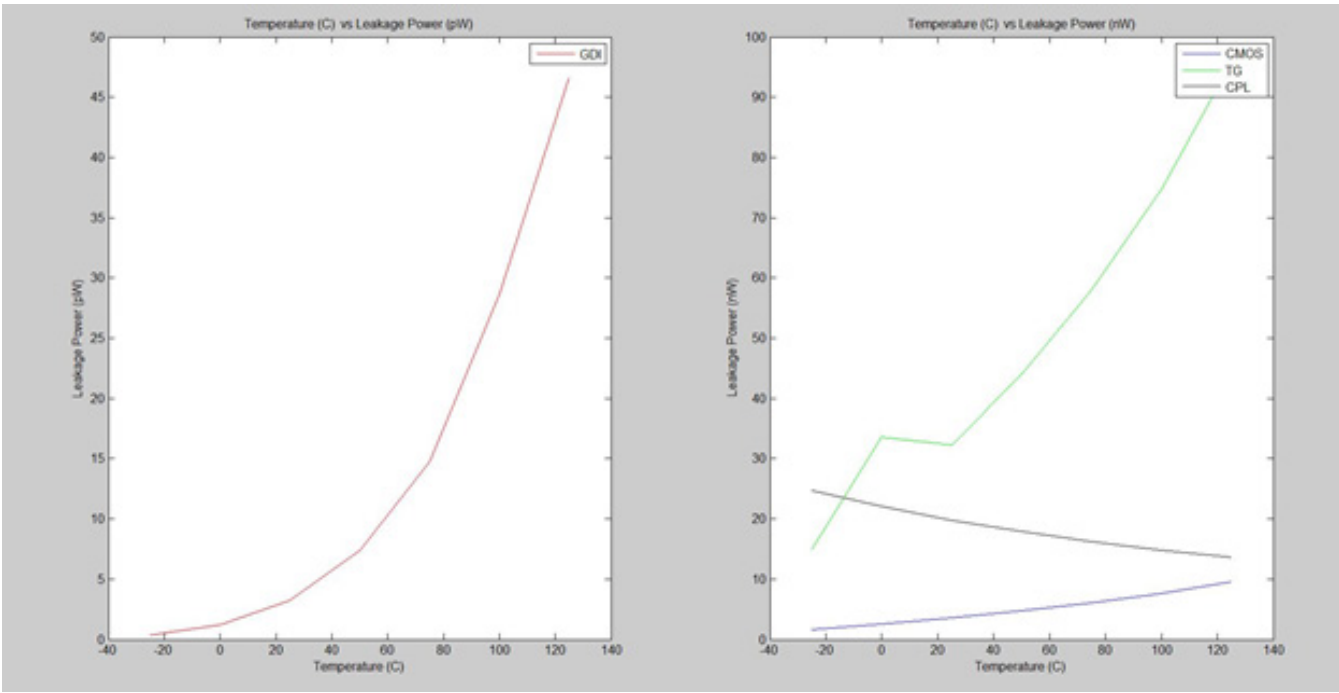

Figure 28. Leakage power (inputs at high logic level) of 8-bit FinFET adder.

MOSFET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 20. The leakage power (inputs at high logic level) of 8-bit MOSFET adder (for all logic styles) is correlated

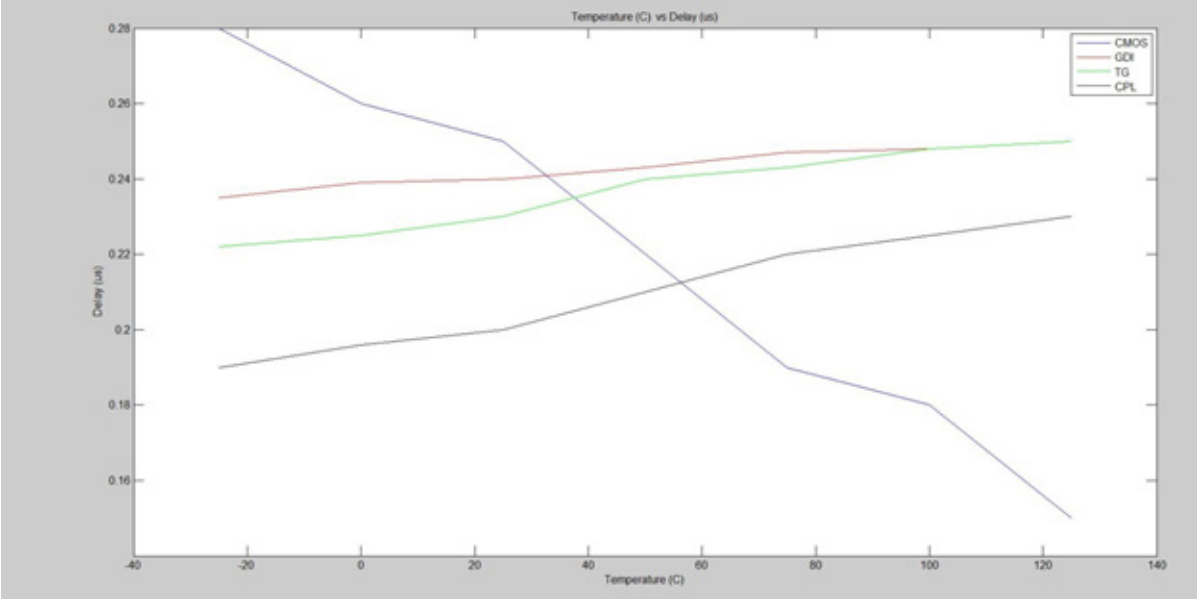

Figure 29. Delay of 8-bit FinFET adder.

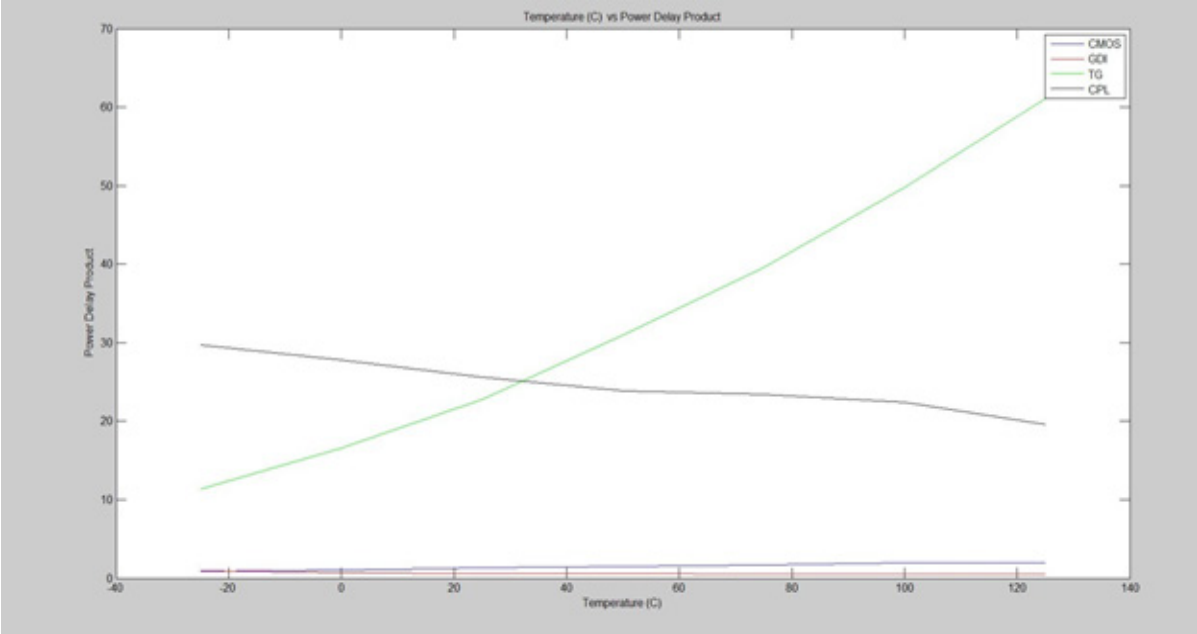

Figure 30. Power delay Product of 8-bit FinFET adder.

with range of temperature values, is graphically represented in Figure 21. The delay of 8-bit MOSFET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 22. The power delay product of 8-bit MOSFET adder (for all logic

styles) is correlated with range of temperature values, is graphically represented in Figure 23.

The dynamic power of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 24. The static power (inputs at low logic level) of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 25. The leakage power (inputs at low logic level) of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 26. The static power (inputs at high logic level) of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 27. The leakage power (inputs at high logic level) of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 28. The delay of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 29. The power delay product of 8-bit Fin FET adder (for all logic styles) is correlated with range of temperature values, is graphically represented in Figure 30.

Figure 17 and 24 we can infer that the maximum dynamic power dissipated by an 8-bit MOSFET adder is 0.882mW and that of an 8-bit Fin FET adder is 0.156μW. From Figure 18 and 25 we can infer that the maximum static power (inputs at low logic level) dissipated by an 8-bit MOSFET adder is 1.68mW and that of an 8-bit Fin FET adder is 0.305μW. From Figure 19 and 26 we can infer that the maximum leakage power (inputs at low logic level) dissipated by an 8-bit MOSFET adder is 0.139mW and that of an 8-bit Fin FET adder is 0.227μW. From Figure 20 and 27 we can infer that the maximum static power (inputs at high logic level) dissipated by an 8-bit MOSFET adder is 0.945mW and that of an 8-bit Fin FET adder is 0.17μW. From Figure 21 and 28 we can infer that the maximum leakage power (inputs at high logic level) dissipated by an 8-bit MOSFET adder is 0.134mW and that of an 8-bit Fin FET adder is 0.024μW. From Figure 22 and 29 we can infer that the maximum propagation delay value of an 8-bit MOSFET adder is 0.46μs and that of an 8-bit Fin FET adder is 0.28μs. From Figure 23 and 30 we can infer that the maximum power delay product of an 8-bit MOSFET adder is 0.405pJ and that of an 8-bit Fin FET adder is 0.029pJ.

3. Conclusion

FINFET not only has exceptional performance over MOSFET but is prepped to take over MOSFET as the superior technology below 90nm. The modeling and optimization of the adder, was done at 32nm technology. The FINFET structure has been investigated with the aim of reducing the leakage power and propagation delay. The FINFET adder gave rise to a reduction in the leakage power dissipation by 99.9% in addition to a reduced propagation delay by 39% and power delay product by 29%. It is also evident that the adder implemented in GDI logic style consumes less power than other adder structures.

4. References

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