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DC-DC Step-Down Converter with Wide Switching Range and Low Ripple Voltage for Wireless Sensor Node Applications

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Abstract

Objectives: This paper presents a switched capacitor based dc to dc step down converter architecture to produce multiple output voltages with low ripple factor for the applications in wireless sensor nodes. The use of energy efficient non overlapping clock generators to minimize short circuit current has been presented. **Methods:** The proposed architecture consists of the integration of a capacitive ladder based dc to dc step-down converter with a non overlapping clock produced by a Constant Energy Ring Oscillator (CERO) instead of Current Starved Ring Oscillator (CSRO). The converter produces multiple output voltages as per the requirement of the oscillator. The switched capacitor consists of MOS Transmission gates as switches and the capacitors. All the simulations were performed in the 90nm technology by the Cadence Virtuoso simulator. All the switches in the DC-DC converter were implemented as transmission gates. **Findings**: A very low ripple voltage output was produced by the DC-DC converter. Its efficiency was found to be greater than 90% with a switching frequency of 500 MHz. Compared with the previous topologies, the number of transistors used was highly reduced. **Improvements:** A wide range of output voltage from 0.8V to 2.7 V was generated. The ripple voltages were as low as 0.02V at full load conditions.

Keywords: DC-DC, Ring Oscillator, Ripple Voltage, Switched Capacitor, Wireless Sensor Nodes (WSN)

1. Introduction

In today's wireless industry, with the advent of Internet of Things the use of wireless sensor nodes (WSN) are becoming extremely important. The WSNs may be placed in remote locations or inside human or animal bodies for the purpose of surveillance, gathering sensory information and communicating with other connected nodes in the network. So it is of utmost importance that the WSN should require minimal or no maintenance and should be highly energy efficient. To realize this energy autonomy, energy harvesters come into play. For this purpose the WSNs are designed in such a way that they can adaptively optimize themselves according to the varying load conditions, harvested energy and battery voltage using various adaptive techniques. One such adaptive technique involves changing the operation speed of the WSN by modulating the frequency of the oscillator present in the WSN according to the harvested energy.

The architecture[1] of an adaptive technique for energy harvesting system based on switched capacitors is shown in Figure 1. It consists of a high voltage lithium battery which provides power to the various components of the WSN after chopping it down to a suitable voltage which is required for its efficient operation (e.g. 0.6V for microprocessor and 0.45V for SRAM). The energy efficiency of the WSN largely depends upon the switching losses due to the parasitic capacitance and drive power switches. This switching loss varies according to CV_{DD}[2,3].

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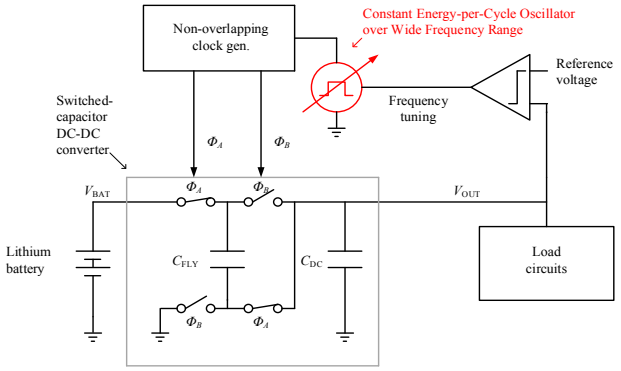

Figure 1. Architecture of switched capacitor DC-DC converter in WSN.

So an ideal oscillator in WSN must cover a wide frequency range. Also the power consumed by it should be proportional to the frequency so that the oscillator does not dominate the overall power at slow speeds and low load conditions[1]. In context of the frequency range requirement, a ring oscillator can be considered a good candidate due to its wide tuning range, compact design and small silicon area. But however the requirement of proportionality between power consumed and frequency cannot be fulfilled by a simple ring oscillator.

2. CERO and CSRO

A ring oscillator can be designed and implemented in a number of ways. Two such ways are: Current Starved Ring Oscillator (CSRO), Constant Energy-per-cycle Ring Oscillator (CERO)

CSRO: The CSRO is the conventional form of ring oscillator which consists of a delay generator circuit and a current starving circuit. Its works by controlling the amount of current required to charge or discharge the capacitive load of each stage. To get sustained oscillations the circuit must provide a phase shift of 360 degrees and must have unity voltage gain at around oscillation frequency[4]. This is accomplished by modulating the control voltage with the turn on resistance of the pull down transistor and pull up transistors through a current mirror. This variable resistance allows controlling the current required to pull-up or pull-down the load capacitance. A large control voltage allows a large current to flow, producing a small resistance and hence gives less delay. Similarly if the control voltage is decreased, the corresponding delay increases. The topology of CSRO is shown in Figure 2.

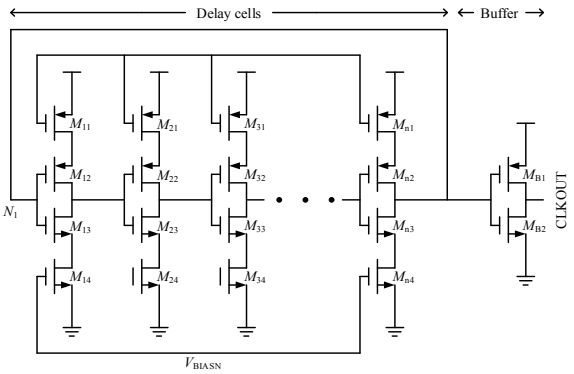

Figure 2. Topology of CSRO.

CERO: Unlike the conventional CSRO, the CERO has a constant energy per cycle over a high frequency range. So it can be said to be more efficient than the CSRO. It charges or discharges the capacitance using the sub-threshold current of MOS transistor without short circuit current. It consists of a current feeding scheme with gate voltage control to control the output frequency efficiently. Since it works below the threshold voltage i.e., between V_{thn} (NMOS threshold voltage) and (V_{dd}-|V_{thp} |) (PMOS threshold voltage), the power consumption becomes proportional to the frequency by avoiding the short circuit current. The topology of CERO and the block diagram of a 3 stage CERO delay cell are shown in Figure 3 and 4 respectively.

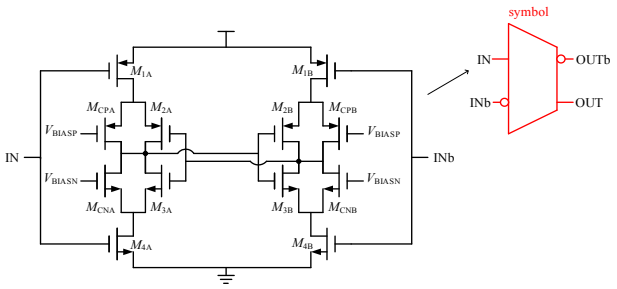

Figure 3. Topology of CERO.

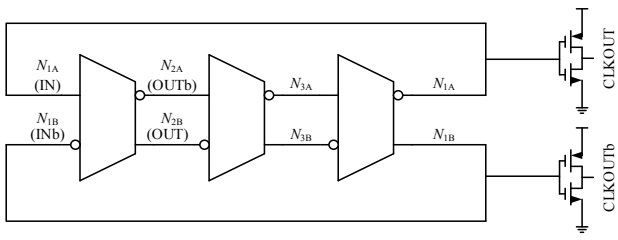

Figure 4. A 3 stage CERO delay cell.

One of the major differences between a CSRO and CERO is that they modulate their output frequencies in opposite manner. A CSRO changes its output frequency by limiting the current, whereas the CERO injects more current to change the frequency. For higher clock frequencies the charging or discharging current is increased via the current controlled transistor.

3. Topology of DC to DC converter

The topology implemented for DC to DC converter[5] is shown in Figure 5. The advantage of this topology is that it can supply three different voltage levels to the WSN according to its demand. Unlike other converters where different topologies are used to provide different output voltages, it can supply the changing voltage demand by just changing the tapping of the output voltage node. There are three output voltage nodes namely $V_{OUT\ 1}$, V_{OUT2} and V_{OUT3} as shown in Figure 2. The output voltage of $V_{OUT\ 1}$, V_{OUT2} and V_{OUT3} are 0.8V, 1.8 V and 2.7V respectively at full load condition and 1 V, 2V, 2.8V at no load condition. We apply the input voltage of 3.8V from a lithium ion battery. The efficiency of the DC to DC step-down converter is estimated by $\eta=(1-\delta V/VNL)$, where δV is the ripple voltage and VNL is the voltage at no load. Hence we see that as the ripple voltage increases the efficiency decreases and vice versa.

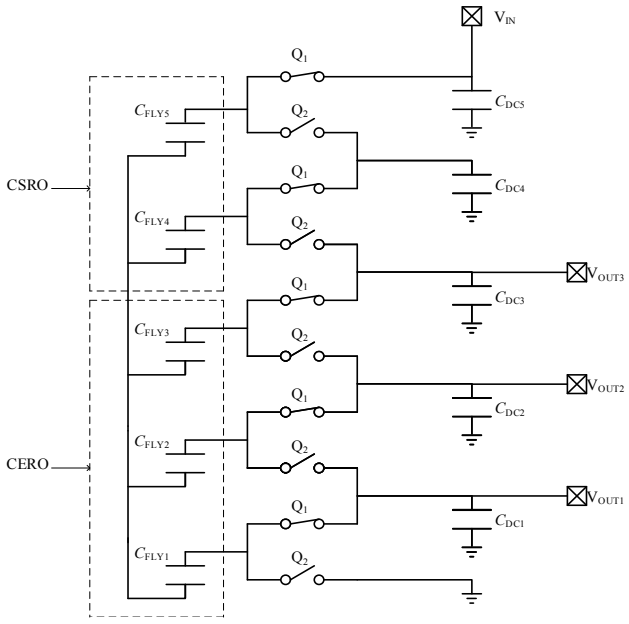

Figure 5. Topology of DC-DC converter.

4. Integration of DC to DC Converter with CERO

Architecture is proposed where the DC to DC converter is integrated with the CERO[6]. The output frequency of the CERO is 500 MHz, which is fed to the DC to DC converter. In this DC to DC converter topology, different voltages are supplied by the same circuit by just changing the tapping of the output voltage. To detect the required load current, input and output nodes are shorted. Thus the tap changing is a very crucial task which is performed by a combinational control circuit.

The control circuit consists of blocks like multiplexers whose select lines are the outputs of comparators are used to weigh the output with reference voltage. The architecture[7] is shown in Figure 6.

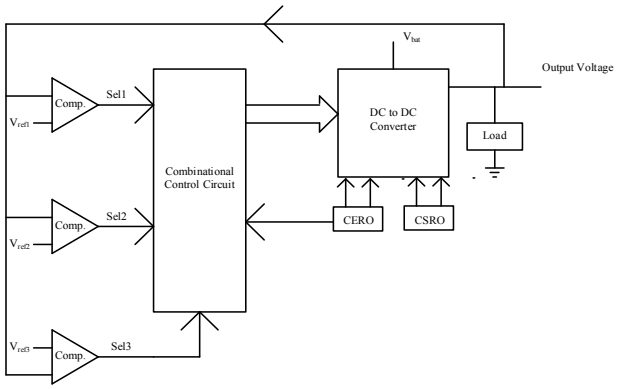

Figure 6. Integration of DC-DC converter with CERO.

5. Simulation Results and Comparison with Previous Work

The proposed DC to DC converter produces an output of very low ripple voltage. This increases the efficiency of the converter to a great extent. The circuit is implemented in 90nm technology. At full load condition the value of the load capacitance is taken as 100pf. The value of the entire C_{fly} is taken as 1pf. The input voltage used for

the DC to DC converter is 3.8V. Figure 7, 8, 9 shows the output waveform of the CERO, CSRO, and the DC to DC converter. The maximum efficiency of the converter is found to be 98%. The efficiency calculation is done without considering the losses. A comparison of the integrated topology with the previous work[2] is shown in Table 1.

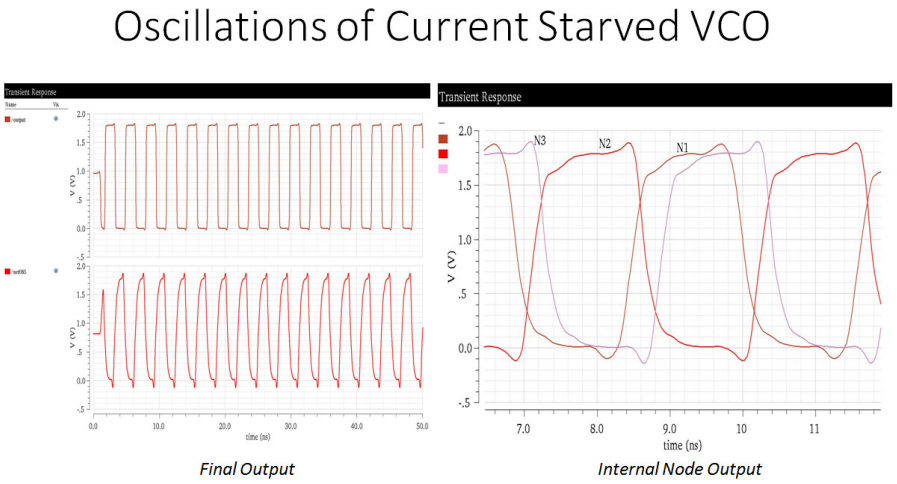

Figure 7. Waveform of CSRO.

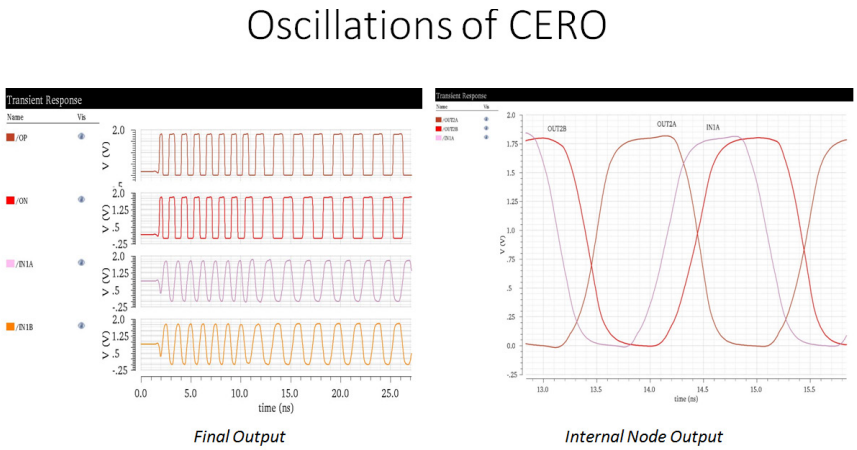

Figure 8. Waveform of CERO.

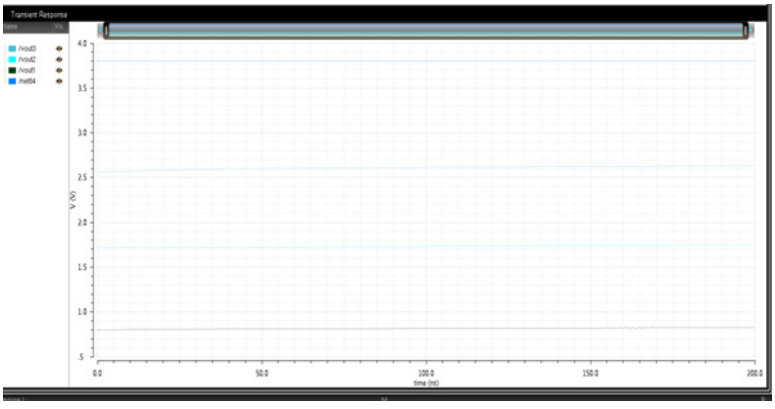

Figure 9. Output Waveform ofDC-DC converter.

Table 1. Comparison of presented work with previous work

Parameter	Proposed topology	Previous work
Technology	90nm	90nm
Input Voltage (V)	3.8	1.2
Conversion Ratio	1/4 1/2 3/4	1/2 2/3 5/6
Output Voltage (V) at No Load	1 2 2.8	0.59 0.76 0.87
Ripple voltage (V)	0.028 0.030 0.071	0.093 0.080 0.135
Efficiency η (%)	97.17 98.48 97.41	84 89 84
switching Frequency (MHz)	500	364
Total Number of transistors used	40	60

6. Conclusion

The paper presents a topology for a switched capacitor based DC- DC converter. The ripple voltage and efficiency is higher than its predecessor. The comparisons between all their parameters are shown in table. Also the number of transistors used in this topology is much less than the previous architecture which uses three different topologies to provide voltage of different levels. The presented DC to DC converter topology was able to achieve more than 90% efficiency over a wide range of output voltage from 0.8V to 2.7V.

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