Indian Journal of Science and Technology, *Vol 11(17), DOI: 10.17485/ijst/2018/v11i17/122769, May 2018*
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Design and Implementation of FIR Filter Architecture using High Level Transformation Techniques

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Abstract

Objectives: FIR filter structure is designed with area and delay optimization is designed using Systolic Architecture and Associativity High Level Transformation technique in this paper. Finite Impulse Response (FIR) filter structure with optimized parameters is one of the major challenges in VLSI Signal Processing. **Methods/Statistical Analysis:** The designed FIR filter is designed using Modelsim for functionality verification and the structure is implemented in Spartan 3E FPGA kit using Xilinx ISE simulator for the analysis of the designed architecture. **Findings:** The FIR filter is designed with 4-Tap, 8-Tap and 16-Tap length and the designed architecture using Systolic architecture with Associativity technique shows 8.9%, 2.3% and 2.4% reduction in LUT for 4-Tap,8-Tap and 16-Tap filter respectively and 14.22%,11.89% and 12.32% reduction in delay for 4-Tap,8-Tap and 16-Tap filter respectively. **Application/Improvements:** Further Associativity techniques may be used for future work.

Keywords: Architecture, FIR Filter, High Level Transformation

1. Introduction

The importance of reducing area and delay parameters is increasing as range of sophistication of applications in Very Large Scale Integration (VLSI). The three important parameters to be considered for any VLSI architecture designs are Area, Power and Delay. So in that way many techniques has been incorporated for the reduction of power which can be done by reducing the number of functional units in the architecture and to increase the speed of the system by reducing the critical path of the circuit through various methods[1].

The FIR filter is considered here where a High level transformation technique has been incorporated for the reduction of area and to improve the speed of the system. The transformation techniques considered here is Systolic Architecture method along with Associativity transformation. The designed FIR filter can be used in many VLSI applications such as Adaptive Noise Cancellation and System Identification techniques applications.

2. Finite Impulse Response (FIR) Filter

The filter in which impulse response is of finite duration is defined as Finite Impulse Response. FIR filters can be designed with different methods. The objective of FIR filter is to produce ideal results[2,3]. The transfer function of FIR filter is when the order of the filter increases the complexity and amount needed for processing the input is also increased.

The function of an FIR filter is to accept the input signal and blocking specific frequency and passing the real signal minus those components to the output side. Where FIR is a digital filter the filter operates on the digital input and provides the digital output.

2.1 FIR Filter Design

The FIR filter are generally designed using basic building blocks such as multiplier, adders and the series number of

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delays. Figure 1 shows the general FIR filter of length N. The delays considered in the filter operate on the input-data. The Coefficient value added to the filter is used for multiplication[4,5].

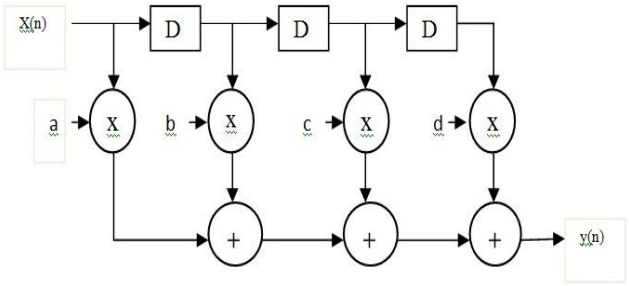

Figure 1. Conventional four tap FIR filter.

Figure 1 shows the general FIR filter structure of length N, where x(n) represents your input sample and D represents the delay samples and a,b,c,…. represents the filter coefficients which is to be multiplied with input sample. The order can be of any type according to the signal processing applications. Where if an N tap fir filter is designed it consists of (N-1) delay elements and N filter coefficients and (N-1) adder blocks. In this paper 4 tap conventional FIR filter is designed and simulated for functionality verification and implemented in Spartan-3 to determine area and delay parameters of the filter[6–8].

The critical path of the above FIR filter is given below,

$$T_{c1} = T_{mult} + 3T_{add}$$

Where,

T_{c1} represents the critical path of 4-tap FIR filter

T_{mult} represents the delay of multiplier

T_{add} represents the delay of adder

2.2 FIR Filter Design using Systolic Architecture

The proposed architecture is the Fir filter design using Systolic architecture with associativity technique[9]. Here systolic architecture includes a number of Processing Elements (PE) that computes and transfers the data. It is also called as Systolic array and it regularly pump the data in and out in the network[10].

The critical path of Systolic 4-tap FIR filter is given below,

$$T_{c2} = T_{mult} + T_{add}$$

Where,

T_{c2} represents the critical path filter
T_{mult}represents the delay of multiplier
T_{add} represents the delay of adder

So it is clear that the critical path of Systolic FIR filter is greatly reduced to ($T_{mult} + T_{add}$), compared to the normal FIR filter. Thereby, improvement in speed of the filter can be achieved. The 4-tap filter is designed using systolic architecture and simulated for functionality verification and implemented in Sparatan-3 to calculate the area and delay parameters.

2.3 FIR Filter Design using Associativity

The proposed architecture includes the FIR filter architecture designed using Systolic Architecture along with Associativity. While designing the Filter structure with systolic architecture technique the area and register utilization is increased when the architecture is implemented, so in order to minimize the utilization of registers the associativity technique is included where it reduces the height reduction of the architecture which in terms reduces the area and delay of the circuit by reducing the critical path of the circuit in terms of adder and multiplier blocks.

The critical path of the above FIR filter is given below,

$$T_{c1} = T_{mult} + 2T_{add}$$

Where,

T_{c1} represents the critical path of 4-tap FIR filter
T_{mult} represents the delay of multiplier
T_{add} represents the delay of adder

Figure 2 shows the fir filter design using associativity transformation where in the associativity technique the critical path Tm + (N-1)Ta is reduced to, Tm+ (log 2 N) T a.

2.4 Proposed Architecture

In the proposed architecture the FIR filter is designed using Systolic Architecture with Associativity transformation. Where the systolic architecture is designed to reduce the critical path which increases the LUT so in order to reduce the area the associativity technique is included.

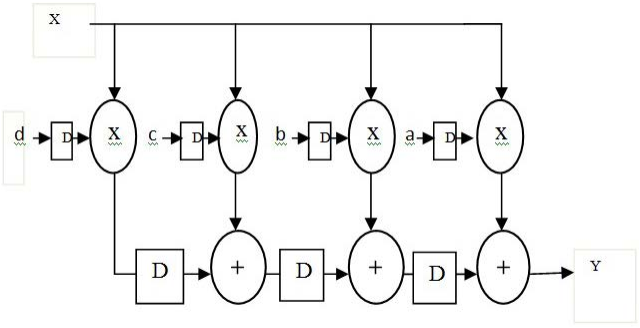

Figure 2. Systolic architecture for Four tap FIR filter.

3. Results and Discussion

The HDL coding for the FIR filter is designed and simulated in Modelsim to check the functionality of the conventional and proposed architecture and the circuit is implemented in the SPARTAN-3E FPGA kit using XILINX to check the architectural parameters of the conventional and proposed architecture. Figure 3 shows the Modelsim output of Conventional FIR filter designed using Verilog programming where the input is of hexadecimal value of 4 and the filter coefficients of 0,0,1 and the obtained output is hexadecimal value of 4.

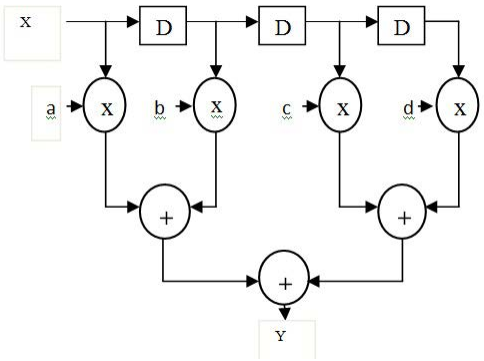

Figure 3. Associativity for four tap FIR filter.

In Figure 4 the FIR filter is designed using Systolic Architecture with Associativity transformation technique. The main advantage and significance of this proposed architecture is it produces the optimization of area and Speed parameters.

The critical path of the proposed architecture is given by Tmult + Tadd. Figure 5, 6 shows the Modelsim output of Proposed FIR filter designed using Verilog programming where the input is of hexadecimal value of 4 and the filter coefficients of 0,0,1 and 0 and the obtained

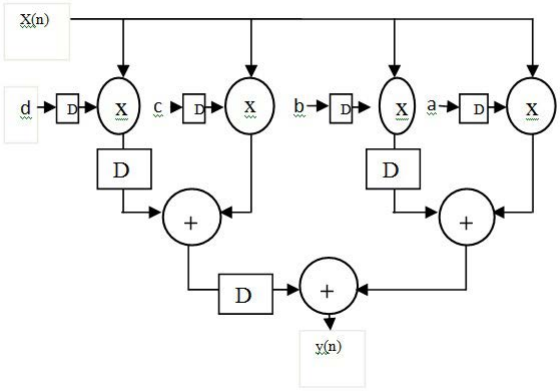

Figure 4. Proposed architecture (Systolic Architecture + Associativity) for 4 tap FIR filter.

output is hexadecimal value of 4 where it defines the similar functionality between the conventional and proposed architecture. The designed FIR filter using Systolic Architecture and Associativity reduces the LUT and Delay of the circuits. Initially when 4 tap FIR filter was designed the number of LUT obtained is 79 and the delay taken by the circuit is 24.203ns and when systolic architecture is introduced in the circuit the LUT and Delay parameters obtained is 85 and 22.100ns respectively. Where in the systolic architecture the delay reduces but increases because of the inclusion of delay elements and when associativity is incorporated the area and delay reduces so along with systolic architecture techniques the associativity technique is implemented to design efficient VLSI architecture of the filter.

The area and delay parameters in the circuit when associativity includes the reduction in area but when both systolic architecture and associativity is incorporated area and delay optimization is improved when comparing to the other techniques.

Table 1 shows that the FIR filter designed using systolic architecture shows 8.6%, 6.6% and 4.9% reduction in delay for 4-Tap, 8-Tap and 16-Tap filter respectively and when associativity technique is implemented the architecture shows 8.86%, 3.16% and 2.39% reduction in number of LUT for 4-Tap, 8-Tap and 16-Tap filter respectively and the proposed architecture (Systolic Architecture and Associativity) shows. 9%, 2.3% and 2.4% reduction in LUT for 4-Tap, 8-Tap and 16-Tap filter respectively and 14.22%, 11.89% and 12.32% reduction in delay for 4-Tap, 8-Tap and 16-Tap filter respectively.

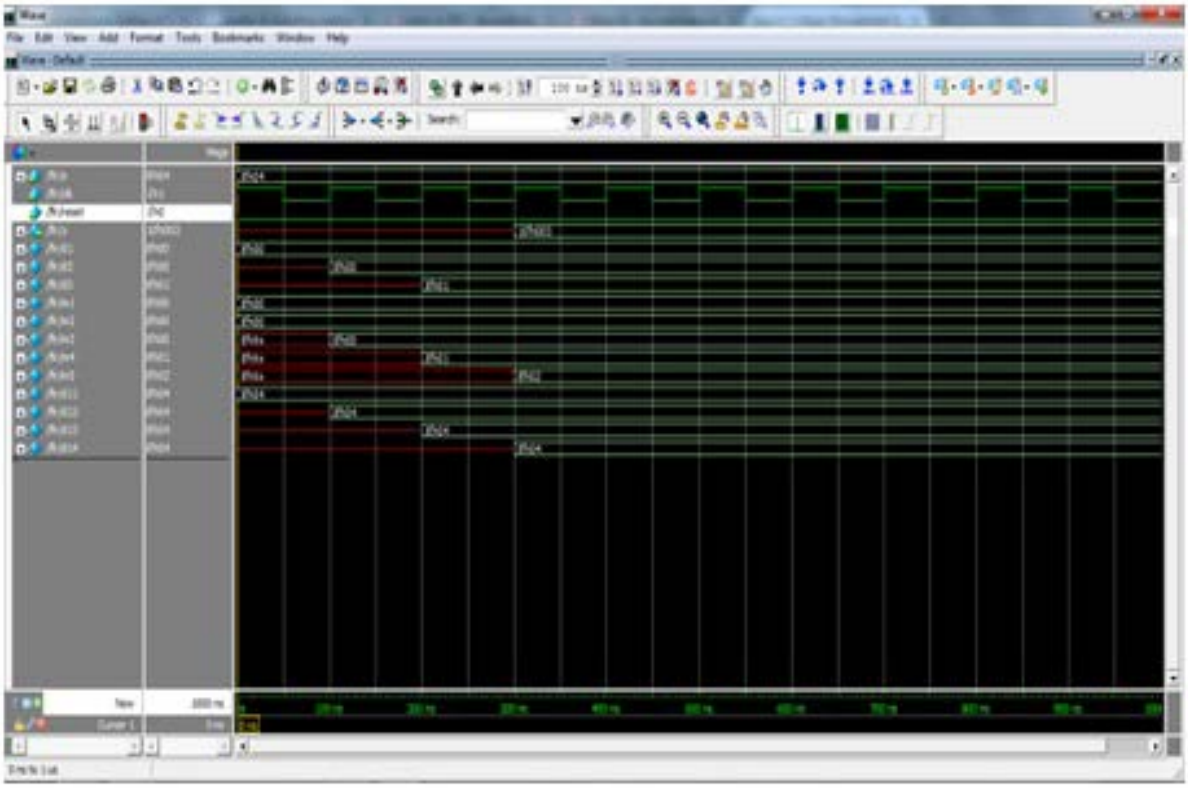

Figure 5. Model sim output for conventional FIR filter.

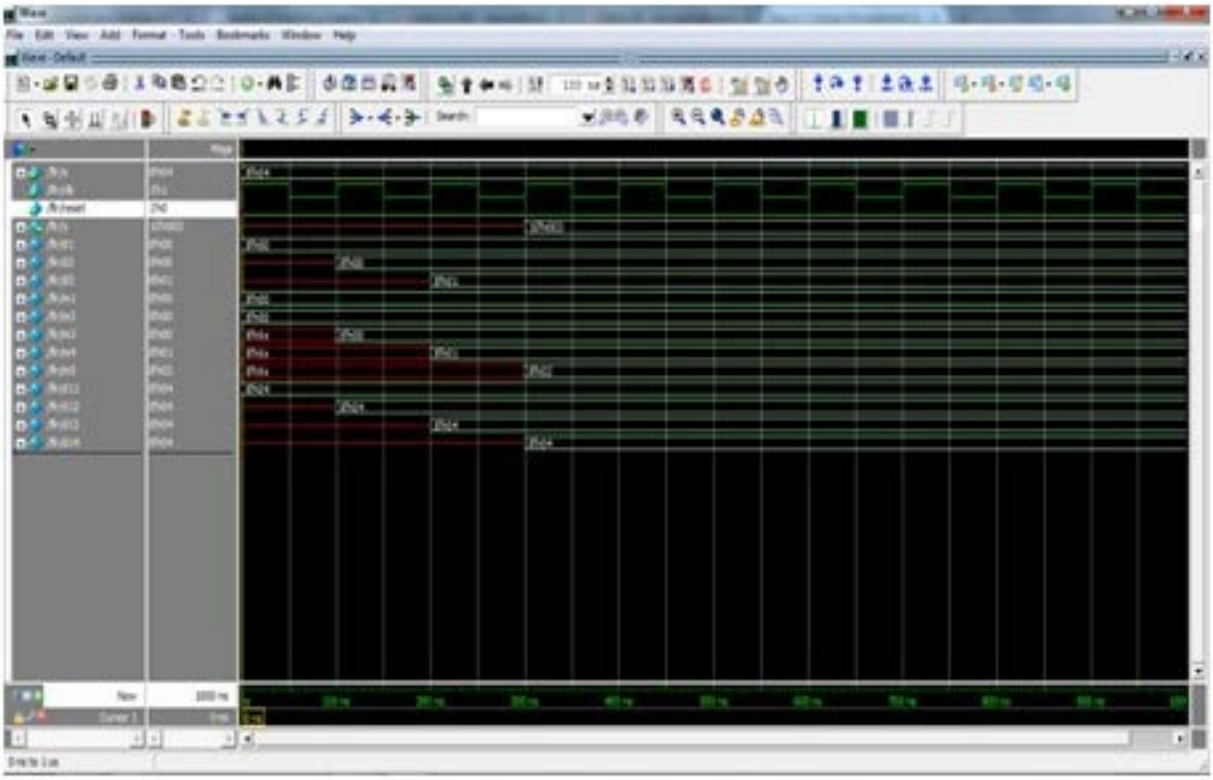

Figure 6. Model sim output for proposed FIR filter.

Table 1. Area and delay comparison between conventional and proposed FIR filter architecture

TRANSFORMATION TECHNIQUES	4-TAP FILTER		8-TAP FILTER		16-TAP FILTER	
	LUT	Delay	LUT	Delay	LUT	Delay
Conventional	79	24.203ns	253	30.330ns	585	35.747ns
Systolic Architecture	85	22.100ns	267	28.319ns	591	33.981ns
Associativity	72	24.203ns	245	30.330ns	571	34.125ns
Systolic Architecture + Associativity (Proposed)	74	20.76ns	247	26.723ns	579	31.341ns

4. Conclusion

The efficient FIR filter structure is obtained using Systolic architecture technique and Associativity technique. The proposed architecture shows 8.9%, 2.3% and 2.4% reduction in LUT for 4-Tap, 8-Tap and 16-Tap filter respectively and 14.22%, 11.89% and 12.32% reduction in delay for 4-Tap, 8-Tap and 16-Tap filter respectively comparing to the conventional structure when implemented in the Sparatn-3 FPAGA kit. The designed architecture can be implemented for VLSI signal processing in Adaptive filter architecture for Noise cancellation technique in future work.

5. References

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