Indian Journal of Science and Technology, *Vol 10(3), DOI: 10.17485/ijst/2017/v10i3/110626 January 2017* *ISSN (Print) : 0974-6846*
ISSN (Online) : 0974-5645

Subthreshold FinFET SRAM at 20nm Technology with Improved Stability and Lower Leakage Power

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Abstract

Background/Objectives: The Complementary Metal–Oxide–Semiconductor (CMOS) scaling feature was the wonderful feature which led the electronics market into in an era of miniaturization but with the fascinating feature some limitations has also been observed. **Methods/Statistical analysis:** CMOS technology has also given a new horizon to the memory circuits like Static Random-Access Memory (SRAMs). To overcome the limitations of scaling of the CMOS technology, Fin Field Effect Transistor (FinFET) technology has been chosen. To overcome the limitations of scaling of the CMOS technology, FinFET technology has been chosen. Like CMOS SRAMs, FinFET SRAMs have also gained popularity because of the advantages as discussed in this paper. **Findings:** In this paper, FinFET SRAM cells have been proposed in three different configurations for better stability and reduced leakage power in sub threshold region at 20nm technology.4 different modes of FinFET has been used to implement the SRAM. The FinFETs are classified as (i) SG-mode (ii) LP-mode and (iii) IG mode. A comprehensive analysis has been made for all the 4 types of SRAM stability which includes for Read Margin, Write Margin, Hold Margin and leakage power analysis by finding the leakage current for all the proposed circuits and has compared with the previous work and it has been found that the proposed circuits serves better in terms of stability and reduced leakage current. The cell has been implemented for sub threshold voltages ranging from 0.4V to 0.1V. The maximum Write Margin at 0.4V is 196.9mV, Read Margin is 110 mV. **Application/Improvements:** It has been found that from the different SRAM circuits, IG-P has the maximum Write SNM, Read SNM and hold margin while LP mode has minimum leakage current, next the IG-P mode FinFET.

Keywords: FinFET, Leakage Current, Read Margin, SRAM, Write Margin

1. Introduction

The unexpected growth of the handheld devices especially the cellular phone can be visualized by the fact that there were as many cellular phones as the World's population in 2014 according to the United Nation's International Telecommunication Union. The reason behind this explosive growth is the devices which are handheld, small in size, efficient and cost effective. The credit should be given to the CMOS technology who has given high performance, low cost, small size integrated devices. Scaling is the feature which has given the all advancement in CMOS technology. It has been already stated by ITRS that 90% area of the processors chip is occupied by the SRAM.

In all the high speed processors, high performance digital circuits, bio-medical instruments, biomedical implants all requires efficient SRAM having low power, high speed and smallest as much as possible. It becomes a challenge to design an efficient low power with adequate stability and miniature size. CMOS Scaling technology helps a lot in designing the efficient SRAMs but, scaling down beyond 32nm, so many limitations found in CMOS like increased leakage currents i.e. sub threshold currents, gate dielectric leakage currents device becomes more sensitive to short channel effects& threshold voltage variations.

In order to overcome these SCE's multi-gate devices have been emerged as promising candidate. FinFET is the multi-gate device which is more feasible as, it has

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similarity in its fabrication process with planar CMOS technology. It reduces the leakage current and SCEs because of better gate control over the channel. "Scaling" one of the most exciting features also exhibits in FinFET.

Figure 1 shows the 3D pictorial view of FINFET. The thin body device is fabricated with the usual patterning and etching technologies and shaped like fish FIN. Silicon-on-Insulator (SOI) or lower-cost bulk substrates are used so that FIN can be made over them. FinFET has quasi – planar structure as the FIN is shorter than the thickness of the gate[1]. FinFET fabrication process is in very much the same way as for processing of a planar MOSFET because the fin is shorter than the gate thickness, so the structure is quasi-planar. The FinFET occupies less silicon area than a planar MOSFET because the channel width (W) of a FinFET is the peripheral length of the fin that includes all sides of the fin cross-section, and W can be significantly larger than the fin pitch.

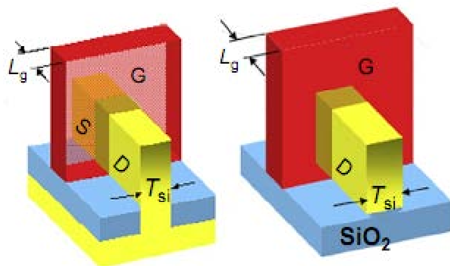

Figure 1. FinFET 3D structure[1].

FinFET channel is lightly doped gives rise to lower transverse electric field and negligible impurity scattering in the on state, FinFET devices have almost negligible depletion charge and junction capacitance which can be easily laminated and results in lower parasitic capacitances which lowers the capacitive load of bit line and threshold variations are also minimum. FinFET SRAM design proposed for low power application in[2]. All the above mentioned properties make FinFET a right choice for SRAMs and it shows better performance over CMOS SRAMs.

Various FinFET SRAMs were been proposed for better performance, stability and reduced leakage. In[3] 6T FinFET SRAM has been proposed for leakage reduction and enhanced speed, in[4] author proposed FinFET SRAM using dynamic gate voltage adjustment.8T FinFET SRAM has been proposed for enhanced read and write margin in[5]. In[6] 6T FinFET SRAM has been discussed with pass gate feedback. In[7] FinFET SRAM cell has been proposed for P type access transistor to increase robustness. In[8] 9T SRAM has been proposed for improved leakage power and access time. Schmitt trigger based FINFET SRAM been proposed in[9].

In this paper,10T FinFET SRAM have been proposed using three different modes of FinFET configiuration for subthreshold region of operation and are simulated and analysed at 20nm PTM FinFET technology and measured the stability factors for read, write and hold mode of SRAM also,leakage current of each confguration has been calculated anda comparison has been made which is best in terms of stability and reduced leakage power consumption.In section 2 10T FinFET circuits has been discussed, Section 3 discusses the proposed work and Simulation results analysed in section 4 .Section 5 inclused the conclusion

2. Schmitt Trigger based FinFET SRAM Cell

In[10] 10T CMOS SRAM has ben proposed for stable operation of cell at low supply voltages.This 10T SRAM was a schmitt trigger based differential bitcell having feedback.The SG mode FinFET SRAM Cell has already been proposed in[9]. It was simulated at 32nm technology but the SNM for the cell was 12mV at 0.4V.In this paper,SG mode SRAM cell is designed and simulated in subthreshold region from 0.1 V to 0.4 V at 20nm FinFET technology and found better stability than the previous work.The 10T shorted gate FinFET is designed and simulated at 20nm technology in this paper as shown in Figure 2.

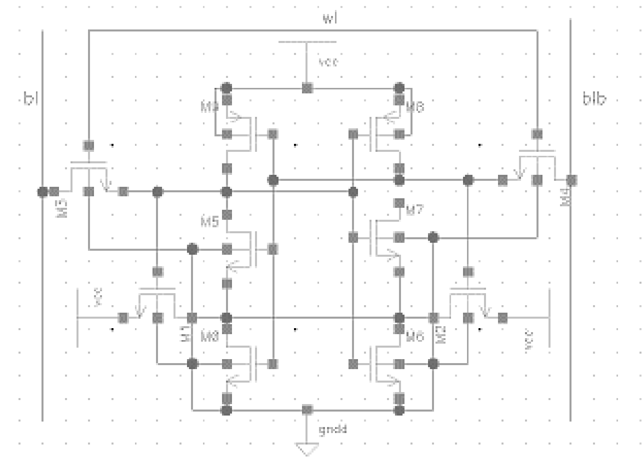

Figure 2. SG mode FinFET SRAM.

3. Proposed FinFET SRAM Cell

In this work, we have propsed Low Power Mode and Independent Gate mode FINFET .We have designed and simulated & compared the 4 different SRAM cell circuits on the basis of the the leakage current and Stability of the cell in subthreshold region.

The FinFETs are classified as (i) SG-mode (ii) LP-mode and (iii) IG mode. In Short Gated mode i.e. SG-mode the two gates are connected together so, they can be a replacement for bulk CMOS devices.In LP-mode which is Low Power mode the back gate bias is tied to a reverse bias volatge to reduce the subthreshold leakage current[4]. Independent gate the two gates can be controlled separately, independent signal drives the two gates[11].

3.1 LP Mode FINFET SRAM

In Figure 3, LP power mode FinFET SRAM has been proposed. In this mode all the transistors are Independent gate FinFET i.e. the front and back gate of the transistors are biased at different voltages. Here, the back gate is tied to bias a voltage which is useful in reducing the leakage current. In this circuit, the back gate of the PMOS transistors are tied to supply voltage and back gate of all the NMOS connected to ground.

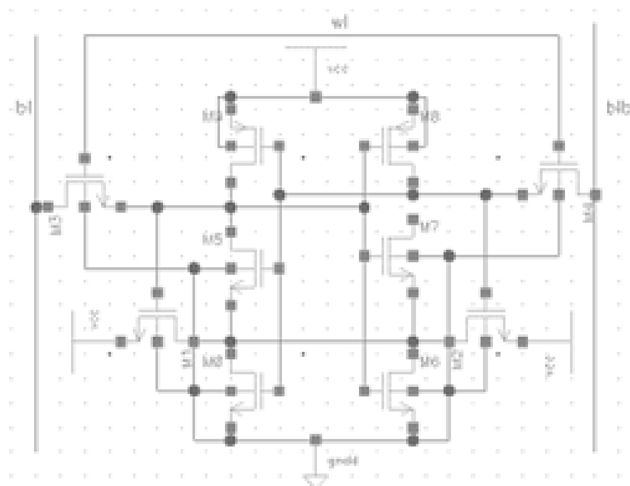

Figure 3. LP mode FinFET SRAM.

In this circuit, the conventional 6T SRAM two inverters and pass transistors been used. Schmitt trigger inverters uses three transistors in place of two transistors as in conventional inverters here in this circuit, M2-M6-M7-M8 forms one Schmitt trigger inverter and the other inverter formed by M0,M1,M5,M9.M3 and M4 are the access transistors. The positive feedback from M1 and M2 adaptively changes the inverter's switching threshold depending on the input direction. During a read operation the voltage of the output node increases because of the voltage divider between the pull down and the access transistor and if this voltage is more than the switching voltage of the other inverter it will results into read failure so to avoid this the feedback mechanism should increase the switching voltage of the inverters. M1 & M0 or M2 and M6 raises the voltage of their common node which increases the switching voltage of the inverter and this preserves the Schmitt trigger action and because of the differential operation it gives better noise immunity[7]. The SG mode works similar to bulk CMOS technology.

3.2 Independent Gate-N (IG-N) Mode SRAM

Figure 4, shows the FinFET SRAM using Independent Gate- N Mode which is mixed mode, In this case the back gate and front gate of NMOS are connected with different biased voltages similar to Independent gate mode while the back and the front gate of the Prosier shorted together as in SG mode. The working of the Cell is similar as discussed in section 3.1.

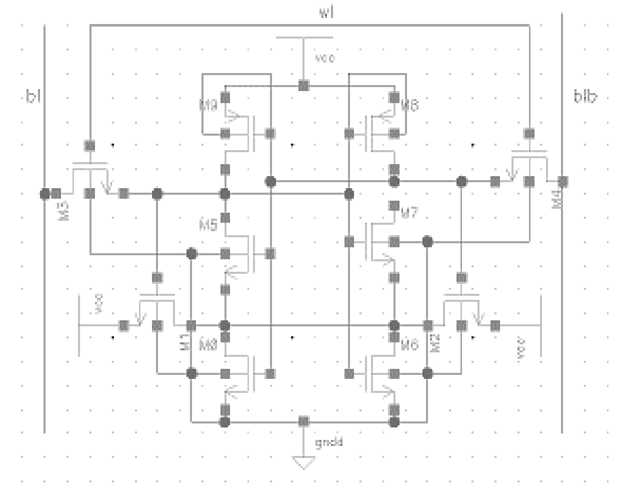

Figure 4. IG-N mode FinFET SRAM cell.

3.3 Independent Gate-P (IG-P) Mode SRAM

FinFET SRAM using Independent Gate -P Mode is a combination of independent gate mode and shorted gate mode shown in Figure 5. The working of the cell is same like 10T Schmitt trigger based SRAM except the biasing

voltages of the gates are different .In this mode, front and back gates of the PMOS transistors are independently controlled and all the NMOS are connected in SG mode i.e., back and front gate of the NMOS are tied together. It is used in low power applications.

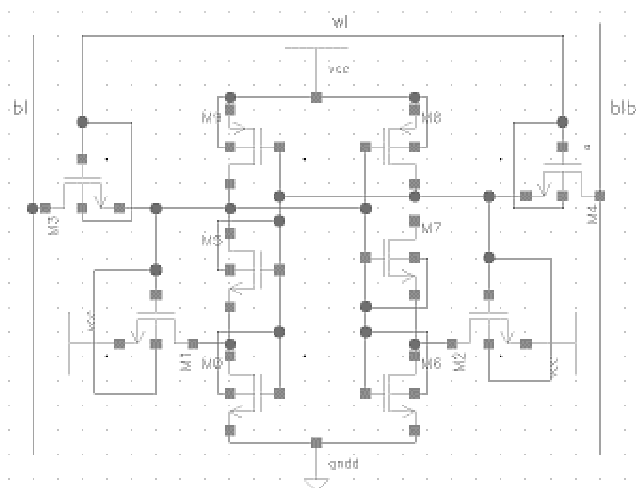

Figure 5. IG-P mode FinFET SRAM cell.

4. Simulation Results

In this paper all the four type of 10T FinFET SRAM have been simulated using 20nm FinFET PTM technology. Stability and leakage current have been focused in this paper in sub threshold region. Write Static Noise Margin (WSNM), Read Static Noise Margin (RSNM), Hold Margin and leakage current been discussed in the following sections.

4.1 SRAM Stability

SRAM stability is determined by SNM, which is the maximum amount of noise voltage which is introduced at the output of two inverters, to retain its data. The graph obtained from VTC curve & inverse VTC curve of the inverters is used to determine the SNM and is called butterfly curve.

The graphical representation of the SNM is as shown in the Figure 6. As, shown in the figure, four squares are fitted between the voltage transfer characteristic curves which are the largest possible squares that can be fit between the two inverter characteristic curves of the SRAM cell. The two squares are for read stability and two for hold stability also known as Read and Hold Margin respectively[12].

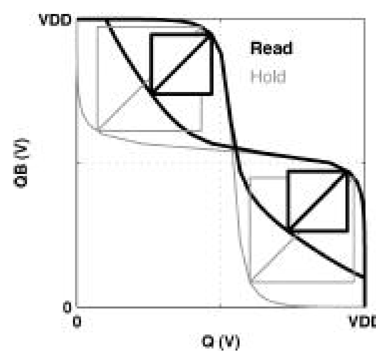

Figure 6. Butterfly curve of SRAM.

4.1.1 Write Stability

Write Margin is defined as the potential difference between the bit line level at which the data is flipped and the end point. Write stability can be finding using butterfly curve. Write Margin is measured using butterfly curve or VTC curves. The write noise margin for logic “1” is the width of the smallest square which can be embedded in the upper right half of the curve. Similarly, for writing “0” WSNM can be found. The final WSNM for the cell is the minimum voltage among the WSNM of writing “0” and writing “1”[13]. WSNM has been calculated in Sub-threshold operation. Table I gives the comparison of the various modes of FinFET SRAM cells. The effect of the voltages can be easily seen in the Table 1. The best WSNM is obtained for IG-P mode FINFET SRAM and IG-N has the minimum WSNM.

Table 1. WSNM of the different modes of SRAM cell

Supply Voltages (Vdd)	WSNM (mV)			
	SG Mode	LP Mode	IG-P Mode	IG-N Mode
0.4V	189.03	188.9	196.91	180.28
0.35	164.4	164.07	171.54	156
0.3V	139.39	138.85	145.52	134.47
0.25V	113.8	112.95	118.57	106.56
0.2V	87.3	85.96	90.35	81.03
0.15V	59.46	57.28	60.51	54.45
0.1V	29.95	26.19	28.87	26.28

4.1.2 Read Stability

During read operation the word-line is kept high and bit-lines are pre-charged to supply voltage, the internal node of the circuit which represents logic “0” gets pulled upwards through the access transistors due to the voltage dividing effect across the access transistor and the driver

transistor. This increase in voltage severely degrades the SNM during read operation. The SNM degrades during read. Here, SNM during read operation in sub threshold region has been calculated and is shown in Figure 7 of the four different SRAM cell configurations. It can be seen clearly that RSNM reduces with supply voltage which indicates the effects of voltage scaling. Almost four different circuit's gives approximately same RSNM. The LP-IGN node gives better RSNM among the four different circuits.

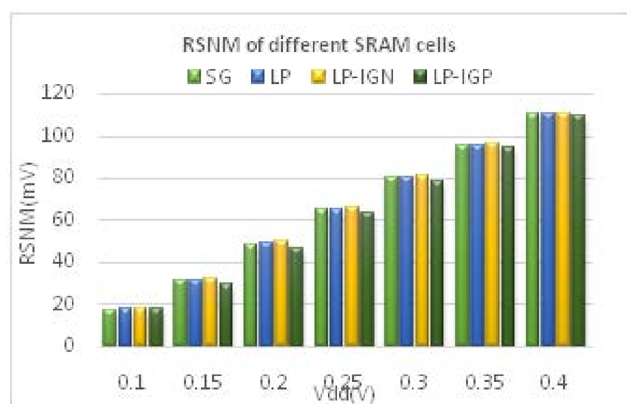

Figure 7. RSNM of different SRAM cells.

4.1.3 Hold Margin

The hold margin is used to analyze the retention voltage of the cell which is one of the important criteria in determining the stability of the cell. The hold margin has been calculated for the various FinFET SRAM circuits in sub threshold region and can be seen that from Figure 8 that IG-P mode FinFET SRAM has maximum hold margin among the four circuits the maximum value for IG-N which is 110.9 mV and LP and SG mode is 110.37mV and IG-P has minimum which is 109.39mV at 0.4 supply voltage.

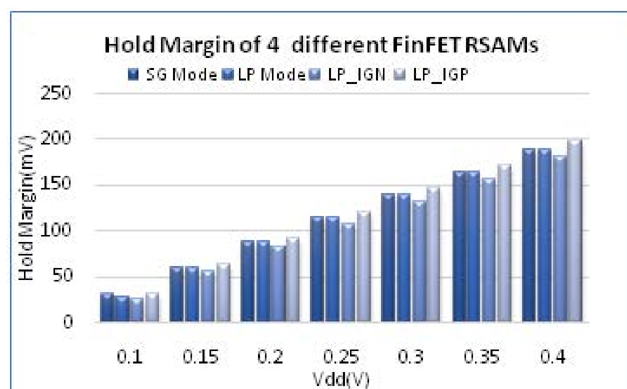

Figure 8. Hold margin of 4 different SRAM cells.

4.2 Leakage Current

Power consumption is a key factor in all the handheld and multimedia devices since these devices should have ultra-low power dissipation. In small devices the leakage power consumption is one of the most concerning factor, in this paper, leakage current has been found for all the four circuits in sub threshold operation which is as shown in Figure 9. Though, LP mode has the minimum leakage current and so does the leakage power, the IG-P also has less power consumption as compared to IG-N mode FinFET SRAm.SG mode has the highest leakage current.

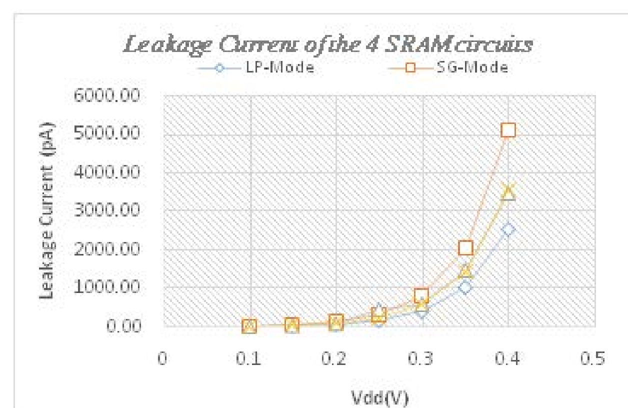

Figure 9. Leakage current of 4 different SRAM cells.

5. Conclusion

Among the four different SRAM circuits, IG-P has the stability factories. Write SNM, Read SNM and hold margin. The LP mode and SG mode FinFET SRAM has almost same SNM while IG-N gas minimum stability among the four circuits. The LP mode has minimum leakage current; next the IG-P mode FinFET.SG Mod has the highest power dissipation, so in terms of stability IG-P and LP mode can be the best candidate. Overall, for both stability and low power IG-P mode is the best candidate. Further, there are many more possibilities to improve the stability and leakage issues by changing the FinFET circuit parameter like Fin height, number of Fins, thickness of the Fins etc. Power reduction techniques can also be used for further reduction in leakage power.

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