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Performance Analysis of Reversible ALU in QCA

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Abstract

Quantum spot Cell Automata (QCA) based reversible method of reasoning is the foundations of creating nanotechnological figuring structures. It ensures enormously low power usage with high thickness and working repeat. Programmable reversible method of reasoning is ascending as an approaching basis arrangement style for execution in present day nanotechnology and quantum preparing with unimportant impact on circuit warm period. Late advances in reversible method of reasoning using and quantum PC figuring mull over improved PC building and math basis unit designs. This work focuses on plan of a powerful reversible ALU (Arithmetic Logic Unit) and its affirmation in QCA. We have considered existing 3 × 3 M-R Gate as the essential building block, a 4*4 reversible method of reasoning entryways (M-R Gate with immaterial delay and orchestrated to convey a grouping of genuine relies on settled yield lines in perspective of programmable select data lines. We similarly display QCA utilization of M-R passage with slightest cell check. The proposed ALU requires only 6 entry ways, which is more locale capable than the present work. It is repeated using QCA Designer.

Keywords: Arithmetic and Logical Unit U, Marrision-Ranganathan, Quantum Dot Cellular Automata, Reversible Logic

1. Introduction

The prototype based model implementation of the standard CMOS circuits with certain limitations have been overcome with the use of developing QCA approach which was first exhibited by Lent et al[1]. The ideal conditions of QCA are its ultra-low power usage, high squeezing thickness and speed of operation[2]. The information streams with no voltage supply in the QCA based circuits what's more, this gives QCA a basic use in the nanotechnology. The matched information which courses through the quantum cell encoded as a restricted charge in the cell. A quantum cell contains four to eight quantum spots, where the position of the electrons in each touch is controlled by columbic drive. This paper depicts the one bit ALU which performs the logical as well as arithmetic operations.

Reversible method of reasoning is a promising figuring arrangement perspective which shows a procedure for building PCs that convey no glow dispersal. Reversible enrolling risen along these lines of the usage of quantum mechanics norms towards the progression of a comprehensive figuring machine. Specifically, the nuts and bolts of reversible enlisting rely on upon the association between entropy, warm move between particles in a structure, the probability of a quantum atom including a particular state at any given time, and the quantum electrodynamics between electrons when they are in closeness. The fundamental standard of reversible enlisting is that a bijective device with a vague number of data and yield lines will make a handling condition where the electrodynamics of the system mull over conjecture of each and every future state in perspective of known past states, and the structure accomplishes each possible state, bringing about no glow scattering.

2. Fundamentals of QCA

This sector begins with the basic QCA cells as shown up in Figure 1 where rectangular quantum cell with four quantum spots are there in each corner. The electrons present in the spot can tunnel beginning with one

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touch then onto the following yet they can't leave as far as possible. Two electrons are accessible in each cell in opposite corner and according to the position of the electrons in the quantum cell polarization occurs as +1 or -1. There are two sorts of bit approach in QCA as showed up in Figure 1(b) and as requirements be 90 degree and 45 degree wire affiliations is made.

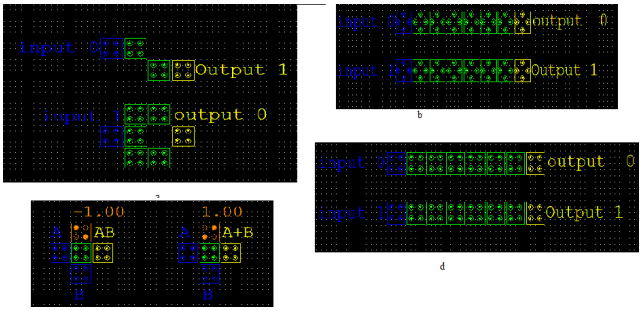

Figure 1. QCA design of Basic ckts.

In an essential QCA rationale with three data sources and one yield is an acknowledgment of larger part door or lion's share voter and designed asAlso, and additionally door. The circuit design in Figure 1(c) demonstrates thearrangement of lion's share door which demonstrates the execution asyield Y=AB+BC+CDwhere A,B,C,D are the information sources and thefocal is the gadget cell. Figure 1(d) demonstrates the essential inverter entryway utilizing QCA and Figure 1(b) demonstrates the data moves through 90 degree and 45 degree wire.

3. Clocking in QCA

Multiplexed examination framework is used as a piece of QCA justification The planning is given to the circuit by genuine controlling the potential limits between the neighboring spots in the quantum cell. With the development of the potential obstruction tunneling potential diminishments and electrons in the spots start to cutoff themselves. Exactly when the tunneling potential is high electrons delocalize themselves and cause an uncertain potential. In QCA based circuit arrange particular cells are not coordinated overall, a social event of cells is isolated into subgroups and multiplexed clock signs are associated moreover. Switch, hold release and loosen up are the four times of a clock signal. The polarization of a QCA cell is settled in the trading stage dependent upon the polarization of the commitment of that cell on the present moment. In the release and loosen up time of the data cell does not impact the polarization of the QCA cell.

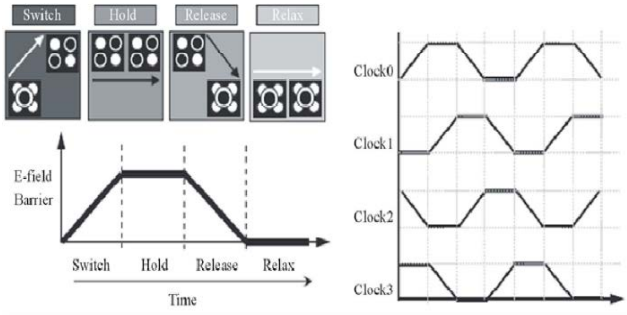

Figure 2. QCA clocking.

4. M-R Gate

MRG (Marrison-Ranganathan) Gate is a 4*4 reversible logic gate and is a programmable gate. MR gate block diagram s shown in Figure 3. the outputs produced by this gate are P=A,Q=A XOR B,R=A XOR B XOR C,S=((AB XOR D) XOR (A XOR B) XOR C)). The truth table is shown in Table 1. When this gate is used as aprogrammable reversible logic structure with two inputs as select inputs it performs 4 logical operations namely OR, NOR, XNOR and XOR.

Table 1. Truth table of M-R gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	0	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	1
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

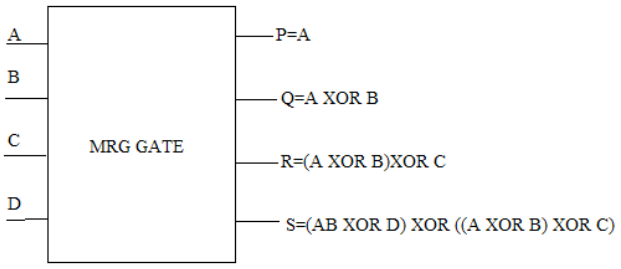

Figure 3. Block diagram of MRG.

Table 2. Programmable inputs to perform calculation

Sel0 (C)	Sel1 (D)	R	S
0	0	XOR	OR
0	1	XOR	NOR
1	0	XNOR	NOR
1	1	XNOR	OR

The QCA implementation of MRG is shown in Figure 4.

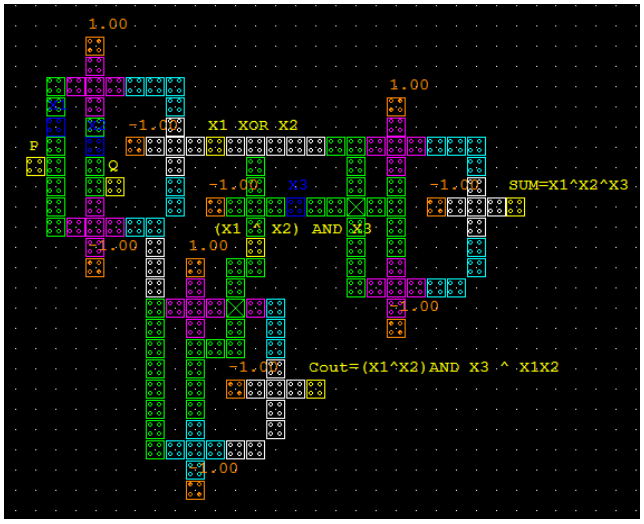

Figure 4. QCA layout of MRG.

5. Implementation of an ALU using Reversible Logic Gates

Two 1-bit ALUs are exhibited in this area. The primary uses the MRG door and HNG door to deliver six legitimate estimations: ADD, SUB, XOR, XNOR, OR and NOR. The ALU has 8 sources of info and 8 yields. The sources of info comprise of three information inputs (A, B and C in) and five settled info select lines. The eight yields are: A, S0, S3 and S4 proliferated to the yield, A ⊕ B, SUM, Cout, Overflow and Result. The cost of this 1-bit ALU is 24, what's more, the most pessimistic scenario deferral is 16. For n-bit ALU gadgets, an expansion cost of 2 is brought about per bit keeping in mind the end goal to engender S1 and S2 to different bits. The results of the proposed ALU are listed in Table 2.

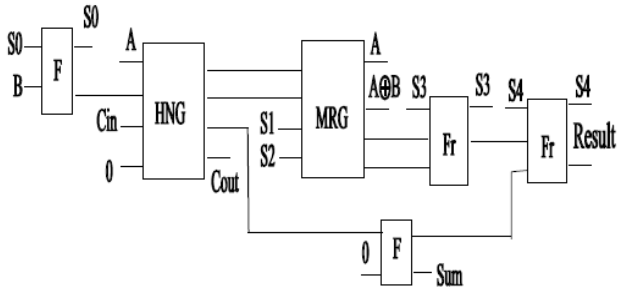

Figure 5. Block diagram of an one-bit ALU.

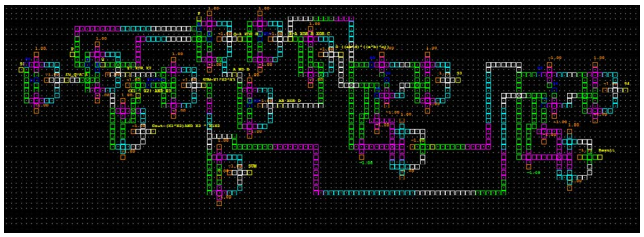

Figure 6. QCA implementation of one-bit ALU.

6. Simulation Results

The simulation results are show in Figure 8 and this QCA Design is compared with the existing CMOS technology design. Where the QCA technology has many advantages like reduced area, improved speed less poer consumption. the comparison Table 3 is given.

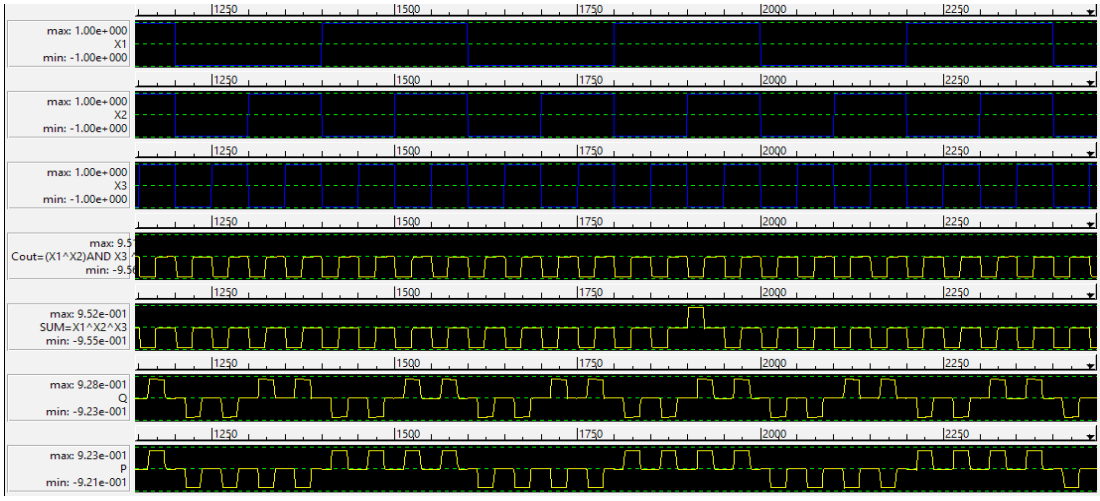

Figure 7. Simulation output of MRG in QCA.

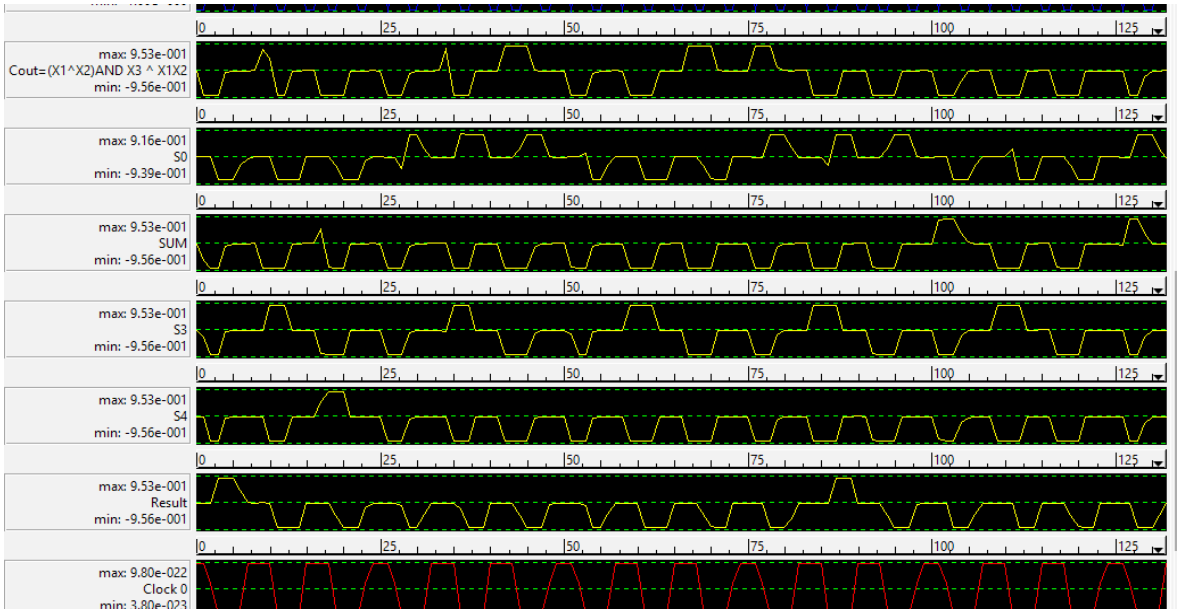

Figure 8. Simulation output of one bit ALU QCA.

The comparison between CMOS and QCA design is been done and the below Table 3 summarizes the comparison. QCA Design has the more area efficient ($0.24nm^2$) than the CMOS design. and power dissipation is comparatively low (5.73e-7nW)

Table 3. Comparison between QCA and CMOS design

Parameters	CMOS	QCA
No. of cells	2	969
Area (nm^2)	16.4	0.24
Power(nW)	345.9	5.738e-7
Dealy(nS)	108	11.90

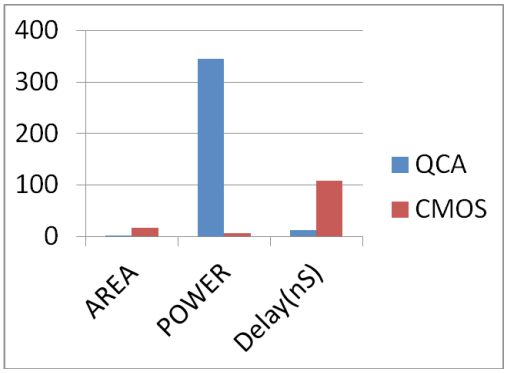

Figure 9. Graphical representation of comparison between QCA and CMOS.

7. Conclusion

A QCA based 1-bit ALU is designed which achieves reduced area than all the existing QCA ALU. The proposed ALU has total cell count of 969. The delay required for proposed ALU structure is 11.904ns which is less than CMOS in which 108ns is needed. The area has been drastically reduced in QCA compared to CMOS design. The functionality is checked by using QCA Designer simulation tool The Future extension of our work is to design 4 bit ALU in QCA.

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