

Low Power Realization of Subthreshold Digital Logic Circuits using Body Bias Technique

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Abstract

Background/Objectives: As technology scaling down, subthreshold operation is playing a vital role in the design of digital circuits to achieve ultra low power consumption with considerable performance. **Methods/Statistical Analysis:** This paper presents a novel body bias technique, where the body terminal of NMOS is reverse biased to VDD which reduces the subthreshold leakage. The basic logic gates are designed using proposed body bias scheme. To analyze the performance, standard 28 transistor full adder cell is implemented using the proposed technique and the performance parameters - power, delay, PDP are calculated and compared with the conventional CMOS Full adder. The simulations are done in cadence 90 nm technology for VDD = 0.2v. **Findings:** The simulation results show that the circuits designed using the proposed technique achieves more than 31% savings in power and more than 15% savings in PDP than traditional body bias technique used in static CMOS configuration. **Applications/Improvements:** These circuits are widely applicable in portable battery operated devices such as cellular phones, wearable electronics and remote sensors where ultra low power consumption is required with low to medium performance.

Keywords: Body Bias, CMOS, Full Adder, Logic Gates, Subthreshold Operation, Ultra Low Power

1. Introduction

With the advancements in technology towards the sub-nm regime, subthreshold region of operation is gaining more importance¹. Digital circuits operating in subthreshold region use a supply voltage less than the threshold voltage of the transistors. In this region, the circuits consume less energy but at the cost of degradation in the performance. Until as of late, maximizing the frequency of operation overwhelmed to the point where this weak inversion or subthreshold region operation gathered very little focus. Recent explorations in applications where low energy operation is required, demands subthreshold circuits. These advancements towards portability for which subthreshold circuits are appropriate have made into two classes of applications². More energy constrained systems and portable battery operated devices are the two different classifications. In the energy constrained systems energy conservation is the primary constraint

where performance is of secondary. Portable battery operated devices require high performance for sometime however likewise spend some significant divisions of their operations doing non-execution assignments. Mobile phone is the best example, as it remains in idle mode for many hours, until it receives the input from the wireless link or the user. Hence subthreshold circuits are the ideal ones for these kind energy constrained and portable applications.

When the PMOS and NMOS drive the same current, the operation of circuit with minimum supply voltage occurs. In MOS transistor, the subthreshold conduction takes place when the applied gate voltage is under the threshold voltage (V_{th}). In long channel devices this V_{th} is independent of the drain bias, but in sub-micrometer channel length devices the scenario is different and causes Drain Induced Barrier Lowering (DIBL)³. The general equation for subthreshold current is⁴:

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$$I_{sub} = I_0 e^{\frac{(V_{gs} - V_T)}{nV_{th}}} \quad (1)$$

$$\text{and } I_0 = \mu_0 c_{ox} \frac{W}{L} (n-1) V_{th}^2 \quad (2)$$

Where

VT	Thermal voltage (KT/q)
V _{gs}	gate to source voltage
n	subthreshold slope factor (1+C _{dep} /C _{ox})
C _{dep}	depletion capacitance
C _{ox}	oxide capacitance
W	Effective channel width
L	length of the channel
μ ₀	zero bias mobility

On considering the static CMOS configuration as a reference, where PMOS body terminals connects to V_{DD} and NMOS body terminals connects to ground. We proposed a novel body biasing technique where PMOS body terminals are forward biased to V_{DD} and NMOS body terminals are reverse biased to V_{DD}. In this paper, the subthreshold logic gates are designed using the proposed body bias technique. Also a conventional 28T full adder circuit is implemented using the proposed body bias logic and different performance parameters are compared with the existing static CMOS full adder design⁴.

2. Impact of Body Bias Configuration

As Silicon on Insulator (SOI) technology devices is more advantageous than the other devices as in MOSFET, it is easy to isolate the body terminal from other electrical points in VLSI⁵. This benefit made convenient to the designers in controlling the threshold voltage (V_{th}) by biasing the body of MOSFET independently. This independent body bias dynamically varies the threshold voltage of the MOSFET and the effect of V_{th} variation due to body bias is known as body effect. The basic equation which shows how body bias impacts on threshold voltage is⁶.

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_B - V_{SB}} - \sqrt{2\phi_B}) \quad (3)$$

where Φ_B flatband voltage
 γ body effect coefficient
 V_{th0} V_{th} with zero substrate bias
 V_{SB} source to body bias voltage.

In order to maintain the minimum threshold voltage (V_{th}) in static CMOS configuration, the body terminals of PMOS is connected to V_{DD} and the NMOS body

terminals connected to ground. In the proposed logic the body of the PMOS connected to V_{DD} (as in standard CMOS configuration) but the NMOS body is reverse biased to V_{DD}. The supply voltage V_{DD} is chosen as 0.2V to operate designed circuits under subthreshold region for achieving ultra low power consumption. When the body of NMOS is biased with negative supply the channel depletion region increases which causes the raise in threshold voltage. As leakage currents are the main sources of power consumption in subthreshold circuits, this raise in threshold voltage significantly reduces the subthreshold leakage current. The body bias design is shown in Figure 1.

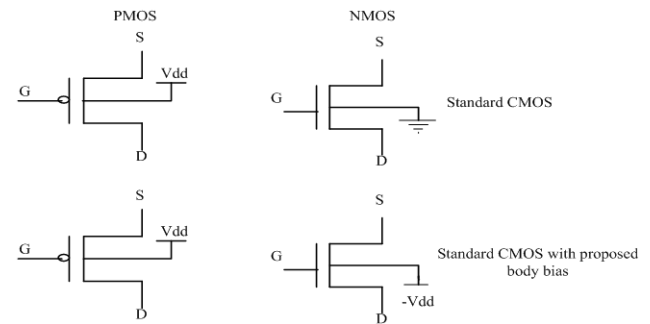
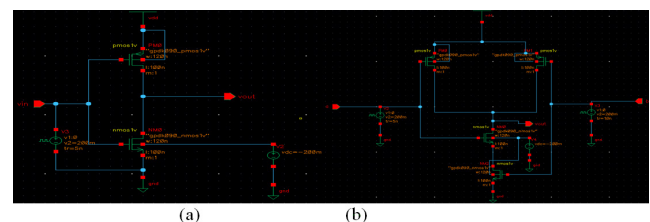


Figure 1. Body connections of MOS devices.

3. Subthreshold Logic Circuits using the Proposed Body Bias Scheme

Logic gates are the essential building blocks of the digital design and they keep on being a theme of interest particularly as devices are scaled under nanometer regime. The basic CMOS inverter and the two input logic gates NAND, NOR, AND, OR, XOR are designed using the proposed reverse body bias logic in cadence virtuoso 90nm technology. And also the standard CMOS full adder which is the basic module in many digital VLSI systems is implemented. The subthreshold designs of some basic gates and 28T static CMOS full adder⁷ using reverse body bias logic is shown in Figure 2.



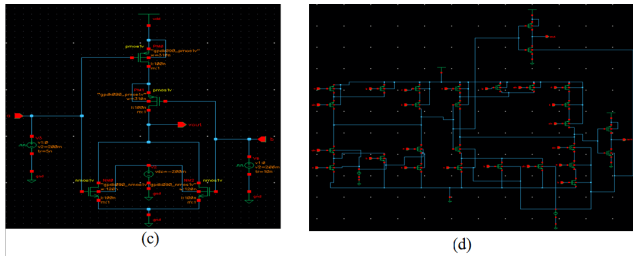


Figure 2. Subthreshold logic circuits using proposed body bias: (a) CMOS inverter; (b) NAND gate; (c) NOR gate; (d) Full Adder.

4. Results and Discussion

The basic logic gates and the 28T CMOS full adder designs using the proposed body bias logic are simulated and compared with the standard CMOS logic. All the designs are operated under subthreshold region and the chosen supply voltage (V_{DD}) is 0.2V. The output waveforms of the designed subthreshold circuits inverter, NAND, NOR, AND, OR, XOR and 28T full adder using the proposed body bias logic are shown in Figure 3.

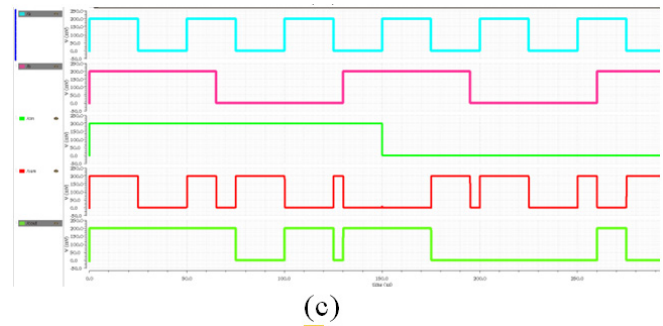
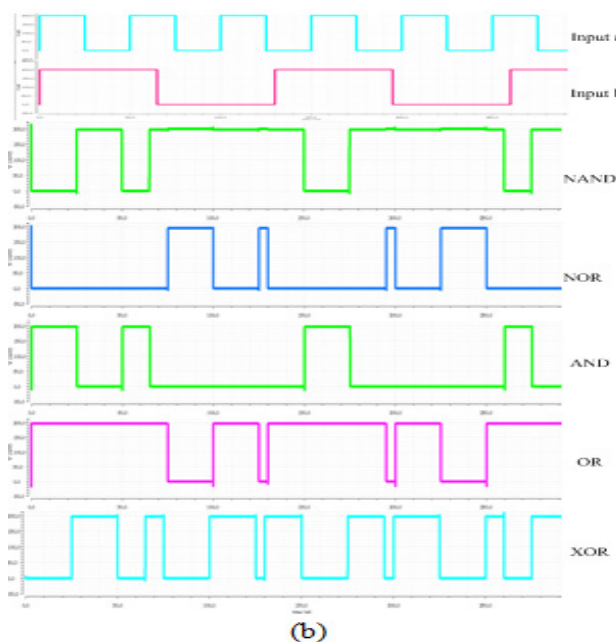
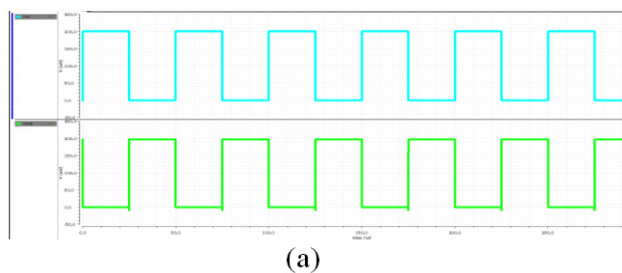


Figure 3. Simulation response of the subthreshold digital circuits using proposed body bias configuration : (a) CMOS inverter; (b) 2 input logic gates; (c) Full Adder.

For proper comparisons all the circuits are operated at frequency of 20 kHz and supply voltage of 200mV. The performance parameters power, delay and PDP obtained from the simulations are compared in Table 1. From Table 1 it is shown that there is a significant reduction in the power and PDP of the designed logic circuits when operated in subthreshold region using the proposed body bias configuration. For a basic CMOS inverter, it is observed that by using proposed body bias more than 33% savings in power and more than 15% savings in PDP are achieved.

Table 1. Performance comparison of subthreshold digital circuits

Design		Power (pW)	Delay (ns)	PDP (aJ)
CMOS Inverter	conventional	172.7	3.71	0.6407
	proposed	114.9	4.7	0.54
CMOS NAND	conventional	200.1	8.75	1.75
	proposed	132.4	9.92	1.31
CMOS NOR	conventional	134.8	9.89	1.33
	proposed	92.63	11.21	1.03
CMOS AND	conventional	291.6	11.02	3.21
	proposed	194.8	12.01	2.33
CMOS OR	conventional	396.6	17.33	6.87
	proposed	271.2	21.62	5.86
CMOS 12T XOR	conventional	670.7	21.52	14.43
	proposed	453.0	18.2	8.24
CMOS 28T FA	conventional	943.4	50.9	48.019
	proposed	644.9	64.6	41.66

To evaluate the performance of the proposed body bias scheme, the implemented full adder is simulated at different supply voltages (V_{DD}) from 0.2v to 1.2V and

the performance parameters power, delay and PDP are compared in the Figures 4, 5 and 6 respectively.

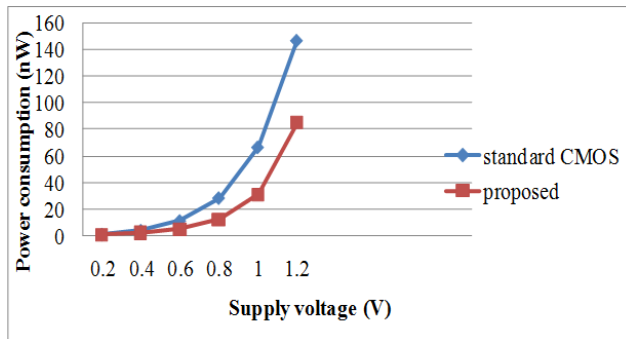


Figure 4. Power comparison at different V_{DD} .

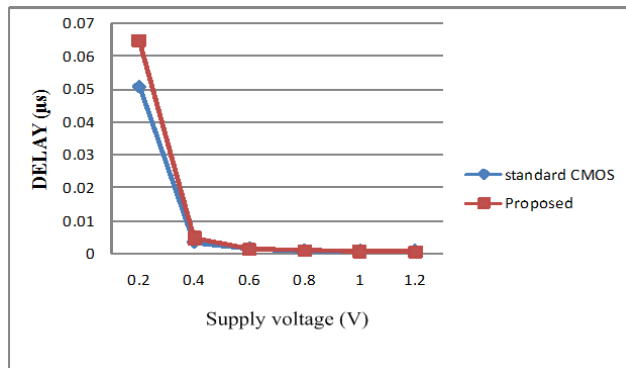


Figure 5. Delay comparison at different V_{DD} .

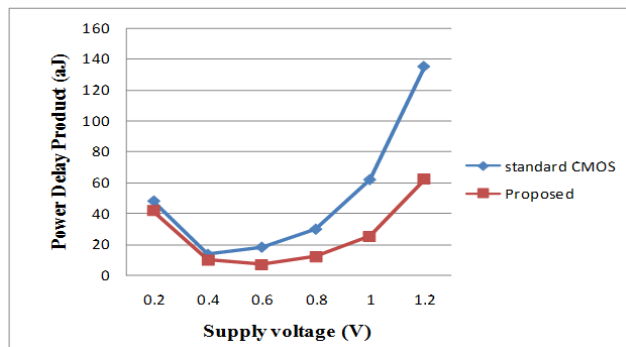


Figure 6. Power * Delay comparison at different V_{DD} .

From the comparisons made in Figures 4, 5 and 6 it is observed that:

- The full adder design using the proposed body bias scheme achieved more than 31% power savings than standard CMOS configuration at different supply voltages from $V_{DD} = 0.2V$ to $1.2V$. Also the magnitude of percentage decrease in power is more with the increase in V_{DD} . This is due to the decrease in subthreshold leakage currents.

- The delay of the full adder design using the proposed scheme dominated the standard CMOS configuration at all the supply voltages from $V_{DD} = 0.2V$ to $1.2V$. Particularly in subthreshold region of operation ($V_{DD} = 0.2V$) the proposed scheme incurred a penalty of 27% increase in delay because of less output driving capability due to the increase in threshold voltage of the device.
- The PDP of the proposed full adder design achieves almost 15% savings compared to the standard CMOS configuration at supply voltages ranging from $V_{DD} = 0.2V$ to $1.2V$.

5. Conclusion

In this paper, the design of the basic logic gates operating in subthreshold region using the proposed reverse body bias technique is presented and is compared with the standard CMOS configuration. The simulations are performed in cadence 90nm technology. The simulations results shows that the circuits designed using the proposed scheme achieved more than 33% savings in power and more than 15% savings in PDP.

Also the 28T CMOS full adder is designed and simulated at different supply voltages from $V_{DD} = 0.2V$ to $1.2V$. The results show that the proposed scheme achieved almost 15% savings compared to the standard CMOS configuration.

Hence from the comparisons, the proposed body bias scheme is one of the best alternatives to achieve ultra power consumption with accepted performance.

6. References

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