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High Performance FIFO Design for Processor through Voltage Scaling Technique

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Abstract

Green computing is making revolution by bringing high speed processor with less power consumption. Our paper is based on this philosophy. **Objectives:** To come out High Performance FIFO for processor by minimizing the power consumption. **Methods/Statistical Analysis:** To make FPGA based design of FIFO we used voltages and frequency scaling techniques. Keeping voltage constant at 2.3 volt we varied frequency from 20MHz to 250MHz and for other experiment we kept the frequency constant and varies voltages from 1volt to 2.3 volt. **Findings**: The power consumption is reduced to 95.79% on voltage scaling where as there is a 4.38% less power consumption on frequency scaling. **Application/Improvements:** It will surely help in futuristic processor development.

Keywords: Field Programmable Gate Array (FPGA), First in First Out (FIFO), Hardware Description Language (HDL), High Performance Design, Voltage Scaling

1. Introduction

A FIFO is a kind of data structure which can be used as buffer in computer system architecture as shown in Figure 1 and Figure 2. It is always useful for us once we have a first in first out kind of requirement. In computer system there is always requirement of buffer or intermediate storage once our data arrive at the receiving PCB (printed circuit boards) at higher rates or in batches. This kind of buffers we can observe in our daily life (for example, a queue of customers at the branch of any Bank). The cash counter of the bank works normally, while the number of customers coming to it is very irregular. If the number of customer would increase and want to deposit their money at the same time, then we must try to form a queue, which works by the principle of first come, first served.

1.1 Field Programming Gate Array (FPGA)

FPGA (Field Programming Gate Array) can be reconfigured after the manufacturing, in other words we can look FPGA as it can be reprogrammed to specific application after manufacturing. FPGA does nothing by itself, so we need to create configuration file or bit file for FPGA. Once we loaded it then FPGA will perform exactly like the digital circuit you want.

For designing energy efficient system FPGA always provide privileges. We can apply different- different

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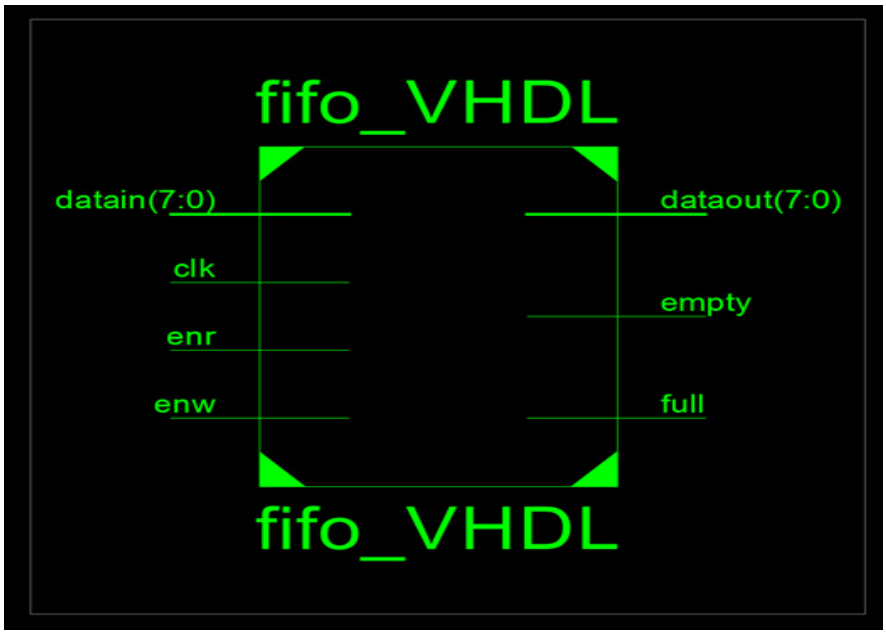

Figure 1. Top Level of Schematic of FIFO.

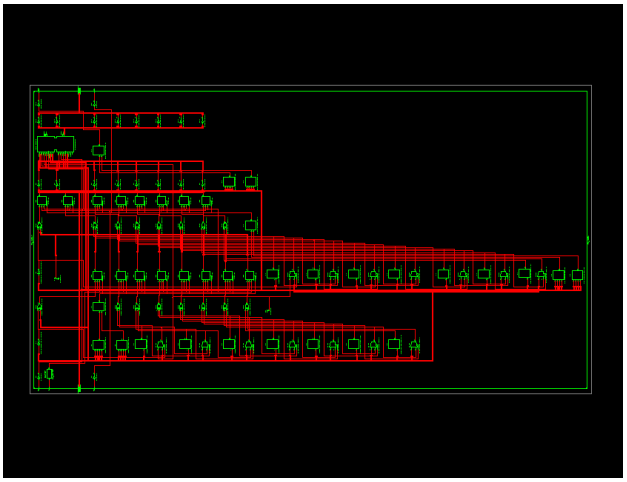

Figure 2. RTL Schematic of FIFO.

techniques like voltage scaling, capacitance scaling for designing power efficient circuit or system. The design implementation using FPGA is explained by the diagram as shown in Figure 3. For configuring FPGA we always use a hardware description language (HDL), we also use it for describing the functionality of ASIC (Application Specific Integrated Circuit). Verilog and VHDL are two most famous hardware description languages.

In FPGA we design our system by third party like Matlab and then it will converted through VHDL language. After the verification and synthesis the design transferred to chip. In Virtex-6 family we have number of differ-

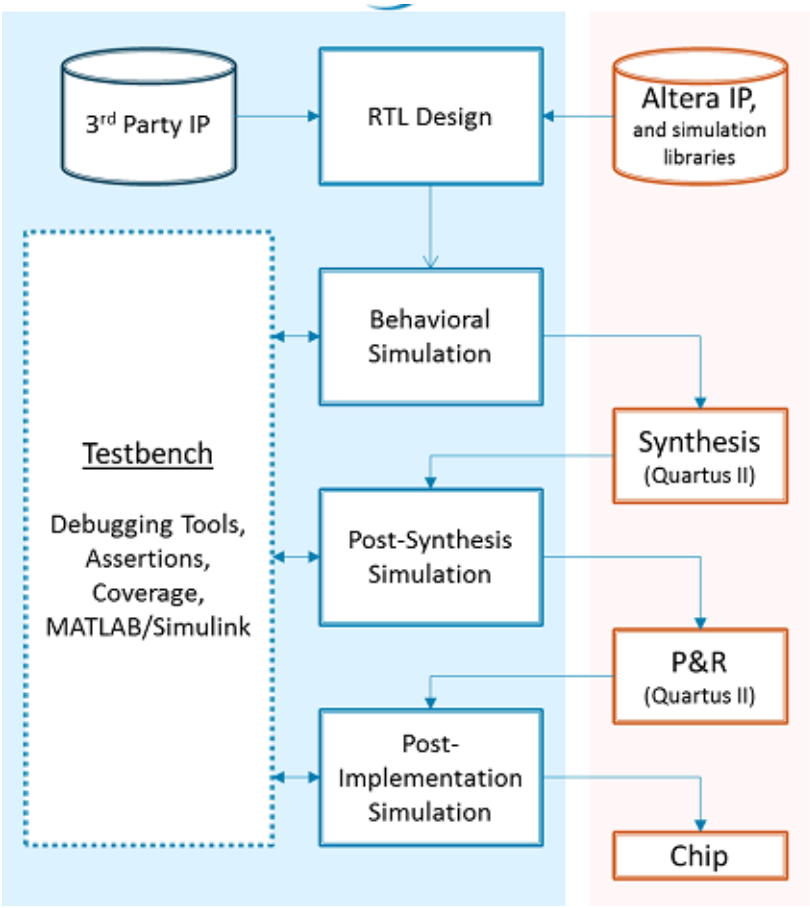

Figure 3.

ent voltages like Output driver supply voltage (VCCO), Core supply voltage (VCCINT), Reference voltage for IO standards (VREF), Auxiliary voltage (VCCAUX), RAM block memory voltage (VCCBRAM), but we are going to consider only two voltages Output driver supply voltage (VCCO) and Auxiliary voltage (VCCAUX) which will be useful for designing the power optimized system.

1.2 Voltage Scaling

Voltage scaling is a power management technique in which we increased and decreased voltages according to circumstances. By applying the voltage scaling technique we can vary the voltage of any electronic devices and we can minimize the power consumption of different electronic devices. We cannot operate our device at peak voltage or less than the base voltage because at peak voltage our device consume more power and at less than base voltage halt state can occur, so it is always advisable to keep our scaling range between the peak and base voltage.

2. Related Work

Adaptive voltage scaling with in-situ detectors in commercial FPGAs[1]. Energy Efficient Counter Design Using Voltage Scaling On FPGA[2]. Energy efficient design and implementation of ALU on 40nm FPGA[3], Energy effi-

cient flip flop design using voltage scaling on FPGA[4], Voltage scaling and aging effects on soft error rate in SRAM-based FPGAs[5], Simulation of Voltage Scaling Aware Mobile Battery Charge Controller Sensor on FPGA[6], Voltage Scaling Based Wireless LAN Specific UART Design Based on 90nm FPGA[7], Energy efficient Reconfigurable Computing with Adaptive Voltage and Logic scaling[8], HSTL IO Standards Based Processor Specific Green Counter[9], Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling on Virtex-6 FPGA[10].

3. Methodology

As shown in figure 4 first we look for the design specification of the device. We converted this design specification into RTL (Register Transfer Level) coding, it describes that how data is transformed when it is passed between one register to another register. After that we apply voltage scaling technique. Now we look for simulation and verification of our FIFO design. The successful verification of design produces logic synthesis in which system is going to implement. For the physical layout of FIFO we

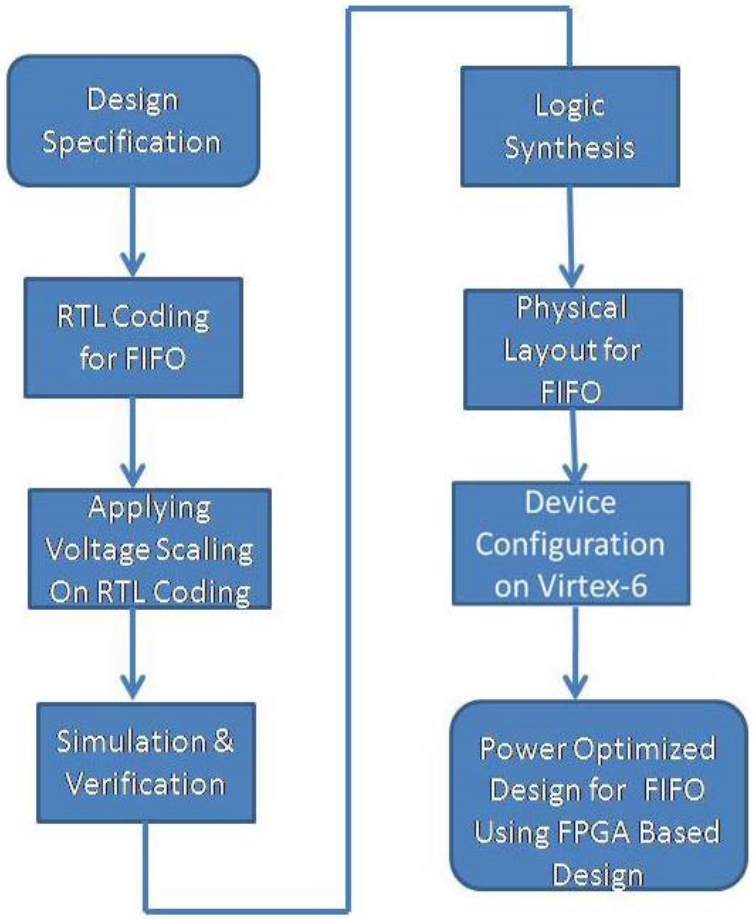

Figure 4. Design Methodology of FPGA.

use the logic synthesis design, now the physical layout of FIFO is configured with FPGA devices. For this work we implement our physical layout on Vertex-6.

4. Experiment

In our work we are going to make FPGA (Field programmable Gate Array) based design of FIFO and apply voltage scaling techniques in which we consider different– different voltages and frequency. For the analysis of the power consumption of FIFO following range of the frequency and voltages has been taken into consideration as shown in table 1 and table 3.

Table 1. Range of Frequencies

Frequency
20 MHz
200 MHz
250 MHz

Following are the Power analysis of different IO standards of FIFO at different frequency at fixed voltage 2.3 Volt while working with AIRTX-7 FPGA. The inference from the table 2 has been made that when we scale down the frequency from 250MHz to 20 MHz then there is 87.5% reduction in IO power and there is 4.38% reduction in total power consumption which is also shown by Bar graph in figure 5.

Now in our second experiment we are going to analysis power of different IO standards of FIFO at different voltages while working on AIRTX-7 FPGA. We are going

Table 3. Different voltages used

Voltage
1Volt
1.5 Volt
1.9Volt
2.3Volt

Table 2. Total Power Analysis at Fixed Voltage

Frequency	Clock	Signals	IOs	Leakage	Total Power
20 MHz	0.000	0.000	0.001	1.042	1.046
200 MHz	0.004	0.002	0.007	1.047	1.083
250 MHz	0.005	0.002	0.008	1.049	1.094

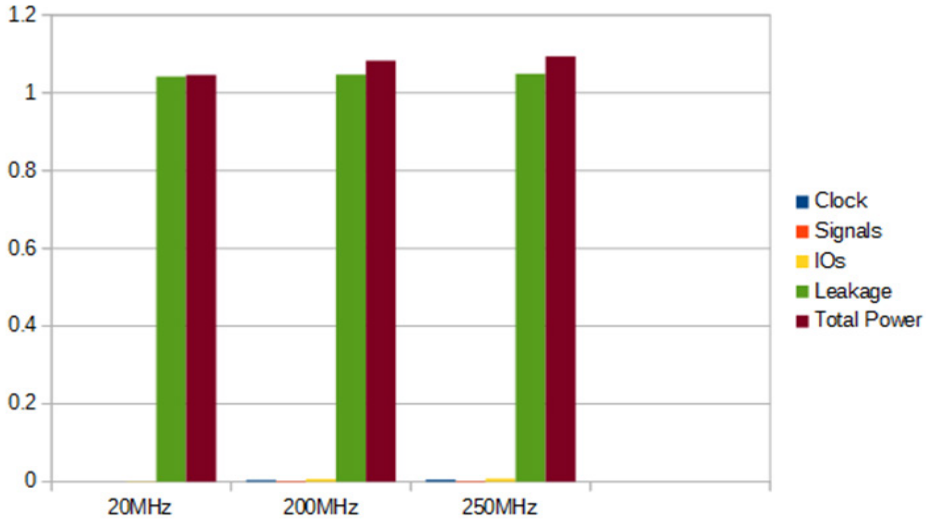

Figure 5. The Power Analysis of FIFO at Different Frequencies

Table 4. Power Analysis at Different Voltages

	Voltage	Dynamic	Quiescent	Total Power
Supply Power (W)	1V	0.001	0.042	0.044
	1.5V	0.002	0.110	0.112
	1.7V	0.002	0.183	0.185
	1.9V	0.003	0.316	0.318
	2.3V	0.004	1.042	1.046

to make frequency fixed and changed the voltage from 1 Volt to 2.3 Volt.

The inference from the Table 4 has been made that when we scale down the Voltage from 2.3 volt to 1 volt then there is 95.79% reduction in total power consumption, which is also demonstrate by Bar graph in Figure 6.

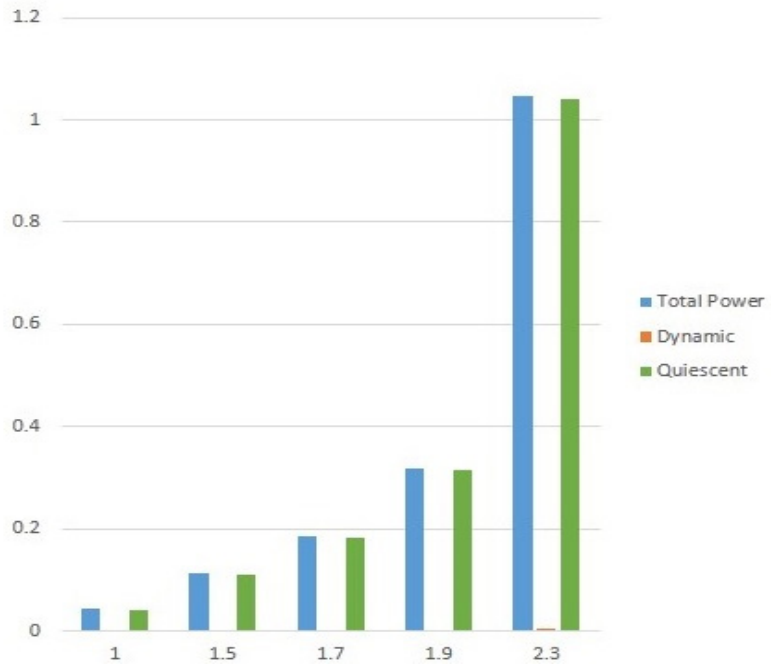

Figure 6. The power analysis of FIFO at Different Voltages.

5. Conclusions

In this work, we design high Performance FIFO for Processor using voltage scaling technique. We realized this design through VHDL. It is concluded that, there is not too much effect on the total power dissipation when the voltage was fixed and changing the frequency between 20 to 250MHz, but we found that once we scale down the voltage from 2.3Volt to 1Volt then there is huge effect on total power dissipation.

6. Future Scope

In this work, high Performance FIFO Design for Processor is implemented on 28nm on Airtex-7,but we have a scope to redesign this FIFO on latest 28nm Virtex-7,65nm Virtex-5 and 40nm Virtex-6, 90nm Virtex-4 FPGA to make the most energy efficient FIFO for processor. We can also take more frequency range to redesign energy efficient FIFO.

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