

Design of Low Power 6T-SRAM Cell and Analysis for High Speed Application

G. Shivaprakash^{1*} and D. S. Suresh²

¹Department of Electronics and Instrumentation Engineering, M. S. Ramaiah Institute of Technology, Vidya Soudha, MSR Nagar, MSRT Post, Bangalore, Karnataka, 560054, India; shivaprakash@msrit.edu

²Department of Electronics and Communication Engineering, Channabasaveshwara Institute of Technology, N.H. 206, B.H. Road, Gubbi, Tumkur –572216 (Near Bangalore), Karnataka, India; sureshstumkur@yahoo.co.in

Abstract

Static Random Access Memory (SRAM) is one of the core components in the digital world. Generally, it consumes enormous amount of power and die area. Thereby extensive research in SRAM is in progress related power dissipation, memory chip area and supply voltage requirement. In this paper SRAM analysis in terms of Static Noise Margin, Data Retention Voltage, Read Margin (RM) and Write Margin (WM) for low power application is considered. Static Noise Margin (SNM) is one of the most essential parameter for memory design because it affects both read and write margin. SNM is related to the threshold voltages of the Negative Metal Oxide Semiconductor (NMOS) and Positive Metal-Oxide Semiconductor (PMOS) devices of the SRAM cell. High Read and Write Noise Margin are also significant challenges in the design of SRAM. Data Retention Voltage (DRV) is calculated for 6T-SRAM cell for high-speed application. Different types of curve are taken straightforwardly to analyses the 6t-SRAM by varying the size of the transistor. Performance analysis is estimated in 6T-SRAM designed and implemented in 90nm technology.

Keywords: Data Retention Voltage, Noise Margin, Read Margin, SRAM, 6T-SRAM, Virtuoso, Write Margin

1. Introduction

Nowadays one of the widely used electronic device or electronic circuit is SRAM¹. Stability in SRAM when designed using the Complementary Metal–Oxide–Semiconductor (CMOS) technologies generally depend on the SNM. SRAM memory technology is used because of its speed and robustness. As the device is scaled down in sizes several design challenges arise in the nanometer size SRAM design. In an SRAM cell operation generally supply voltage scaling is performed. The minimum voltage also referred as DRV is the needed for a SRAM

cell to store the data. Reducing the VDD reduces sub-threshold leakage current and gate leakage. Conversely, when VDD is reduced too far data loss occurs in SRAM. The DRV is applied to preserve data in the bit cells of SRAM. For analyzing high speed SRAM calculation of read margin and WM is necessary. A significant vision in this paper is to analyze 6T SRAM cell is based on noise marginal by evaluating the DRV, Read Margin and Write Margin. Nowadays focus is on low supply voltage which reduces the SNM. The stability of SRAM cell can be analyzed based on the SNM value because performance is proportional to the SNM. Therefore as SNM reduces

*Author for correspondence

the performance of SRAM cell also reduces or vice versa. For improving the performance of a 6T SRAM cell parameter such as Cell Ratio (CR), Pull up Ratio (PR), Voltage Supplies (VDD) is generally considered. The basic introduction to 6T SRAM cell architecture is provided in section 2, section 3 explains the SRAM working and section 4 to 7 elaborates the SRAM w.r.t SNM, RM, WM and DRV. In the section 8 SRAM Implementation Methodology is provided and SRAM's Simulation Results are explained in detail in section 9. The section is concluded in section 10 and references are provided.

2. Static Random Access Memory (SRAM)

Much digital architecture consists of SRAM. In digital architectures, the density of the design and speed of execution is the most criticized element. Devices are scaled to achieve less complexity, supply voltages and threshold voltages. The Figure 1 represents a 6-Transistor memory cell which is widely accepted as the standard memory cell. To achieve high density, the memory cells should be sized properly a conventional 6T SRAM configuration is considered. This 6T SRAM works on 1V power supply conventional 90 nm for its operation when compared to 1.8V in conventional 180 nm. If the supply voltage applied to the operation of SRAM is low, then power consumption is also scaled down. Data bits to be stored in SRAM are applied to the cross coupled inverters.

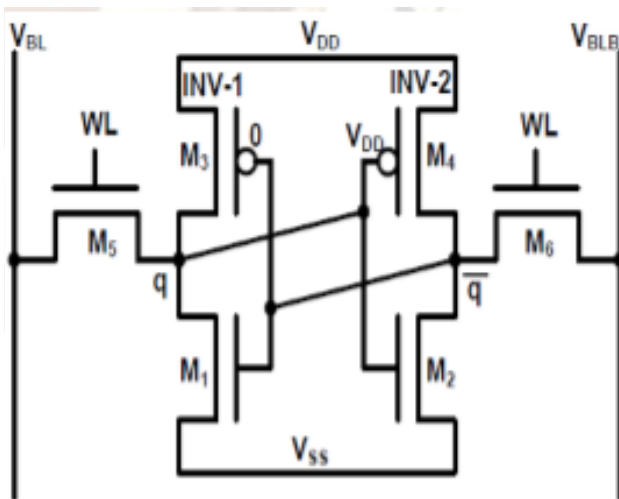


Figure 1. SRAM Schematic.

These cross coupled inverters have two stable states '0' and '1'. Apart from the cross coupled inverters in SRAM additionally two transistors are connected named access transistors and driver transistor. These two transistors are to control the read operation and write operations of 6T SRAM. The SRAM cell is generally enabled by the Word Line (WL) controlling M5 and M6. The transistors M5 and M6 control data transferring in read and write operations. To improve noise margins two bit lines are typically provided in SRAM. To measure the level of weakness in 6T SRAM, the theory of SNM is applied².

3. SRAM Working

The SRAM generally works in three modes of operation, namely hold mode, read mode and write mode³. When SRAM is in standby mode or Hold mode the Word Line is connected to ground. SRAM retains the data without flipping the data. Data is retained in the SRAM till power is applied. When the SRAM is in Read mode, bit-line is pre-charged to VDD and the word-line is set. To read a '0' or '1' the bit-line is generally discharged through the access transistor. Discharging Current is equated through M1 and M5 and is specified in equation 1⁴. The cell ratio is defined as the ratio of the drive transistor and the load transistor. The SNM depend on the Cell Ratio. Therefore it is verified that as the CR increases SNM of the memory cell increases resulting in increase of current in a memory cell [4].

$$\beta_{n,M5} \left\{ (V_{DD} - V_{Q5} - V_{tn}) V_{DSATn} - \frac{V_{SATn}^2}{2} \right\} = \beta_{n,M1} \left\{ (V_{DD} - V_{tn}) V_{Q5} - \frac{V_{Q5}^2}{2} \right\} \quad (1)$$

The equation 1 is simplified to equation 2

$$V_{Q5} = \left\{ V_{SSATn} + CR(V_{DD} - V_{tn}) - \sqrt{V_{DSATn}^2(1 + CR) + CR^2(V_{DD} - V_{tn})^2} \right\} \div CR \quad (2)$$

Where CR is called the CR or β ratio and is represented in equation 3.

$$\text{Cell Ratio (CR)} = \frac{W_1/L_1}{W_5/L_5} \quad (3)$$

If the SRAM is working write mode, the bit-lines in the SRAM are always complementary and to store '0' or '1' discharging through the access transistor is necessary⁵. The PR is defined as the ratio of the load transistor and the access transistor. Therefore it is verified that as the PR increases SNM of the memory cell increases. Current passing through M4 and M6 are equated in equation 4⁶ to ensure that write is success⁷.

$$\beta_{n,min} \left\{ (V_{DD} - V_{tn})V_Q - \frac{V_Q^2}{2} \right\} = \beta_{p,M} \left\{ (V_{DD} - V_{tp})V_{DSATp} - \frac{V_{DSATp}^2}{2} \right\} \quad (4)$$

This equation 4 is simplified to equation 5 as

$$V_Q = V_{DD} - V_{tn} - \sqrt{(V_{DD} - V_{tp})^2 2 \frac{\mu_p}{\mu_n} PR \left\{ (V_{DD} - V_{tp})V_{dsatp} - \frac{V_{DSATp}^2}{2} \right\}} \quad (5)$$

Where PR or α Ratio and is represented in equation 6 is

$$\text{Pullup Ratio (PR)} = \frac{W_4/L_4}{W_6/L_6} \quad (6)$$

4. Static Noise Margin

SNM is the square formed in the mutual normal Voltage Transfer Characteristics (VTC) and mirrored voltage transfer characteristics⁸. The values of CR⁹, PR¹¹ and V_{DD} ¹⁰ typically play important roles in the analysis of the SNM of a 6T SRAM cell. SNM should be of High value for high stability of the SRAM cell. Figure 2 represents a general connection for a SRAM bit-cell holding data and to represent SNM.

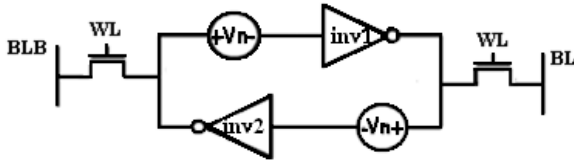


Figure 2. The general setup of SRAM for SNM².

In the SRAM cell SNM is also dependent on RM and write margin. To measure the SNM Butterfly method in 6T SRAM cell is mostly considered where the voltage transfer characteristics curves are rotated to generate butterfly structure¹².

To calculate SNM in CMOS the drain current is considered and is specified as

$$I_D = \frac{1}{2} \beta (V_{GS} - V_T)^2 \quad (7)$$

$$I_D = \beta V_{DS} \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) \quad (8)$$

In the saturated and linear regions, SNM is calculated as

$$SNM_{\text{sat}} = V_T - \left(\frac{1}{(k+1)} \right) \left\{ \frac{V_{DD} - \frac{2r+1}{r+1} V_T}{1 + \frac{r}{k(r+1)}} \frac{V_{DD} - 2V_T}{1 + k \frac{r}{q} + \sqrt{\frac{r}{q} (1 + 2k + \frac{r}{q} k^2)}} \right\} \quad (9)$$

$$r = \text{ratio} = \frac{\beta_d}{\beta_a} \quad (10)$$

$$q = \frac{\beta_p}{\beta_n} \quad (11)$$

V_T = Threshold voltage

$$k = \left(\frac{r}{r+1} \right) \left(\left\{ \frac{r+1}{r+1 - (V_S)^2 / (V_T)^2} - 1 \right\} \right) \quad (12)$$

$$V_S = V_{DD} - V_T \quad (13)$$

$$V_r = V_S - \left(\frac{r}{r+1} \right) V_T \quad (14)$$

From the graphical analysis the VTC of Inverter 2 (inv2) and inverse VTC 1 from Inverter 1 (inv1) is plotted. The two lobed curves formed are generally referred as “butterfly curve” and are considered for the analysis of the SNM in a SRAM.

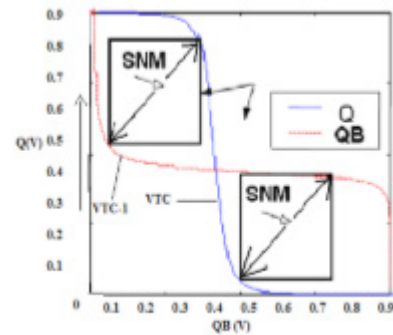


Figure 3. Calculation of SNM.

By referring the Figure 3 the SNM can be considered as the side of the two squares formed between the two VTCs of a SRAM cell the VTC of one cell inverter superposes the voltage transfer characteristic (VTC) of the other cell inverter¹³. The two-lobed graph formed is usually known as a “butterfly” curve and is analyzed to determine the SNM of the SRAM. The SNM from this method with respect to curve represented is defined as the side length of the largest square which can be fitted inside the lobes of the “butterfly” curve.

5. Read Noise Margin

The cell in a read operation it must retain its state. During read operation the cell is vulnerable if the Read-SNM decreases. The reason for vulnerability is that when Read-SNM is calculated the word-line and both the bit-line are pre-charged high. Due to the voltage dividing effect across the access transistor and

drive transits or internal node of the bit-cell representing a zero gets pulled upward through the access transistor thus degrading in SNM during the read operation occurs. The cell may change its state during a read cycle which results in a wrong data. Figure 4 shows VTC curve for RSNM characteristics and based on this curve RM is calculated. The RM defines the read stability of the SRAM cell. In the SRAM cell the data retention in standby mode and read access is a vital constraint. The SRAM cell stability reduces with supply voltage reduction thereby increasing the leakage current resulting from scaling in the technology. If the value of SNM is increased, the read stability of the SRAM cell increases. Therefore a SRAM cell with high RSNM has good read stability.

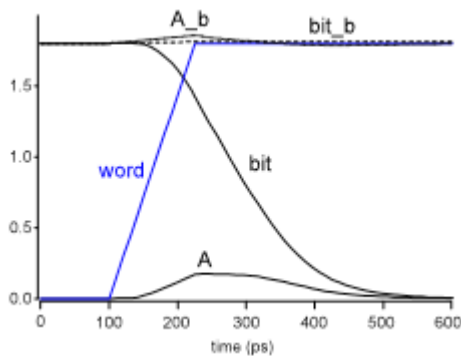


Figure 4. RM from SNM.

6. Write Noise Margin

The write noise margins are obtained by sweeping the inverters (QB and Q). WM is the measure of the ability to write data into the SRAM cell and is defined as the minimum bit-line voltage applied for flipping the state of the SRAM cell. The SRAM Cell write noise margin value usually depends on the cell design and is measured using butterfly curve shown in Figure 5. The input data are sent to the bit-lines during a write mode and to access the cell the word lines are set. If the bit-line is charged to '0' the node of the cell flips state from '1' to '0'. The circuit representing '1' at its output and its bit-line connected to GND is applied to write '0' to that node. WM voltage is considered as the maximum noise voltage at bit lines when write operation is successful. When noise voltages exceeds the WM voltage, then write failure occurs. The most common static approach uses SNM as a criterion. A cell with lower WSNM has poorer write ability.

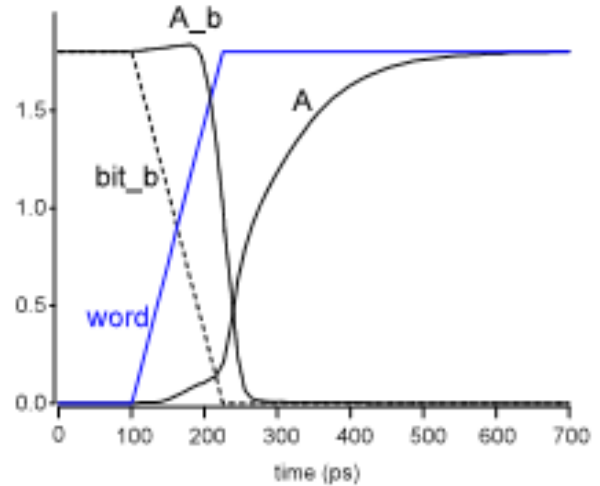


Figure 5. WM Calculation from SNM.

7. Data Retention Voltage (DRV)

DVR is the minimum V_{DD} required for retaining the cell data in the SRAM Cell¹⁵. In the SRAM cell two nodes (q and q_b) are available to store values of '0' or '1'¹⁴. When decreasing the V_{DD} the data in the SRAM cell remain constant and at a particular voltage there is a flip in the state of SRAM cell, the voltage at which flipping occurs the DVR is obtained.

The Voltage Transfer Curves of the internal inverters degrade to such a level that SNM of the SRAM cell reduces to zero as shown in the Figure 6. If the output of the SRAM cell $q='1'$, $q_b='0'$, it flips the value to $q='0'$, $q_b='1'$. The value of the power supply voltage V_{DD} decreasing so DVR should be slightly more than the threshold voltage. The threshold voltage is 200mV so below this value in standby/read mode can cause SRAM to flip state.

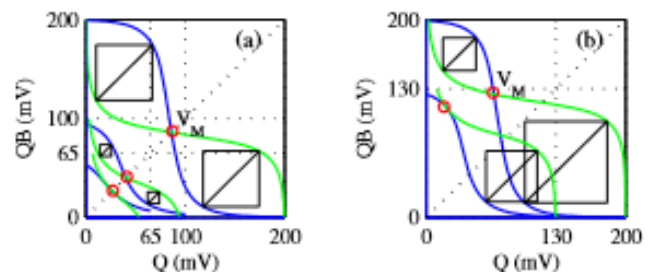


Figure 6. VTC of SRAM cell during DRV calculation.

8. Implementation Methodology

A 6T SRAM is implemented in cadence analog suite in 90nm technology and is represented in Figure 7. Generally in the design the size of NMOS and PMOS transistors is 100nm. To find the CR transistor NM2 is considered as driver transistor and NM3 is considered as the load transistor. The ratio of driver transistor to load transistor considered is in the range of 1 to 2.5 for read operation. Thereby the RM is directly proportional to the cell ratio. To find the PR transistor PM1 is considered as load transistor and NM4 is considered as the access transistor. The ratio of load transistor to access transistor considered is in the range of 3 to 4. Thereby the WM is directly proportional to the PR. The SNM is directly proportional threshold voltage V_{Th} and the DRV is directly proportional threshold voltage V_{Th} . For 90nm technology the threshold voltage of 200mV is generally considered.

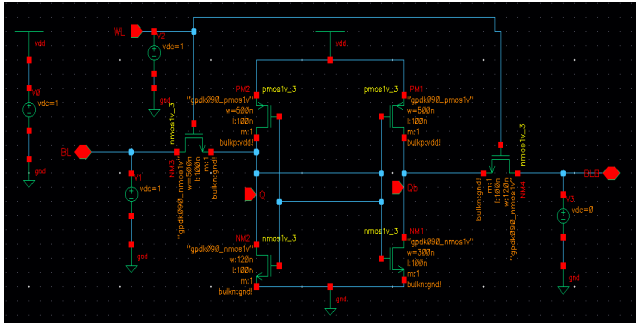


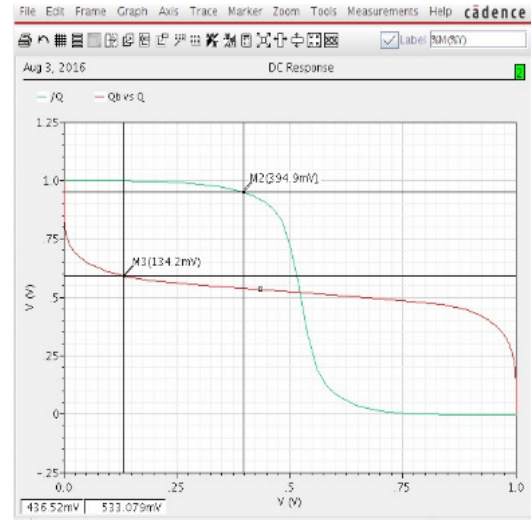
Figure 7. Schematic diagram of SRAM cell.

9. Simulation Results

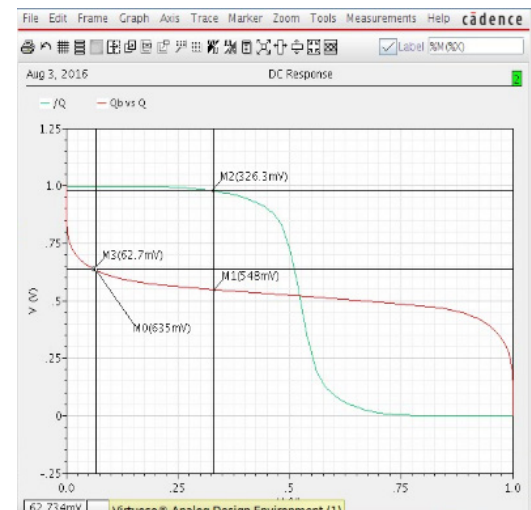
The dependency of SNM with respect to the CR is tabulated in Table 1 and the SNM for CR from 0.8 to 1.6 is plotted in Figure 8 (a) to 8 (e).

Table 1. CR vs SNM

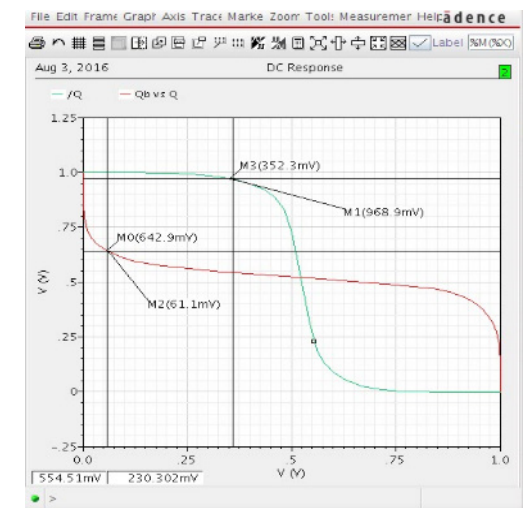
Cell Ratio	W_1	W_5	W_3	SNM
0.8	1.6 μm	2.0 μm	6.4 μm	394.9-134.2=260.7
1.0	2.0 μm	2.0 μm	8.0 μm	326.3-62.7=263.6
1.2	2.4 μm	2.0 μm	9.6 μm	352.3-61.1=291.2
1.4	2.8 μm	2.0 μm	11.2 μm	402.4-59.27=343.13
1.6	3.4 μm	2.0 μm	12.8 μm	410.8-49.61=361.19



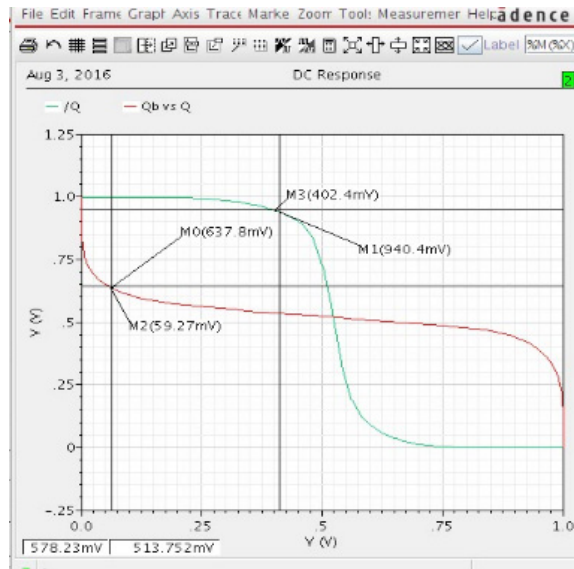
(a)



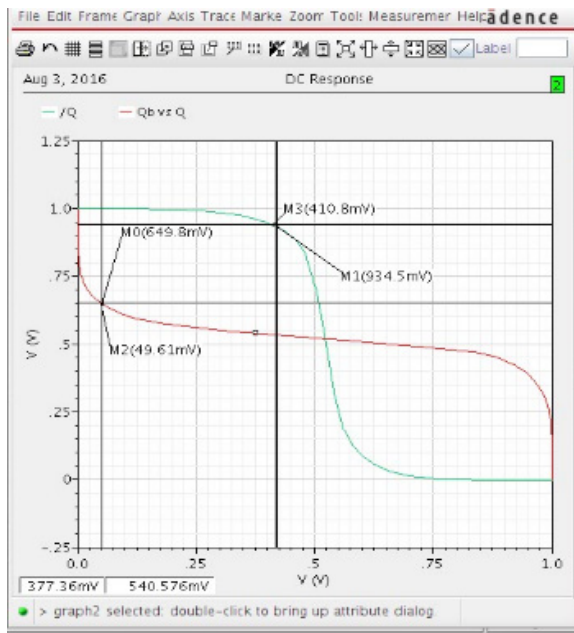
(b)



(c)



(d)



(e)

Figure 8. (a) SNM vs CR when CR=0.8(b) SNM vs CR when CR=1.0 (c) SNM vs CR when CR=1.2 (d) SNM vs CR when CR=1.4 (e) SNM vs CR when CR=1.6.

As the CR is increased the SNM also increase. But the trade-off is the size of the transistors. For example to get SNM as 263.7mV the CR is just 0.8, it means that it requires less area. Whereas when the SNM is 361.19mV the required CR is 1.6 which is twice the area for 263.7mV SNM. Hence it is inferred from Figure 9 that to get better SNM, areas has to be sacrificed.

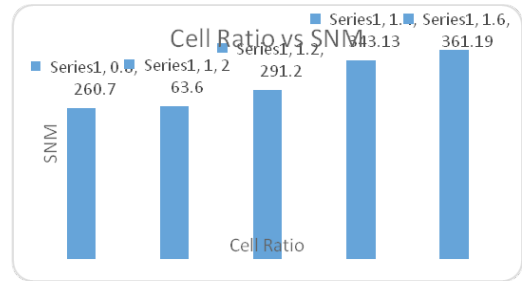
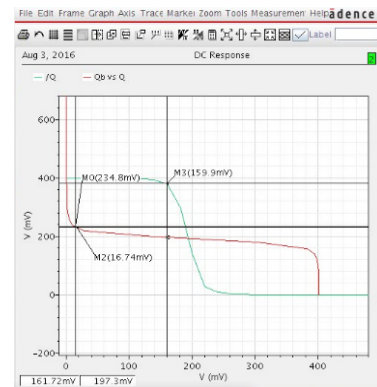


Figure 9. Graph of SNM vs CR.

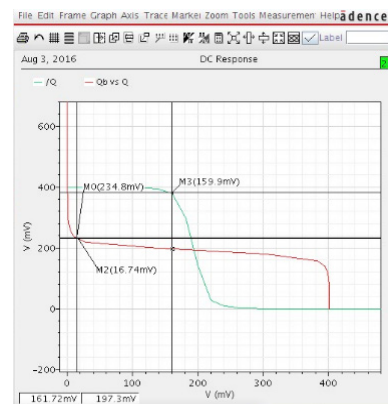
The dependency of SNM with respect to the DRV is tabulated in Table 2 and the SNM for DRV from 1.0 to 0.2 is plotted in Figure 10 (a) to 10 (e).

Table 2. DRV vs SNM

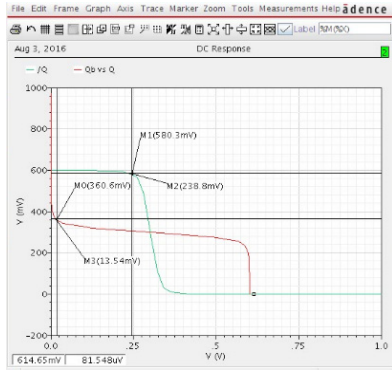
DRV	SNM
1.0	362.5-67.76=294.74
0.8	337.0-47.44=289.56
0.6	238.8-13.54=225.26
0.4	159.9-16.74=143.16
0.2	85.03-40.15=44.88



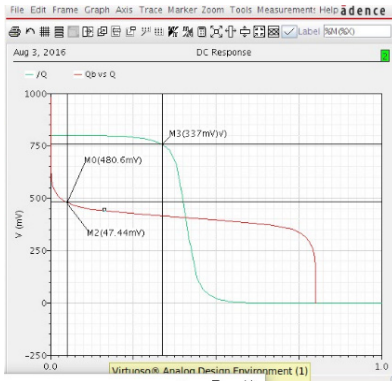
(a)



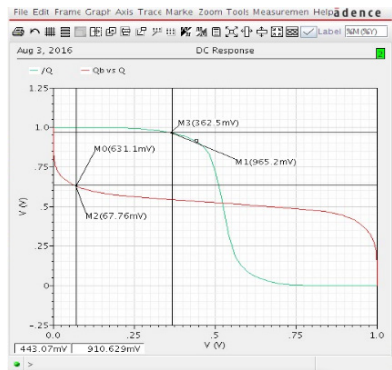
(b)



(c)



(d)



(e)

Figure 10. (a) SNM vs DRV when DRV=0.2(b) SNM vs DRV when DRV=0.4 (c) SNM vs DRV when DRV=0.6 (d) SNM vs DRV when DRV=0.8 (e) SNM vs DRV when DRV=1.0.

For DRV analysis normal $V_{DD} = 1$ V for 90nm. The V_{DD} is reducing till the data is flipped. The data is flipped almost at 200mV because the V_{th} of the transistors in 90nm technology is 180mV. DRV can't be less than the V_{th} . For 90nm technology SRAM DRV = 200mV which should be more than the V_{th} (180mV) Assuming CR = 1 and setting width of transistor M1 and M5 to be 2.0 μm

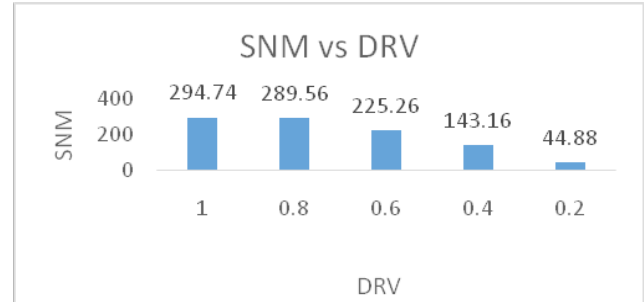
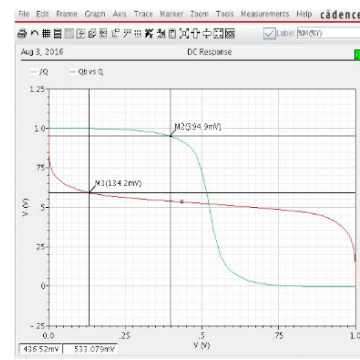


Figure 11. Graph of SNM vs DRV.

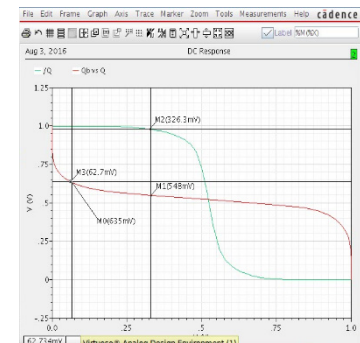
The dependency of SNM with respect to the CR is calculated to find the respective RM which is tabulated in Table 3 and the SNM for CR from 0.8 to 1.6 is plotted in Figure 12 (a) to 12 (e).

Table 3. RM vs SNM

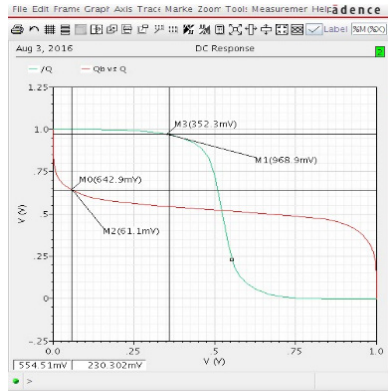
Cell Ratio	Read Margin	SNM
0.8	0.660	$394.9 - 134.2 = 260.7$
1.0	0.810	$326.3 - 62.7 = 263.6$
1.2	0.826	$352.3 - 61.1 = 291.2$
1.4	0.852	$402.4 - 59.27 = 343.13$
1.6	0.879	$410.8 - 49.61 = 361.19$



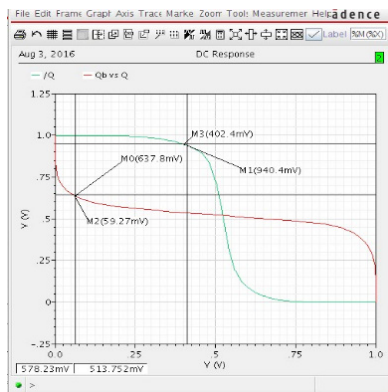
(a)



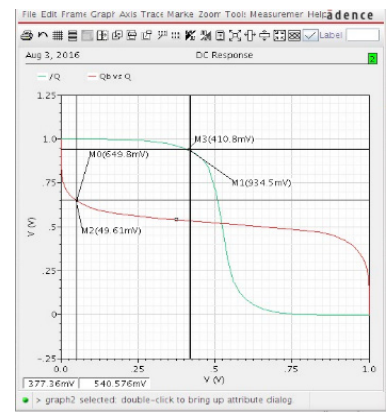
(b)



(c)



(d)



(e)

Figure 12. (a) RM vs SNM when CR=0.8(b) RM vs SNM when CR=1.0 (c) RM vs SNM when CR=1.2 (d) RM vs SNM when CR=1.4 (e) RM vs SNM when CR=1.6.

The RM is calculated as the ratio of SNM to the maximum value while finding SNM. For example, the RM for the case CR=0.8 is calculated as follows.

$$RM = 260.7 / 394.9 = 0.660$$

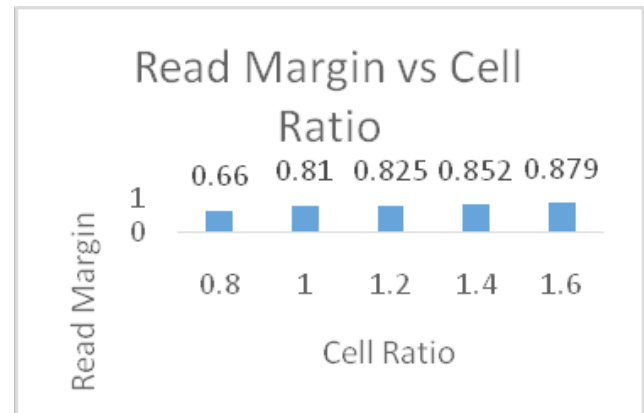
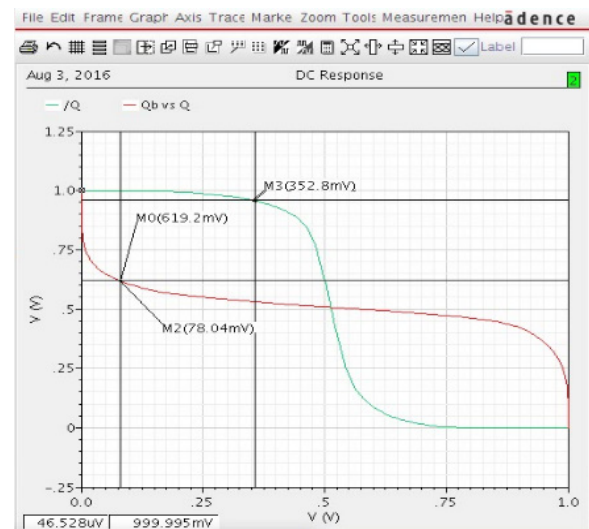


Figure 13. Graph of RM vs CR.

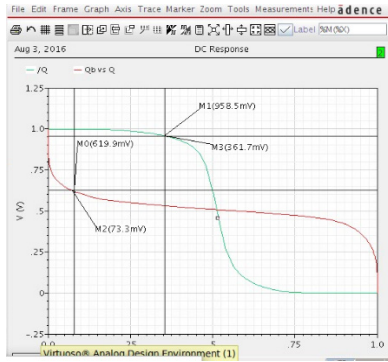
The dependency of SNM with respect to the PR is calculated to find the respective Write Margin which is tabulated in Table 4 and the SNM for PR from 3.0 to 4.0 is plotted in Figure 14 (a) to 14 (f).

Table 4. WM vs SNM

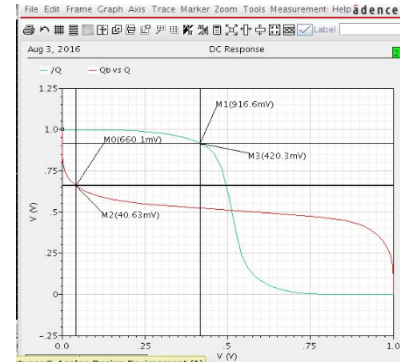
Pull-up Ratio	W4	W6	Write Margin	SNM
3.0	360 nm	120 nm	0.778	352.8-78.04=274.76
3.2	384 nm	120 nm	0.797	361.7-73.3=288.4
3.4	408 nm	120 nm	0.870	383.7-49.71=333.99
3.6	432 nm	120 nm	0.888	389.8-43.36=346.42
3.8	456 nm	120 nm	0.874	423.7-53.23=370.47
4.0	480 nm	120 nm	0.903	420.3-40.63=379.67



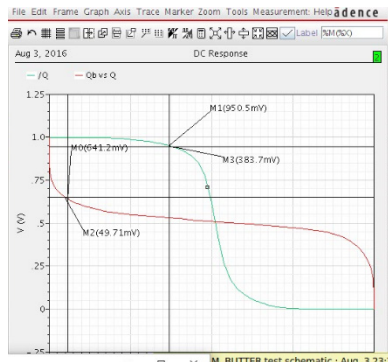
(a)



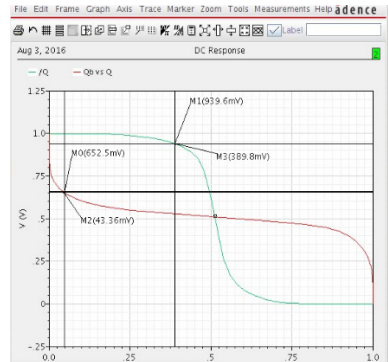
(b)



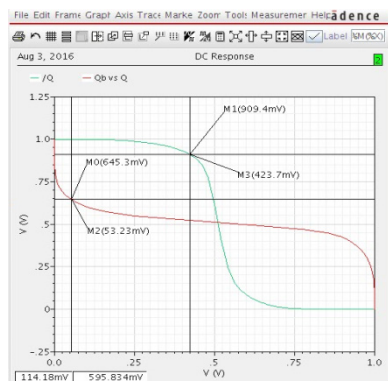
(e)



(c)



(d)



(f)

Figure 14. (a) WM vs SNM when PR=3.0(b) WM vs SNM when PR=3.2 (c) WM vs SNM when PR=3.4 (d) WM vs SNM when PR=3.6 (e) WM vs SNM when PR=3.8 (f) WM vs SNM when PR=4.0.

As the PR is increased, the SNM is also increased. For example when the PR is 3, the SNM is 274.7mV whereas the SNM is 379.67mV when the PR is 4. It is evident that better SNM can be achieved by sacrificing the area of the transistors. The WM can be calculated as follows

$$WM = 379.67/420.3 = 0.903$$

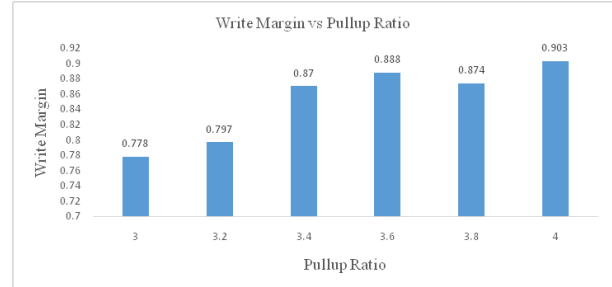


Figure 15. Graph of Write Margin vs Pullup ratio

10. Conclusion

A 6T SRAM is designed using CMOS transistor and implemented in CADENCE design suite in 90nm technology. The SRAM was analyzed by simulating it for parameters like Static Noise Margin. From the SNM, RM and WM are verified and analyzed. The RM and WM are verified by considering the values of CR of 1 to 2.5 and PR of 3 to 4. Performing analysis based on relationship between DRV and SNM, a statistical model is proposed to estimate the DRV value for an SRAM of given size. As the technology is growing, the device dimension is reducing, results in variation of V_{TH} affecting SRAM cell stability

to great extent. From the simulation results good SNM is obtained by scarfifying the area. The DRV of 0.6V is obtained for CR of 1 by setting the width of transistors M1 and M5 same. RM is calculated with respect to SNM is 0.66 and WM with respect to 0.902.

11. References

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