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An Efficient Low Power and High Speed Distributed Arithmetic Design for FIR Filter

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Abstract

Background/Objectives: FIR filters play a vital role in signal processing applications. This research work presents a low power and high speed efficient buffer based Distributed Algorithms and it is analyzed with Electro Cardio Gram (ECG) signal Finite Impulse Response (FIR) filter design. **Methods/Statistical Analysis:** The proposed FIR filter is designed using buffer based DA and it is simulated and synthesized using Cadence digital labs. This is compared with different architectures such as conventional DA, separated look up table DA and LUT less DA. **Findings:** Synthesis report shows that the proposed design has 52% less power dissipation compared with the conventional DA, 21% reduction in delay with separated Look Up Table (LUT) DA and 8% reduction in area with LUT less DA. **Conclusion/Improvements:** Presently this method is applied for ECG signal input with 16-tap FIR filter. This can be extended for higher order filters to achieve better performance.

Keywords: Distributed Arithmetic (DA), Electro Cardio Gram (ECG), Finite Impulse Response (FIR), Look Up Table (LUT)

1. Introduction

1.1 Overview

A Finite Impulse Response (FIR) filter is a digital filter structure that can be used to implement almost any sort of frequency response. An FIR filter is usually implemented by using a series of delays, adders and multipliers to create the filter's output. FIR filters are used to perform signal preconditioning, anti-aliasing, band selection, decimation/interpolation, low-pass filtering and video convolution functions [1–3]. FIR filters can be designed using different methods, Distributed Arithmetic algorithm is one among them. The main units in FIR filters are multipliers and adders. DA is a multiplier-less architecture based on 2's complement binary representation of data which will pre-compute and stored in LUT and bit position reordering.

ECG is the acquisition of electrical activity of the heart captured over time by an external electrodes attached to the skin. Signal processing is a huge challenge since the actual signal value will be 0.5mV in an offset environment of 300mV. An efficient DA architecture of FIR filter is proposed for the ECG signal processing system. Compared with the traditional algorithms, Distributed Algorithms greatly reduce the size of the hardware circuitry to improve the circuit speed of execution.

1.2 Distributed Arithmetic

MAC operation is very common in all Digital Signal Processing Algorithms. DA is an efficient technique for

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calculation of sum of products or vector dot product or inner product or Multiply and Accumulate (MAC). The basic DA technique is bit-serial in nature. DA hides the explicit multiplications by shifts and ROM look-ups[4].

Generally, DA is a bit-serial computation mechanism which uses addition operation to produce the equal results instead of a multiplication operation. Efficiency mechanism is an advantage[5].

$$y[n]=\sum_{k=0}^{k-1}h[k]x[n-k] \tag{1}$$

Where h[k] is the filter coefficients and x[k] is the input data. For the convenience of analysis x' [k] = x [n-k] is used for modifying the equation and we have:

$$y[n]=\sum_{k=0}^{k-1}c[k]x'[k] \tag{2}$$

Then we use B-bit two's complement binary numbers to present the input data:

$$x'[k]=-2^{B}.x_{B}[k]+\sum_{b=0}^{B-1}x_{b}[k].2^{b} \tag{3}$$

Where $x_b[k]$denotes the b[th] bit of x[k], $x_b[k]$ ϵ {0, 1} substituting (3) into (2):

$$\begin{aligned} y&=\sum_{k=0}^{k-1}h[k].\left(-2^{B}x_{B}[k]+\sum_{b=0}^{B-0}x_{b}[k].2^{b}\right)\\ &=-2^{B}\sum_{k=0}^{K-1}h[k]x_{B}[k]+\sum_{b=0}^{B-1}2^{b}\sum_{k=0}^{k-1}h[k]x_{b}[k]\\ &=-2^{B}f(h[k],x_{B}[k])+\sum_{b=0}^{B-1}2^{b}f(h[k],x_{B}[k] \end{aligned} \tag{4}$$

We have $f(h[k],x_b[k])=\sum_{k=0}^{K-1}h[k],x_b[k]$. In Equation 4, it can be observed that the filter coefficients can be pre-stored in LUT and addressed by x_b = [x_b[0],x_b[1],…,x_b [k-1]]. This way, the MAC blocks of FIR filter are reduced to access and summation with LUT.

1.3 Conventional DA Architecture

The conventional LUT based DA architecture for 4-tap FIR filter is shown in Figure 1. The DA architecture consists of three units: the DA_LUT unit, the shift register unit and the adder/shifter unit. The LUT is used to store the pre-computed coefficient values. This gives the main impact in low power design. The main disadvantage of LUT based design is if the filter coefficients too much, then the LUT size become too large. So the different architectures are designed to reduce the size of the LUT.

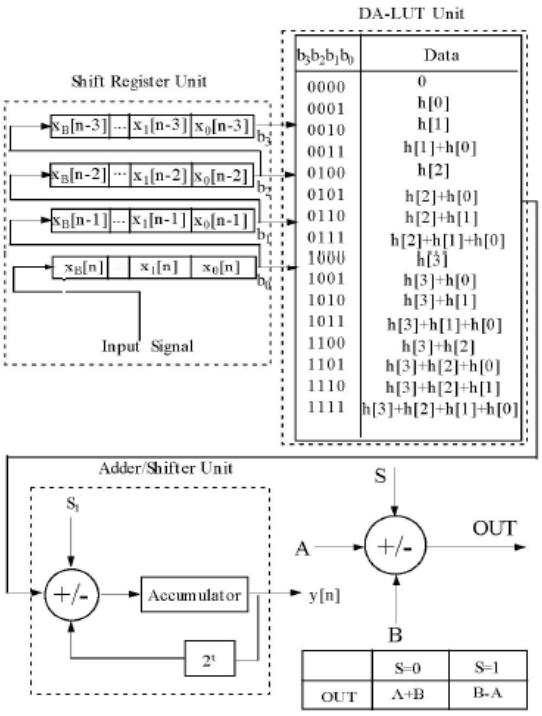

Figure 1. LUT based DA for 4-tap FIR filter.

1.4. Separated LUT DA Architecture

The hardware implementation cost of memory in DA architecture grows exponentially as the filter size increases. So it can be possible to divide the K-tap FIR into L smaller FIR filters. Hence LUT size is reduced to L x 2^M-words. Figure 2 shows the design of 4-tap FIR filter for separated LUT-DA architecture[6].

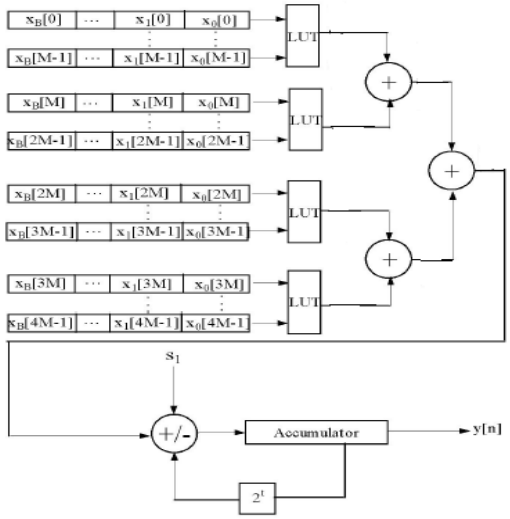

Figure 2. Separated LUT DA architecture for 4-tap FIR filter.

1.5 LUT Less DA Architecture

The LUT Less DA architecture dramatically reduces the memory. In this architecture all the LUT units are replaced by multiplexers and adders[7–9]. By usage of combinational logic circuit, the filter performance will be affected. Figure 3 shows the LUT Less 2 DA architecture for 4-tap FIR filter.

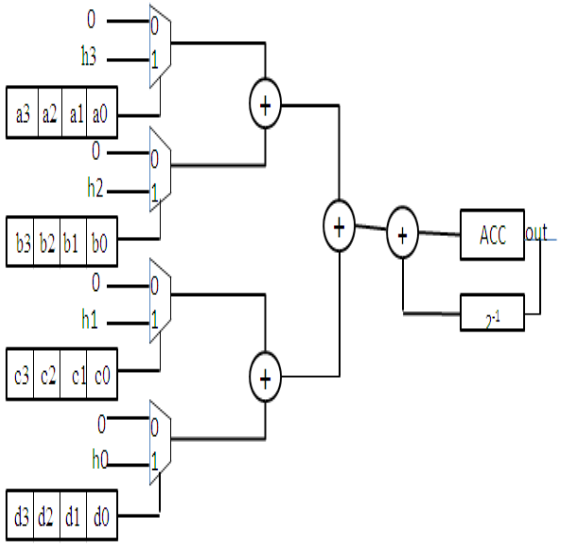

Figure 3. LUT less architecture for 4-tap FIR filter.

2. Proposed Buffer based DA Architecture

The adder units in RAM-based DA are responsible for most of the consumed powers. This is mainly due to all of-the-time operating of adder units. In other words, adder units are used even for direct pass of filter coefficients without logic or level altering. This primarily consumes power in even no-action time slots. Therefore, if the adder unit be active just for its main purpose (addition of two deferent operands) in determined times, the total power consumption of mentioned unit will be reduced.

From the LUT Less DA Architecture for 4-tap FIR filter shown in Figure 3, it understands that when the output of one multiplexer is 0 and the other's is a coefficient value for example, to add h0+0, h1+0 and 0+0, there is no need to use the direct adder. An adder is required whenever the outputs of two multiplexer is a coefficient value. In order to perform this operation we can use tri-states wired-or configuration as shown in Figure 4.

In the proposed LUT, the adder is placed in the input of a tri-state whenever we have two coefficients serves as an enable to the tri-state. The inputs are given to the NAND gates to produce the control signal for the tri-state unit. The output of the tri-state units are feed to the multiplexer. In this manner, the proposed LUT is replaced with tri-state units and multiplexers.

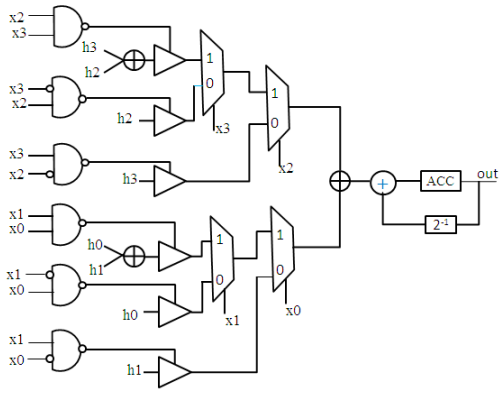

Figure 4. DA LUT architecture using tri-state buffer.

3. Application of FIR Filter: ECG System

Electrocardiography is a diagnostic tool to assess the electrical and muscular functions of the heart. ECG can measure the rate of heartbeat, as well as provide indirect indication of blood flow to the heart muscle. The ECG is a quite simple test to perform. Patches are placed on the skin to detect electrical impulses that the heart generates. These impulses are recorded by the ECG machine. By using an implantable loop recorder ECGs can be invasively recorded[10].

ECG assessment includes the determination of the rate, assessment of the rhythm and evaluation of the electrical conduction patterns. An ECG picks up electrical impulses generated by the polarization and depolarization of cardiac tissue and translates into a waveform[11]. The rate and regularities of heartbeats, the size and position of the chambers are measured by this waveform[12].

The ECG can also provide information about the conduction of electricity by heart muscle cells. By analyzing the shape of the ECG wave, the physician may be able to resolve if there is decreased blood flow to parts of the heart muscle. The occurrence of an acute blockage associated with a myocardial infarction or heart attack can be determined as well.

3.1 Design Specifications

The MATLAB has become powerful tool for the design and analysis of digital signal processing applications. Using MATLAB, the filter coefficients of ECG signal can be calculated.

In order to cut-off frequency of ECG waveform control 110 Hz, using MATLAB to design a sampling frequency of 48 KHz, the filter cut-off frequency of 150 Hz of the FIR filter. Usually, linear phase FIR filter using window function method. MATLAB window function used here to design. The basic idea of the design window function is to select an ideal frequency selective filter and then truncate the impulse response to obtain a linear phase and causal FIR filter. According to the given filter specifications and selected Kaiser window design, 16-order FIR digital low-pass filter characteristic parameters are as follows:

h[0] = h[15] = 0.028219
h[1] = h[14] = -0.0073159
h[2] = h[13] = -0.049899
h[3] = h[12] = -0.061658
h[4] = h[11] = -0.01404
h[5] = h[10] = 0.089426
h[6] = h[9] = 0.20909
h[7] = h[8] = 0.28894

4. Results and Discussions

By using Verilog HDL language Altera platform, Distributed FIR filter has been simulated according to the Distributed Arithmetic Architectures. The input data and filter co-efficient are to be pre-added. The output simulation waveform for the proposed DA is shown in Figure 5.

The synthesis report of different DA architecture using Cadence tool is shown in Table 1.

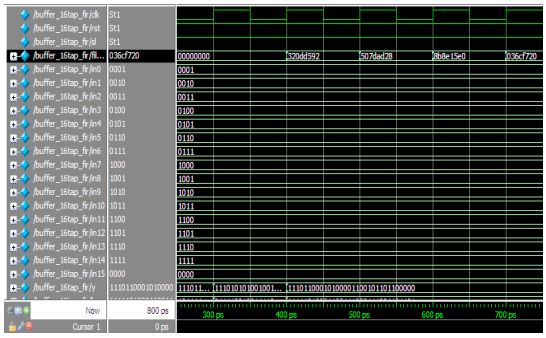

Figure 5. Simulation results using modlesim.

Table 1. Synthesis report using Cadenc Digital Lab

FIR filter design	Power dissipation(mW)	Delay (ps)	Area (μm^2)
Conventional DA based	2.14	459	10279
LUTLess2	7.52	920	5854
Separated LUT DA	8.99	254	4554
DA-LUT using Buffer	1.02	201	5356

The following graph shows the power dissipation, delay and area report of conventional, LUT Less, Separated LUT and Buffer based LUT DA architectures.

Power Dissipation of different LUT architecture is shown in Figure 6. Seperated LUT and LUT Less architecture consume more power than conventional and buffer based architecture. Separated LUT and buffer based LUT have less delay and occupies less area than other conventional and LUT Less architecture as shown in Figures 7 and 8.

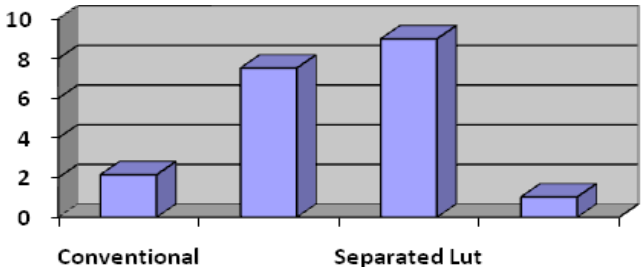

Figure 6. Power dissipation in mW.

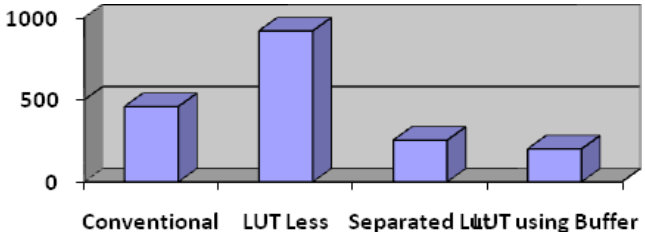

Figure 7. Delay in ps.

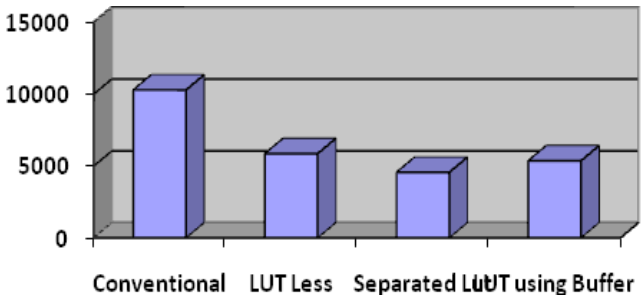

Figure 8. Area report in μm^2.

Comparing with three DA architectures buffer based DA gives the 52% less power dissipation compared with the conventional DA, 21% reduction in delay with separated LUT DA and 8% reduction in area with LUT Less DA.

5. Conclusion

MAC and DA are common used in Digital Signal Processing and Filter design. Different DA LUT architectures design for FIR filters reduce in different aspects such as power, delay and area. Thus to reduce LUT size higher order filters divided into several groups of small filters. The design Distributed Arithmetic unit has the run-time coefficient configurability. The target architecture is designed, verified and simulated with Verilog HDL. For power, delay and area target architecture is synthesized in Cadence digital lab. Currently the proposed method is applied for ECG signal and compared with different DA LUT architectures. The proposed design has 52% less power dissipation compared with the conventional DA, 21% reduction in delay with separated Look Up Table (LUT) DA and 8% reduction in area with LUT Less DA. This can be extended for higher order filters to achieve better performance.

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