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Fault Classification in Mixed Signal Circuits using Artificial Neural Networks

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Abstract

Objectives: The manufactured Integrated circuits are usable only when they are free from any types of faults or error. This is even more essential in complex circuits like analog and mixed signal circuits. This paper focuses on the fault classification in the analog portion of mixed signal circuits using artificial neural networks. **Methods/Statistical Analysis**: All possible catastrophic possible faults in mixed signal circuits are introduced and simulated in an exhaustive manner using Cadence Simulation package. Faults are introduced one at a time and parameters were recorded. The parametric variations obtained through simulation were normalized and are used to suitably train artificial neural networks by creating them as database. The artificial neural network is trained such that it can identify correct functioning of the circuit from its faulty operation and also to further distinguish it into the component at fault, along with the type of catastrophic or hard fault. **Findings**: Comparative results of Feed forward neural networks trained with Levenberg-Marquardt algorithm and Radial basis function networks in the classification of faults are provided. **Application/Improvements:** This can be extended for the other mixed signal circuits by creating the training data using the software simulations. The hardware implementation is possible using the embedded controllers and other types of ANN can also be selected if necessary.

Keywords: Artificial Neural Networks, Faults Classifications, Integrated Circuits, Training

1. Introduction

Increasing levels of integration has led to the convergence of analog and digital circuits in a single substrate of silicon. These circuits, analog and digital may be independent of each other in terms of operation and may have separate input and output pins or can also constitute an entire system designed for a specific purpose, these chips are commonly referred as Application Specific Integrated Circuits (ASIC) and this entire class of integrated circuits are more generally referred as Mixed signal circuits. With the advent of chips with such varied operation and complexity the task of ensuring their proper operation has become important. Testing of mixed signal circuits requires testing of both analog and digital components; of which testing of digital circuits have already established test procedures such as D-algorithm[1], Built-in Logic Block Observer (BILBO)[2], and Level Sensitive Scan Design (LSSD)[3]. Whereas testing of the analog components imposes a major bottleneck in the testing of mixed signal circuits because of non-linear operation analog circuits and unpredictability of the effect of faults. Though, the hard faults models and soft fault models have been established[4]. The effect of these faults in analog circuits

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cannot be stated with certainty as the effect of the fault propagates in all directions (towards the source and also towards the output). The fault values in analog circuits may not show considerable variation (the output parameter may deviate by 1%) and also performance specifications of analog circuits are also defined in a range with upper and lower limits and not a fixed value as in case of digital circuits. This character of analog faults is effectively handled by artificial neural networks since a window is placed on the estimated of the decision boundaries of the network and the network can also be trained to identify small deviation of parameters in relation to other parameters to effectively locate the fault. Several attempts have been made to classify the faults in a considered mixed signal chip using artificial neural networks. In[5] the faults in an R-2R ladder Digital to Analog Converter (DAC) has been classified using a Fuzzy logic based Learning Vector Quantisation network but the DAC chip considered is of lower resolutions. In[6] an expert system based artificial neural network has been used to classify the faults in a mixed signal chip. The chip consisted of a 2bit Analog to Digital converter (ADC) and a 1-bit DAC. In[7] an attempt to classify a faulty and fault free chip has been reported. The circuits have been classified using artificial neural network along with wavelet pre-processing of DAC output current. The method presented is effective and requires a compact neural network but merely distinguishes faulty and fault free circuits does not locate the component at fault. In this paper, classification of faults in the DAC circuit using artificial neural network is presented. The parametric values are recorded during fault free operation and also with each component at fault. The data is normalized and is used to train the neural network. Another set of parametric data with known fault class but which is unknown to the network is used to validate the results of neural network. Feed forward network trained using Levenberg-Marquardt algorithm and Radial Basis Function networks are used for classification.

2. Mixed Signal Circuits

The mixed signal circuits considered are: DAC, Synthetic Aperture Radar (SAR)-ADC, Servo-Tracking ADC, DAC is used for the conversion of digital signals to analog signals. In ADC, analog signal to be converted is compared with the output of the DAC and the digital input at which it magnitude of both the signals become equal is considered as the digital value of analog signal. The digital input

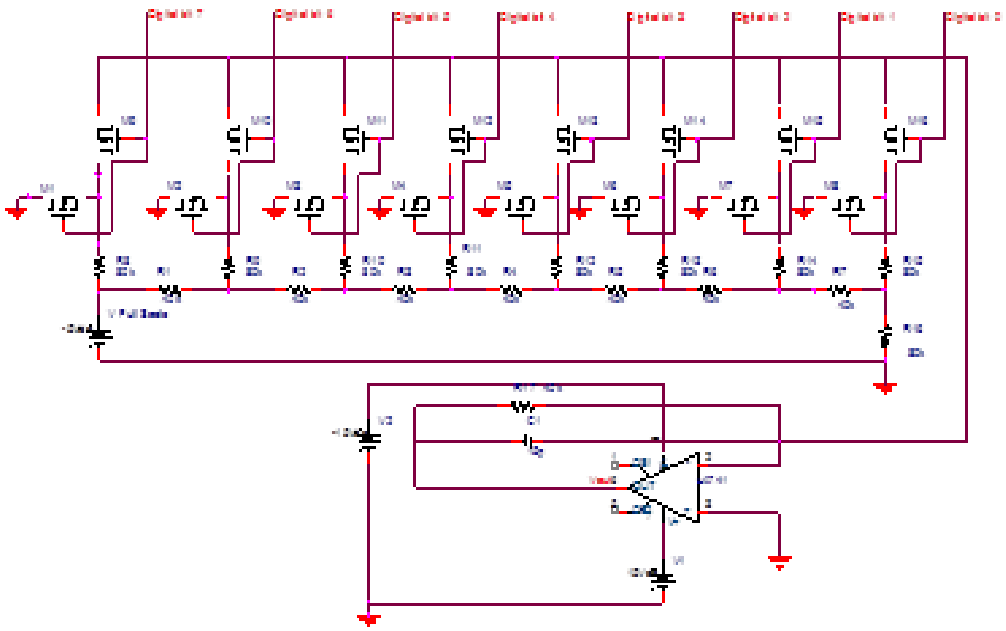

Figure 1. Inverted R-2R ladder digital to analog converter

to DAC may be varied by means of up/down counters or SAR. Hence in all these circuits the proper conversion of signal in DAC. Moreover, it also mentioned[8] that DAC can be used as benchmark for mixed signal test methodologies. The DAC circuit used is as shown in Figure 1.

3. Faults in Digital to Analog Converter

Generally, Faults that occur in electronic circuits are Hard or Catastrophic faults and Soft faults[9]. Hard faults severely affect the performance of the circuit and are caused by open or short of the components at fault or the terminals at fault, in case of transistors[10]. Soft faults are parameter variations that are beyond an acceptable range and that which causes degradation of performance though not as severe as hard faults. In this work, only hard faults are introduced in the DAC since discusses that if a testing method can detect all the hard faults then it can also identify soft faults. The open faults are introduced by connecting a resistance of high value in series with the component at fault and short faults by connecting of low resistance in parallel to the component at fault. In case of transistor used as switches five types of faults are possible. They are:

(i) Source and Drain Short (SSD)
(ii) Source and Gate Short (SGS)
(iii) Drain and Gate Short (DGS)
(iv) Source Open (SOP)
(v) Drain Open (DOP)

The faults in resistors and transistors used as switches are introduced as shown in Figure 2, where RS is a resistor of high resistance and RP is a resistor of low value. The total number of hard faults that is possible in the circuit is = 2 X Number of Resistors + 5 X Number of Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs). Hence the total number of hard faults in DAC chip considered is 114. A careful analysis of the effect of faults in the DAC circuit reveals that certain fault classes collapse and the total number of detectable faults reduces. The faults introduced in the MOSFET legs used as Single Pole Double Throw (SPDT) switches are shown in Figure 3. Since the MOSFETS are used as switches their fault in operation is only reflected in the output according to the digital bit value in the leg. PMOS DGS and NMOS SGS introduce the same fault in the circuit as shown in

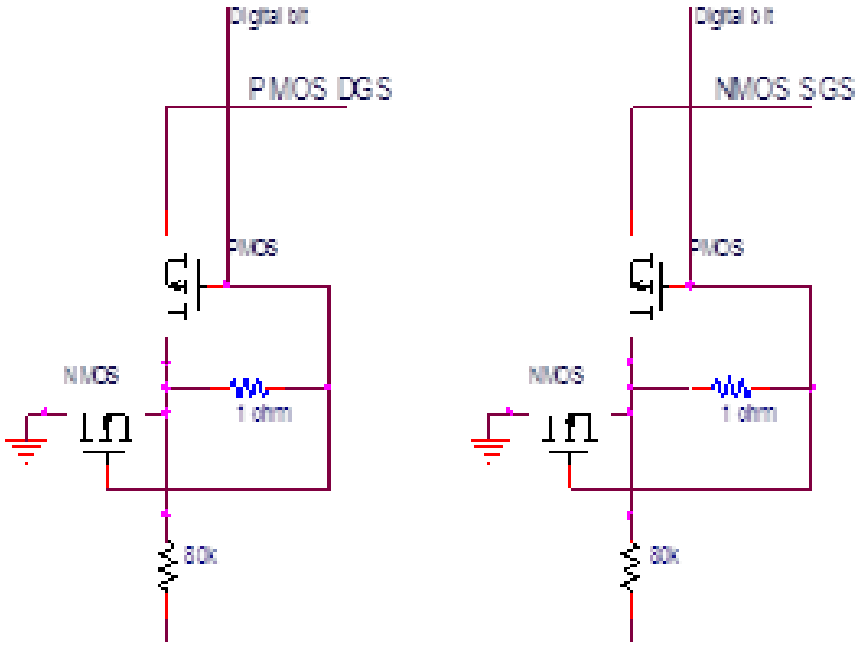

Figure 2. Faults in resistor and MOSFET.

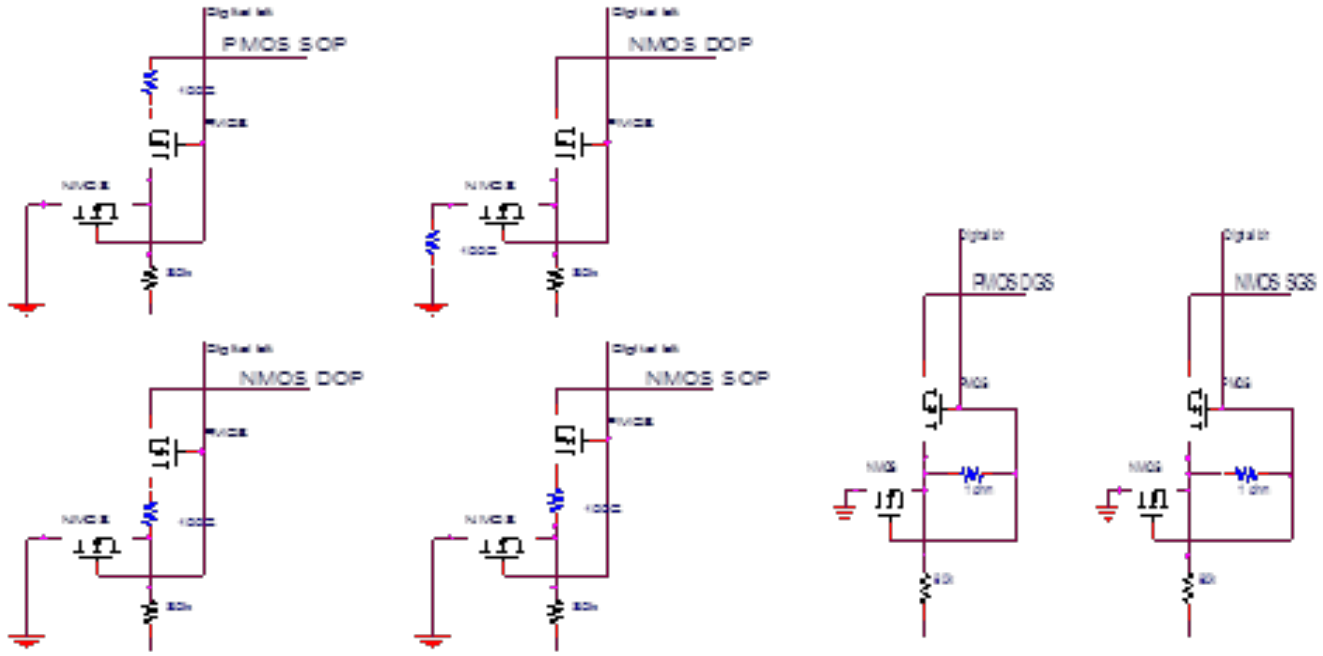

Figure 3. Open and short MOSFET faults.

Table 1. Total number of faults detected in DAC

MOSFETS (M1-M16)	Stuck-short	(2 x 16)+8 = 40
RESISTORS (R1-R17) & CAPACITOR C1	Stuck-open/short	(2 x 17) +1 = 35
Total number of faults		75

Figure 3. Total Number of Faults detected shown in Table 1.

4. Neural Network

This section provides a brief description of the neural networks that are used for fault classification in mixed signal circuit. Artificial neural networks can be effectively used as pattern classifiers. The networks used for classification are Feed Forward Networks (FFN) with Levenberg-Marquardt (LM) algorithm and Radial basis function networks.

5. Feed Forward Networks

Feed forward networks consists of an input layer with identity activation , one or more hidden layers with non-linear activation functions, and output layer which has linear activation function. The network is trained using Levenberg-Marquardt algorithm.

6. Levenberg Marquardt Algorithm

1. The weight values parameter lambda is initialised and Hessian matrix is calculated.
2. The next value of weight update is calculated and weight values are updated.
3. The error is evaluated and if the error has increased the value of lambda is increased by a factor 10 and the step is retracted. If the error has decreased then value of lambda is decreased by 10.
4. This process is repeated till a specified number of iterations or till specified value of error.

7. Radial Basis Function Networks

A powerful pattern classifier was presented by Bloomberg. The input data is initially clustered using k-means algorithm and the cluster centres are fixed. The layer of weights from the cluster layer to the output layer is trained using gradient algorithm. The cluster layer neurons have radial basis activation function.

8. Algorithm

1. Weight values are initialised. The cluster centres found using k-means are also initialised.
2. Each input data pattern is presented and the output of cluster layer is computed. This output is used for computing the weight change by multiplying the derivative of the error in the output neurons.
3. The weight values are updated and this process is repeated till convergence criterion is reached.

9. Neural Network Simulation

The data for the input binary word all zeros with all the faults irrespective of whether they affect the output with bit value zero is recorded and first network classifies the data into two classes, one class which has all the other faults and data of fault free operation and the other class which represents faults that prominently affect the output for input binary word all zeros. The second class in the first neural network is further classified into individual PMOS SDS faults using a third neural network. For data which belongs to the first class of the neural network their corresponding values for the input binary word all ones is used to train the network.

10. Experimental Results

The circuit is simulated and for each fault class 100 trails were performed by slightly varying the values of circuit components up to 5% of the original value. Parameters

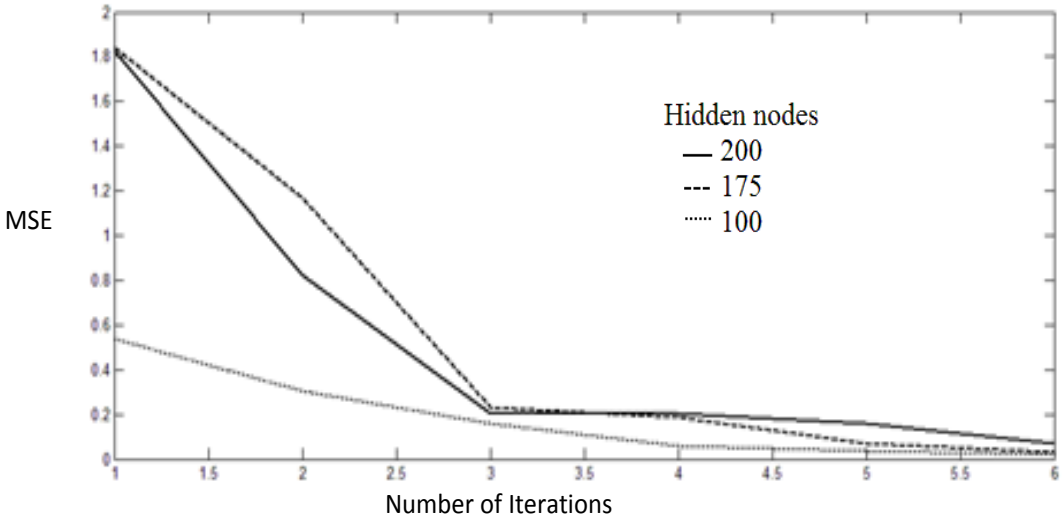

Figure 4. MSE vs number of iterations single layer FFN with LM.

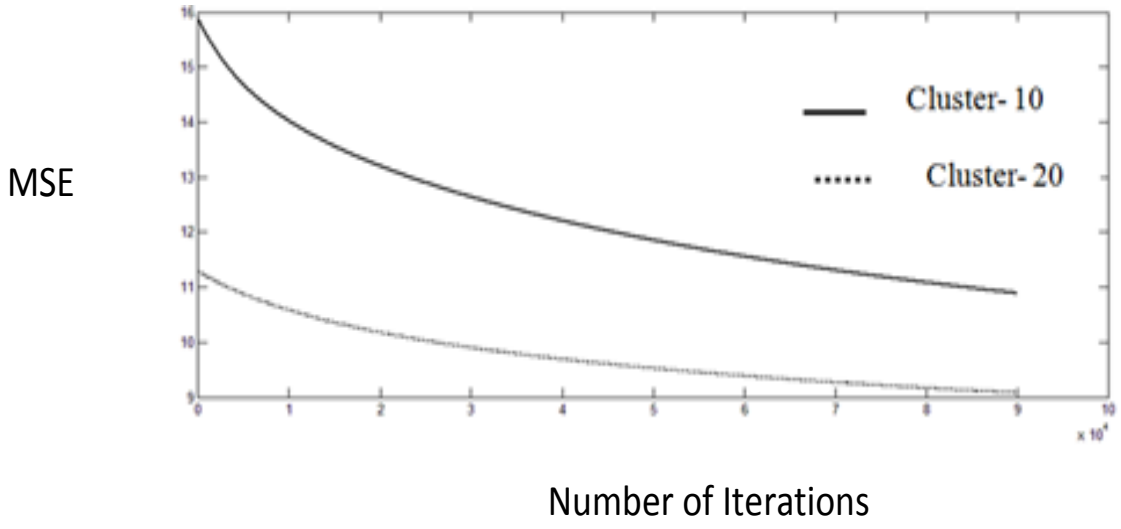

Figure 5. MSE vs number of iterations RBF network.

such as output voltage, Supply current and current flow in digital pins and input voltage to op-amp using suitable input binary words, all zeros or all ones are recorded. The data for different neural networks is segregated and normalized .80% of the data is used for training the network and the remaining data is used for testing. The networks used for classification are single and two layered FFN with LM algorithm and Radial Basis Function networks. The classification accuracy in all the five neural networks was 100%. The use of LM algorithm in training Feed forward network results in faster convergence of the network to specified value of mean squared error in lesser number of iteration. Single layer feed forward virtually requires no time for training except for the network which classifies the resistor faults. Figure 4 Shows MSE vs Number of iterations Single layer FFN with LM. The *Radial Basis Function* (RBF) network was trained by varying the number of clusters. The number of clusters for each class of data in neurons networks was fixed to 10 or 20. As the number of cluster was increased beyond 20 the learning rate had to be reduced to maintain the stability of the net hence the learning rate was reduced up till 0.0001. The classification accuracy above 98% was achieved in all five neural networks. Figure 5 Shows MSE vs Number of iterations RBF Network.

11. Conclusions

The test system considered for developing the fault detection algorithm is an 8 bit inverted R-2R ladder DAC. The faults in the DAC are introduced one at a time and the data was collected. The method by which faults are introduced in the resistors and MOSFETS, used as Single pole double throw switches, were discussed and their effects on the performance of the DAC are critically analysed. Based on this an artificial neural network methodology has been presented, in which data is handled by five neural networks (coded in MATLAB) to effectively identify and locate all possible faults which drastically affect the performance of the DAC chip. The results indicate the possibility of the use of artificial neural network as a fast, efficient, reliable test method for mixed signal circuits.

12. References

1. Airapetian AN, McDonald JF. Improved test set generation algorithm for combinational logic control. 9th Annual International Symposium on Fault-Tolerant Computing. 1979 Jun, p.133-136.
2. Koenemann B, Mucha J, Zwiehoff G. Built-in logic observation techniques. Proceedings, 1979 IEEE International Test Conference. 1979 Oct, p. 37-41.

3. Eichelberger EB, Williams TW. A logic Design structure for LSI testing. 25 Years of DAC Papers on Twenty-Five Years of Electronic Design Automation. 1997 Jun, p. 358-64.
4. Prithviraj K, Alok Barua, Sinhab S. Fault Diagnosis of Analog Integrated Circuits. Springer US. 2005.
5. New Approach of Test for DAC Using Fuzzy Neural Network. http://ieeexplore.ieee.org/document/4389584/. Date Accessed: 20/10/2007.
6. A Fault Diagnosis Expert System Base on Artificial Neural Network for Mixed-Signal Circuits. http://ieeexplore.ieee.org/document/4350992/. Date Accessed: 16/08/2007.
7. Viera Stopjaková, Pavol Maloˇsek, Marek Matej, Vladislav Nagy, Martin Margala. Defect Detection in Analog and Mixed Circuits by Neural network using wavelet analysis. IEEE Transactions on Reliability. 2005 Sep; 54(3):441-48.
8. Analog and Mixed- Signal Benchmark Circuits - First Release. http://ieeexplore.ieee.org/document/639612/. Date Accessed: 06/11/1997.
9. Nishant Govindrao Pandharpurkar, Ravi V. Design of BIST using Self-Checking Circuits for Multipliers. Indian Journal of Science and Technology. 2015 Aug; 8(19):1-7.
10. Beulah Hemalatha S, Vigneshwaran T, Jasmin M. Efficient Methodologies and Architectures of Network-on-Chip. Indian Journal of Science and Technology. 2016 Mar; 9(12):1-8.