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High Vt-low Leakage FDSOI Device for Ultra-low Power Operation

Manisha Guduri*, Amit Krishna Dwivedi, and Aminul Islam

Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi - 835215, Jharkhand, India; manishaguduri@bitmesra.ac.in, a.k.dwivedi@ieee.org, aminulislam@bitmesra.ac.in

Abstract

Objectives: The objective of this research paper is to design High Vt-Low Leakage FDSOI Device for Ultra-Low Power Operation. **Methods/Analysis:** This research work presents the modeling of fully depleted silicon on insulator (FDSOI) device with 350-nm gate length. This paper investigates threshold voltage (Vt) and leakage power of the different FDSOI devices in order to design high threshold voltage and low leakage device. **Findings:** It is observed that device5 shows higher Vt and dissipates lower leakage power when compared to that of other devices (devices1–4). The threshold voltage and subthreshold slope (SS) of device5 are observed to be 0.199 V (~0.2 V) and 80 mV/decade respectively. The leakage power of the device at drain voltage of 1 V is 41.9 nW. **Novelty /Improvement:** This kind of FDSOI device is a platform for designing circuits at nano scale regime for ultra-low power applications.

Keywords: FDSOI Device, Leakage Power, Threshold Voltage, Subthreshold Slope

1. Introduction

Due to side effects of aggressively scaled bulk-CMOS devices, SOI device gained attention of researchers. Even though the SOI technology first appeared in early 1980s, its gradual adoption began in late 1990s. Presently this technology is challenging bulk CMOS technology in almost all sectors of market like RF, analog, ultra-low power applications, photonics, MEMS, etc. According to the observation in[1], around 60% of mobile devices are made of SOI chips by the year 2012.

SOI devices are categorized as Partially Depleted (PD) or Fully Depleted (FD). Devices are called PD SOI MOSFET when the silicon film is thicker than the maximum gate depletion width (W_{dm}). PD SOI devices exhibit floating-body effect. Devices are called FD SOI MOSFET when the silicon film is so thin that the entire film is depleted before the threshold condition is reached[2]. Amongst SOI devices, FDSOI device is driving its direction towards suitability for ultralow power applications. The International Technology Roadmap for Semiconductors (ITRS) is projecting its adoption in IT industry especially in Internet Of Things (IoT) technology. ITRS identifies the extraordinary capability of FDSOI devices and refers these sorts of devices as advanced non-classical CMOS devices[3,4]. FDSOI devices are gaining more attention for their better scaling capability, endurable leakage current, reduced parasitic components, and higher performance[5–7]. Even though there are structural similarities of SOI and bulk MOSFET devices, still there are significant advantages like low parasitic capacitances, better resistance against short channel effects (SCE), no body effect, no latch up problem, and mainly improved subthreshold swing (subthreshold swing is inverse of subthreshold slope), etc. over the existing technology (bulk MOSFET devices)[8]. In this paper, we focus mainly on high threshold and low leakage of FDSOI device which is desirable for ultra-low power applications.

This paper is structured as follows. Section 2 provides modeling of FDSOI device. Design analysis of high V_t-low leakage device is presented in section 3. Finally, conclusions are drawn in section 4.

2. FDSOI Device Modelling

It is expected that downscaling of FDSOI device will be possible with consistency in the improvement in terms of

* *Author for correspondence*

ultra-low power consumption. This technology depends on an ultra-thin layer of silicon over a Buried Oxide layer (BOX)[9]. Transistors built in this way have ultra-thin body with many attractive device characteristics/attributes which are in demand as per current technology trends. Hence, FDSOI device finds its application in almost all electronic gadgets such as mobile internet devices (smart phones, netbooks, etc.), digital camera, camcorders, and so on[10]. Seeing the importance of FDSOI device technology and to propel the trending research in this direction, this work proposes an *n*-channel FDSOI device. In an *n*-channel FDSOI device, if a positive voltage is applied to gate terminal, then the entire *p*-type body is depleted and an *n*-type inversion channel is induced on the surface of the body. The thin body of the FDSOI device avoids the floating voltage. This enhances the device performance in terms of negligible leakage current by offering low leakage power. This makes FDSOI device a perfect choice for ultra-low power applications[11]. Figure 1 shows the basic FDSOI device structure with various interfaces and contacts. The device geometry as shown in Figure 2 has been considered for modeling various attributes of the proposed FDSOI device. Key device parameters and their specifications, utilized for modeling the proposed FDSOI device have been also reported in Table 1.

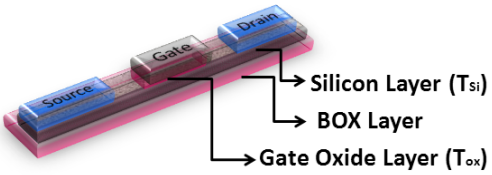

Figure 1. Structure of FDSOI device. The BOX layer is grown on substrate.

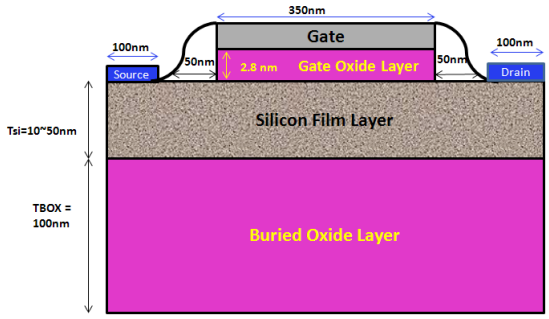

Figure 2. Proposed structure of Fully Depleted Silicon On Insulator (FDSOI) N-type device, which is modeled in this work. The Buried Oxide (BOX) layer is grown on p-type lightly doped substrate (not shown).

Table 1. Device parameters of FDSOI and its specifications

Parameter	Specifications
Channel doping concentration (N_A)	1~6e+18 cm^{-3}
S/D doping	1e+21 cm^{-3}
Buried oxide thickness (BOX)	100 nm
Silicon thickness (T_{Si})	10 ~ 50 nm
Gate Oxide Thickness	2.8 nm
Gate work function	4.5 eV
Gate length	350 nm
Gate voltage (V_G)	0.1 V to 1 V
Drain voltage (V_D)	0.1 V to 1 V
Substrate voltage	0 V

This work considers light channel doping concentration (N_A) ($1\times10^{+18}$ cm^{-3}) to avoid degrading of carrier mobility and the threshold voltage variations. The doping concentration of source/drain region is kept at $1\times10^{+21}$ cm^{-3}. Gate length of the FDSOI device has been kept equal to 350 nm. Silicon film thickness (T_{Si}) is varied from 10 nm to 50 nm and the buried oxide layer (BOX) thickness is kept equal to 100 nm. Further, to analyze the impact of T_{Si} on the device performance, five different device geometries (device1 with T_{Si} = 10 nm, device2 with T_{Si} = 20 nm, device3 with T_{Si} = 30 nm, device4 with T_{Si} = 40 nm and device5 with T_{Si} = 50 nm) have been considered in this work. Here, all these devices (device1-5) are n-channel devices. This works presents the study of various characteristics of the proposed FDSOI device, such as threshold voltage with respect to various doping concentration and leakage power, by modeling the devices (devices1-5) as discussed. The observations of our study are reported in the following sections.

3. Design Analysis

Investigation of threshold voltage (V_t) and leakage power is presented to report the proposed design of high V_t-low leakage FDSOI device. Threshold voltage and leakage power are essential design consideration which need to be addressed while

designing a device, mainly for low power applications[12]. This design also provides a platform for ultra-low power circuits with high V_t. This section presents a brief discussion on threshold voltage variation with respect to process parameter (channel doping concentration) variation. Further, leakage power analysis of different devices is also reported in this section.

3.1 Effect of Variation of Channel Doping Concentration on Threshold Voltage

In this section, FDSOI device is simulated using Atlas 2-D numerical simulator of Silvaco and Tony plot have been utilized for obtaining the reported results. In this paper, channel doping concentration is varied from 1e+18 to 6e+18 cm^{-3} and S/D doping concentration is maintained at 1e+21 cm^{-3}. Further, obtained I_D-V_G characteristics at drain bias of 0.1 V are explored to extract the threshold voltages of all the five devices. This work utilizes linear extrapolation method to extract the threshold voltage of the devices (devices1-5). In this method, the threshold voltage is extracted by calculating the maximum slope of the I_D-V_G curve and finding the intercept with the gate voltage (V_G at I_D=0) axis (x-axis) and then subtracting half of the applied drain bias (V_D/2). Initially, for the channel doping concentration of 1e+18 cm^{-3}, the threshold voltages of devices1-5 were found to be 0.02 V, 0.03 V, 0.07 V, 0.14 V and 0.199 V, respectively. However, with the variation of the channel doping concentration from 1e+18 cm^{-3} to 6e+18 cm^{-3}, the threshold voltages of the devices1-5 exhibit a change from the previous extracted threshold values. The new threshold values are found to be 0.52 V, 0.9 V, 1.218 V, 1.34 V, and 1.489 V, respectively. The variations found in the extracted threshold voltages for various channel doping concentrations are plotted in Figure 3. As can be seen, threshold voltage increases with the increase in channel doping concentration (N_A) demonstrating a linear dependence of threshold on the channel doping concentration. This is quite reasonable because increase in channel doping, increases Fermi potential and channel depletion charge and more effort is required to deplete the whole channel. This can be also verified from the device's model equations utilized in this work.

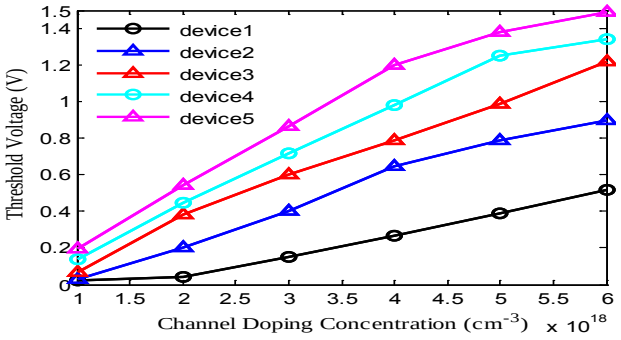

Figure 3. Channel doping concentration versus threshold voltage for different FDSOI (NMOS) devices. Threshold voltage shows almost linear dependence on channel

Analytical model of threshold voltage (V_t) for FDSOI MOSFET is given as [12].

$$V_t = V_{FB} + 2\phi_B - \frac{Q_B}{2C_{OX}} - \left(V_{BG} - 2\phi_B + \frac{Q_B}{2C_{BOX}}\right)\frac{C_{Si}\times C_{BOX}}{C_{OX}\left(C_{Si}+C_{BOX}\right)} \quad (1)$$

where, $Q_B = -qN_A T_{Si}$, V_{FB} and V_{BG} are flat band and back gate voltages, C_{OX}, C_{BOX} and C_{Si} are capacitances of oxide layer, buried oxide layer and silicon film layer. Q_B is area charge density in the depleted silicon film, ϕ_B is work function. Since the capacitance of silicon film layer is very large than that of buried oxide layer i.e. $C_{Si} >> C_{BOX}$, following approximation can be made:

$$\frac{C_{Si}\times C_{BOX}}{C_{OX}\left(C_{Si}+C_{BOX}\right)} \cong \frac{C_{BOX}}{C_{OX}} \quad (2)$$

The device threshold model (3) can be obtained by substituting (2) in (1) as

$$V_t = V_{FB} + 2\phi_B - \left(V_{BG} - 2\phi_B\right)\frac{C_{BOX}}{C_{OX}} + \frac{qN_A T_{Si}}{C_{OX}} \quad (3)$$

From (3) we observe that there is a linear dependence of threshold voltage on silicon film thickness with the slope proportional to channel doping concentration for a FDSOI MOSFET. However, the threshold voltage dependence on silicon film thickness is not observed when the silicon film thickness is greater than maximum depletion region width (X_{DMAX}), where X_{DMAX} is given by

$$X_{DMAX} = \sqrt{\frac{4\varepsilon_{si}\phi_B}{qN_A}} \quad (4)$$

In this case, if $T_{Si} > X_{DMAX}$, then the device is not considered as fully depleted (FD) SOI MOSFET.

Apart from the threshold voltage variations with the channel doping concentrations, variations in the threshold voltage due to variations in the silicon film thickness (T_{si}) of the devices (devices1-5) can be observed from Figure 3. It can be seen that as silicon film thickness increases, the threshold voltage also increases. There is a linear dependence of threshold voltage on the silicon film thickness (T_{si}) of the devices (devices1-5) which follow the relationship as stated in the device threshold model given by (3). The results in this work also closely matches with the existing model of threshold voltage[13].

Further, this work also analyzes the variations in the threshold voltages of the devices for both linear and saturation regions of operation. For this analysis, the

channel doping concentration (NA) and S/D doping concentration are kept equal to 1e+18 cm-3 and 1e+21 cm-3, respectively and drain bias is varied for the different region of operation. Linear threshold voltage ($V_{t,lin}$) and saturation threshold voltage ($V_{t,sat}$) of devices1-5 are extracted for the given conditions and tabulated in Table 2. The $V_{t,lin}$ is extracted with drain bias set to 50 mV (i.e., VDS = 50 mV) and $V_{t,sat}$ is extracted with drain bias set to V_{DD} (i.e., V_{DS} = 1 V), while keeping all other conditions same. It can be observed from the tabulated values that the threshold voltage is significantly reduced with the increase in V_{DS}. This is because of the short channel effects such as drain-induced barrier lowering (DIBL)[14].

Table 2. Linear and saturation threshold voltages of devices 1-5

Device	$V_{t,lin}$(V) (@ V_{DS}=V_{DD}=50 mV)	$V_{t,sat}$(V) (@ V_{DS}=V_{DD}=1 V)
Device1	0.25	0.025
Device2	0.34	0.032
Device3	0.41	0.077
Device4	0.47	0.11
Device5	0.53	0.15

3.2 Leakage Power Analysis of Different FDSOI Devices

As leakage power is a critical design metrics for ultra-low power application, leakage power analysis of all the devices (devices1-5) is also reported in this work. Total power consumption is sum of dynamic power consumption and leakage power consumption. Leakage power has direct impact on total power consumption of a circuit. As leakage power is reduced, total power also reduces. This reduction in total power consumption makes the device suitable for ultra-low power operation. Mathematically leakage power can be expressed as

$$P_{Leakage} = I_{OFF} \times V_{DS} \quad (5)$$

where, I_{OFF} is the leakage current of the device and V_{DS} is the drain-to-source voltage[15]. Table 3 reports leakage power of the devices1-5 for various supply voltages (V_{DD}) ranging from 0.05 V to 1 V. Figure 4 shows the comparison of leakage power of devices1-5 @ V_{DS} = V_{DD} = 1 V. It can be observed for the same Figure that the device5 (with T_{Si}=50 nm) dissipates lesser leakage power compared to other four devices. Thicker the silicon film lower is the leakage current[16]. Therefore, device 5 is the most suitable for ultralow power applications Figure 5 shows I_D-V_D characteristics at gate voltages of 0.2 V, 0.3 V, 0.4 V and 0.5 V of High V_t-Low leakages FDSOI Device (device5).

Table 3. Leakage power of devices 1-5 versus drain voltages

V_{DD} (V)	Leakage power device1 (μW)	Leakage power device2 (μW)	Leakage power device3 (nW)	Leakage power device4 (nW)	Leakage power device5 (nW)
0.05	0.158	0.0264	3.45	0.669	0.146
0.1	0.452	0.0706	9.22	1.83	0.403
0.2	1.14	0.179	24.1	4.90	1.03
0.3	1.9	0.310	43.8	9.09	1.86
0.4	2.71	0.462	68.7	14.4	2.84
0.45	3.13	0.544	99.0	20.5	4.04
0.5	3.56	0.630	134	23.8	5.51
0.6	4.43	0.807	170	27.5	7.79
0.7	5.32	1.01	305	35.9	13.7
0.8	6.36	1.26	480	69.2	21.7
0.9	7.23	1.55	634	106	30.6
1	8.11	1.94	634	150	41.9

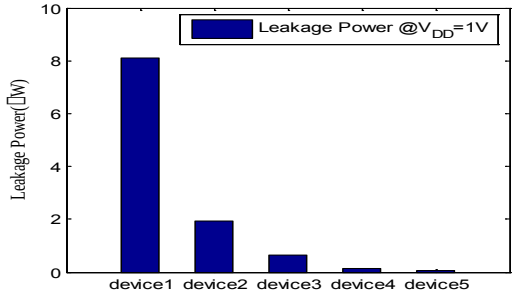

Figure 4. Leakage power of different devices at drain voltage V_{DS} = V_{DD}= 1 V.

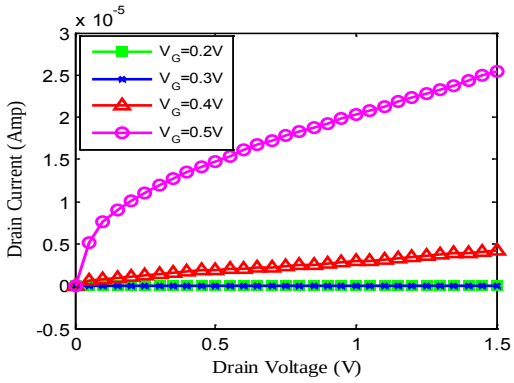

Figure 5. I_D-V_D characteristics at gate voltages of 0.2 V, 0.3 V, 0.4 V and 0.5 V of High Vt-Low leakage FDSOI Device (device 5).

4. Conclusion

In this paper, an FDSOI device with gate length of 350 nm is modeled in sub micrometer regime. By varying channel doping concentration of different devices, threshold voltage is noted. Selecting proper threshold voltage is an important device design target in achieving ultra-low power consumption. Leakage power analysis of different devices is performed and a comparative plot is shown. This work concludes by choosing device5 for ultralow power operation. Device5 is the attractive choice for ultralow power operation because it dissipates lesser leakage power when compared to other devices.

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