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A Power-Efficient Multiplexer using Reversible Logic

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Abstract

The basic concept of reversible circuits is to save energy dissipation in the form of both power and heat in lieu of some additional circuitry. Its use leads to compensating for the garbage bits that will be necessarily generated. Designing a multiplexer can prove to be a very useful block in many complex circuits. A Fredkin gate based multiplexer has been proposed for 180nm, 90nm and 45nm channel lengths. The designed circuit is expected to be fault-tolerant. The W/L ratio has been varied to find the least possible value of power dissipation of the circuit. Substrate-bias voltage of MOSFET can be varied in order to change the threshold voltage value of transistor which helps us in finding the optimum values of driving voltage, input voltage and substrate to bias voltage. Its use is most prominent in an inverter block where tenfold decrease is observed in bulk-driven supply compared to conventional CMOS technology. The value of the bias voltage is found out to be increasing for decreasing channel lengths but bulk-driven voltage supply is not useful in 45nm technology because of increase in transconductance owing to its fixed minimum (W/L) ratio. Delay and power-delay product are also important parameters that have been taken into account. Other important figures of merit like quantum cost, number of garbage outputs, number of gates and quantum depth have also been studied. All the simulations have been done on Cadence tool.

Keywords: Bulk-Driven Technology, Garbage Bits, Power-Delay Product, Quantum Gates, Quantum Cost, Reversible Logic

1. Introduction

Reversible logic has a property that synthesis techniques are applicable for reversible logic in typical, forward method, where output signals are functions of input signals, and in a reverse method, where input signals are functions of output signals. It implies that we can achieve the inverse function for back-tracing by inverting the K-map for the output function and using it as a function to get inputs back from the output[1]. Reversible circuits work on the principle of charge recovery[2]. This leads to considerable saving of power as it makes use of switching nodes whenever a transition has to be made from low to high or vice versa instead of adding separate nodes for fulfilling the requirement. The number of inputs and outputs in the circuit are always kept equal in order to avoid the resistive losses[3]. Undoubtedly, the leakage power losses are one of the most critical problems currently being faced in nanometer scale CMOS technology[4].

Traditional reversible logic gates operate on binary digits or bits. Quantum gates act upon quantum bits or qubits. A single unit of quantum information is called a qubit. Some quantum gates like Feynman gate and both the universal logic gates, namely Fredkin gate and Toffoli gate have their counterparts defined in reversible logic circuits also. The fanout of any reversible logic gate is always limited to one. This only means that each output of a reversible logic gate is allowed to drive only one input of another gate. The standard figures of merit for quantum gates are quantum cost, weighted number of gates, number of constant inputs, garbage outputs and delay[5].

Quantum cost is the quintessential factor in the synthesis of any reversible logic gates. It is determined in terms of the number of basic components used in implementing the gate. The basic components are those which have unity quantum cost like V, V_+ and CNOT gates. The total number of these three gates used in the circuit is called the quantum cost of the circuit. The number of garbage bits produced and the number of constant inputs in the circuit are to be minimised. The garbage bits are produced in a circuit in order to realize unbalanced functions. The heat dissipated due to the production of

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garbage bits is a major issue[6]. Without any constant inputs in a circuit, a reversible circuit only realizes balanced functions at the outputs[7]. The inputs to be kept constant vary with the functionality required to be achieved by a circuit. Different functions can be performed by any gate depending on the input value kept constant.

Multiplexers are the most widely used logic device in almost all the computational circuits. Data selection through various combinations of select line inputs is the basic feature of a multiplexer. They work as Data Selectors, as multiplexer selects one of the given input for the output according to the input chosen as select line. There is a great need for the availability of devices that can perform multiple operations. The need of saving energy on a circuit, especially on a unit that is used several times in a circuit is indispensable. It is an irreplaceable component in communication systems also. A multiplexer and a demultiplexer is a compulsory component in every communication circuit at all the levels. The conventional Fredkin gate itself behaves as a 2:1 multiplexer. The first input works as the select line to choose the output between the second and third inputs. The inherent parity-preserving property of Fredkin gate makes it fault tolerant which eliminates the chances of any non-concurrence in the outputs for a given set of inputs[8].

2. Fredkin Gate

The classical logic for this gate suggests that it is just a flipped multiplexer with a control input A that decides the output. It was introduced by Ed Fredkin and Tomasso Toffoli in 1982. Before describing the quantum circuit for Fredkin gate, it is necessary to first discuss the building blocks of this gate, namely V, V_+ and CNOT gates.

The controlled NOT(CNOT) gate is a 2×2 gate with quantum cost one. The quantum cost of 1×1 reversible gates is zero. The V gate is the square root of NOT gate and V_+ is its Hermitian[9]. The quantum implementation of CNOT gate is as shown in figure 1. The properties of V and V_+ quantum gates are described in the following equations:

$$V \times V = NOT \quad (1)$$

$$V \times V_+ = V_+ \times V = I \quad (2)$$

$$V_+ \times V_+ = NOT \quad (3)$$

The Feynman gate is a 3×3 conservative reversible gate. Each dotted rectangle behaves as a Feynman gate whose quantum cost is 1. So, the overall quantum cost for a Fredkin gate comes out to be 5 which is the sum of 2 dotted rectangles, 1 V gate and 2 CNOT gates. The quantum implementation of Fredkin gate is as shown in figure 2.

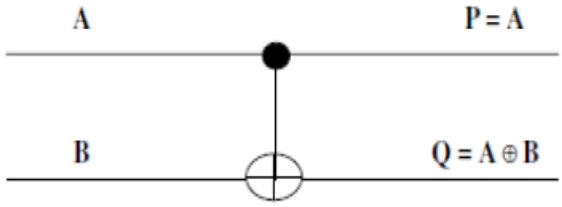

Figure 1. CNOT gate quantum Implementation, Pannu.

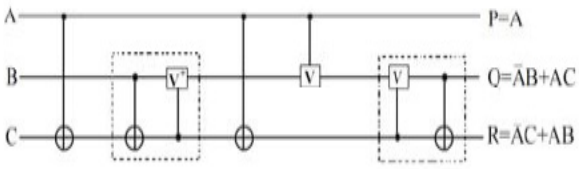

Figure 2. Quantum implementation of Fredkin gate, Pannu.

The parity-checking feature of this gate is particularly very useful in error detection because most of the arithmetic operations do not preserve the parity. It can be used to detect permanent as well as transient faults[10]. It is fully efficient in detection of single faults, although it may be difficult to detect multiple faults. Also, it gets us minimum circuit complexity as the need to insert an error detector circuit separately decreases. In this way, we get a parity preserving 2:1 multiplexer with the help of only one gate which makes it fault tolerant as the error detection at every stage need not be done.

The number of constant inputs used in each circuit is zero. This is due to the fact that the smallest block used here is itself a 2:1 multiplexer using which higher level circuits are synthesized. This eliminates the need to keep any of the inputs constant as the number of inputs at the first stage is exactly equal to those required in a 2:1 multiplexer.

The Average power dissipation in the circuit is determined as:

$$P_{avg} = C V_{DD}^2 f_{CLK}$$

where, P_{avg} =Average power dissipation, C=Load capacitance, f_{CLK} =clock frequency, V_{DD}=supply voltage.

3. Bulk-Driven Voltage Supply

Threshold voltage is a major factor to be reduced in any MOSFET circuit. There are various methods through

which that can be attained but mostly, we need to change the device characteristics for that. It is either by introducing an impurity while fabrication of the transistor or by varying the substrate bias voltage. This has to be done by making use of the relation between the gate to source voltage, bulk voltage applied and the threshold voltage. The presence of bulk node provides the designer an extra degree of freedom in the transistor design process. By applying a voltage between substrate and source, depletion width is increased. It leads to decrease in power dissipation of the circuit. The fundamental equation describing the relationship between the change in threshold voltage and the bias voltage is given as:

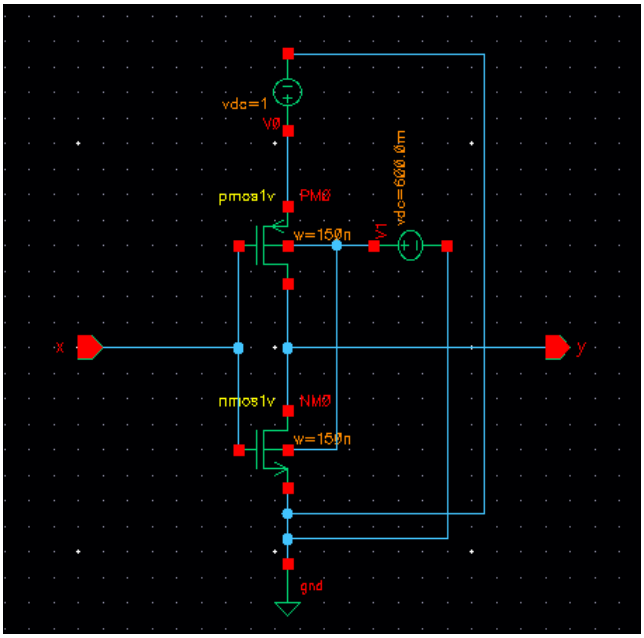

Figure 3. Schematic of inverter with bulk driven substrate with x denoting the input pin and y denoting the output pin.

$$\Delta V_T = \sqrt{(2\epsilon_s q N_a)}\ [(2\phi_F - V_B)^{1/2} - (2\phi_F)^{1/2}]\ /C_i$$

where, ϕ_F depends on the substrate doping; C_i depends on the thickness and dielectric constant of the insulator; V_B is the substrate bias voltage; N_a is the substrate doping. But this method cannot be used on large scale because, if used multiple times in a circuit, the applied bulk voltage can itself be responsible for increasing the overall power dissipation of the circuit. The application of an additional voltage source leads to a definite increase in the overall power dissipation of the circuit. So, it has been used only in the basic inverter circuit in this paper which has significantly contributed to reducing the power dissipation of the circuit. Various values of substrate bias voltages have been studied and the optimum value is chosen for different channel lengths. The criteria for optimisation are the power dissipation in the circuit as well as avoiding the occurrence of glitches in the output waveform. The use of bulk-driven technology also leads to decrease in the transconductance of the transistor[11]. This low transconductance makes the circuit useful in biomedical applications. But in 45nm technology, the application of bulk-driven supply does not contribute to reduction in power dissipation. The increase in transconductance value of the circuit due to higher (W/L) ratio than other technologies is as per the following equation in saturation region:

$$g = \mu_n C_{ox}(W/L)(V_{GS}-V_T)$$

where, g denotes transconductance; C_{ox} denotes the oxidation capacitance; (W/L) denotes the aspect ratio; V_{GS} denotes the gate to source voltage and V_T denotes the threshold voltage.

4. Inverter Circuit Design using Substrate Bias Voltage Variation

The typical CMOS inverter implementation shows considerable decrease in power dissipation when provided with a suitable value of direct supply of bulk voltage as shown in figure 3.

The outputs obtained in the conventional implementation and the application of bulk voltage is shown with the help of figure 4(a) and figure 4(b) respectively.

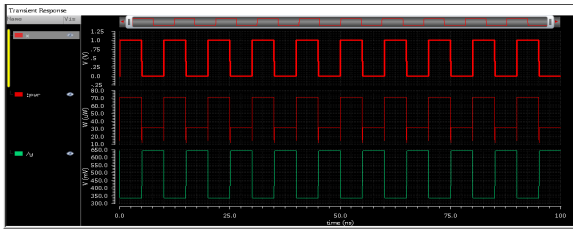

Figure 4(a). Output of a conventional inverter showing average power dissipation of 51.3 µ.

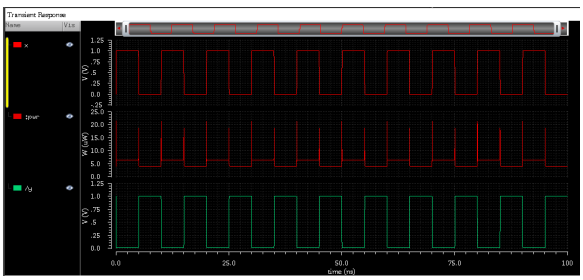

Figure 4(b). Output of a bulk driven inverter showing lesser average power dissipation of 5.2 µW.

The figures have the power dissipation average labelled on them and it is clear that there is about tenfold decrease in the value.

The functionality of Fredkin gate can be described with the help of the figure 5.

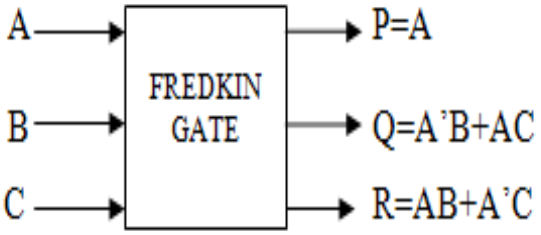

Figure 5. Block Diagram of Fredkin Gate.

The inverter with bulk-driven technology is used in the implementation of Fredkin gate. The schematic drawn for the CMOS implementation of Fredkin gate and the output waveform verifying its functionality as well as showing power dissipation are shown in figure 6 and figure 7, respectively.

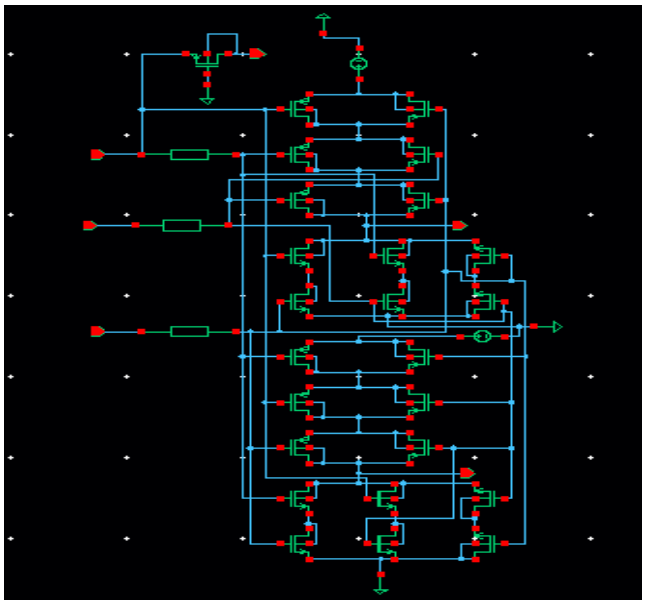

Figure 6. Schematic of CMOS implementation of Fredkin gate.

Illustration: The pins connected from the side of their pointed terminal are the input pins and the pins connected from the plain side are the output terminals.

The functionality of the Fredkin gate makes it quite clear that it behaves as a multiplexer in itself. The output bit obtained same as in the input is not considered as a garbage value[12]. This implies that the first output obtained is not a wasted one. The second terminal provides the multiplexer output and the third terminal gives the output in case we exchange the inputs B and C in the circuit.

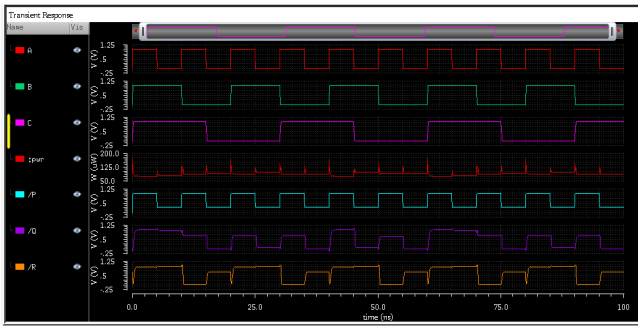

Figure 7. Output waveforms for Fredkin gate in 180nm technology with average power dissipation of 89.3 µW.

5. Implementation of Multiplexer

The Fredkin gate implemented above gives the output exactly same as that of a 2:1 multiplexer[13]. This implies that if the first input of the Fredkin gate is used as a select line, then we can use this gate as a multiplexer itself. This serves as the block to implement a 4:1 multiplexer. Similarly, the 4:1 and 2:1 multiplexers are collectively used to implement an 8:1 multiplexer. The schematic for the 4:1 multiplexer as well as its output waveform verifying functionality as well as showing power dissipation in 180 nm technology are shown in figure 8 and figure 9, respectively.

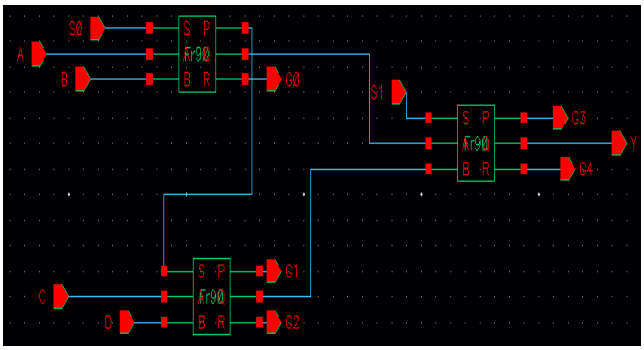

Figure 8. Schematic of 4:1 Multiplexer.

Illustration: $G_0 = S_0'B + S_0A$;

$G_1 = S_0$;

$G_2 = S_0'D + SC$;

$G_3 = S_1$;

$G_4 = S_1(S_0'A + S_0B) + S_1'(S_0'C + S_0D)$;

$$Y = S_1'(S_0'A + S_0B) + S_1(S_0'C + S_0D) .$$

In the similar way, the schematic for an 8:1 multiplexer as well as its output waveform verifying functionality as well as showing power dissipation in 180 nm technology are shown in figure 10 and figure 11, respectively.

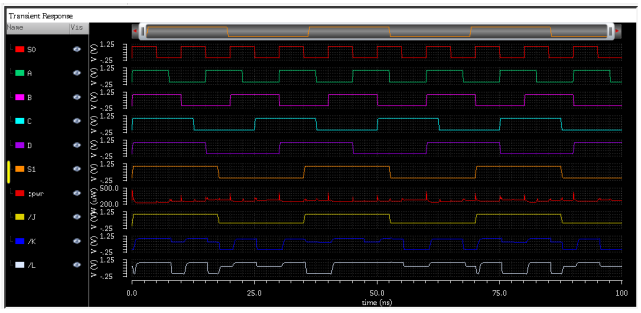

Figure 9. Output Waveform and Power Dissipation in 180 nm technology.

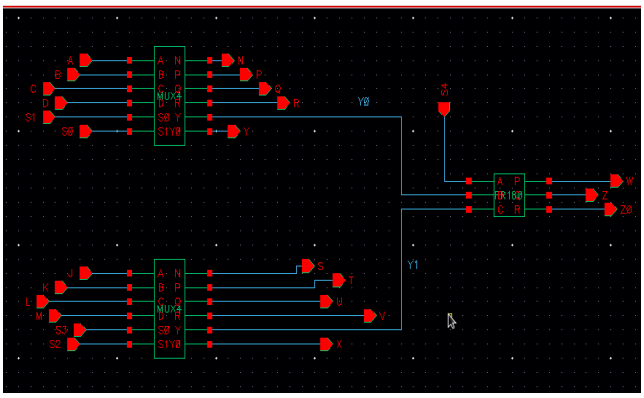

Figure 10. Schematic of 8:1 Multiplexer.

Illustration: The figure makes use of two 4:1 multiplexers and a 2:1 multiplexer. The outputs Y_0 and Y_1 are provided as input to 2:1 multiplexer. The values obtained are represented in the form of Boolean expression as follows:

$$Y_0 = S_1'(S_0'A + S_0B) + S_1(S_0'C + S_0D) ;$$

$$Y_1 = S_3'(S_2'A + S_2B) + S_3(S_2'C + S_2D) ;$$

$$W = S_4 ;$$

$$Z = S_4'Y_0 + S_4Y_1 ;$$

$$Z_0 = S_4Y_0 + S_4'Y_1 .$$

6. Calculation of Delay at 10 MHz Frequency

The maximum total time taken in a circuit to derive any output from the input at highest frequency is called the delay of the circuit. It directly affects the speed of the circuit and hence, this parameter is calculated with a standard simulation time of 100ns. With the increase in frequency, the power dissipation across MOSFETs increases too. The variation of delay with the change in threshold voltage can be studied by varying the substrate bias dc voltage supply and the same is shown in table 1.

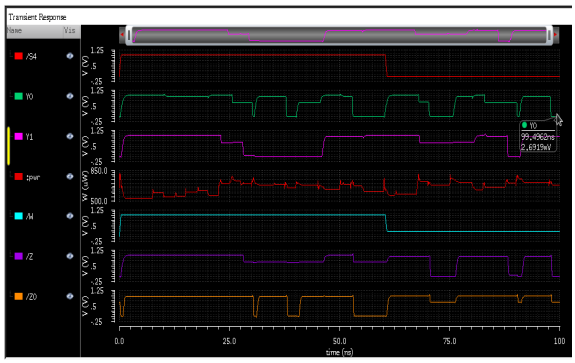

Figure 11. Output Waveform for an 8:1 Multiplexer.

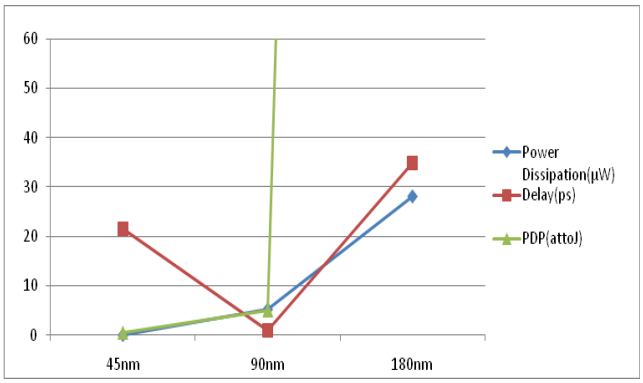

Figure 11. Comparison of various parameters with different channel length in inverter.

7. Importance of the Power Delay Product

In most cases, there is always a trade-off between speed and average power dissipation. So, instead of comparing the parameters separately, the product of power dissipation and the delay in the circuit known as the Power-Delay Product provides us a better estimate of the circuit efficiency. It represents the average energy dissipated for a single switching event[14]. For higher level circuits, the power delay product will be minimum for lesser channel lengths as can be predicted from the results obtained.

8. Results

For n=1, No. of gates = 1 = 2^n-1

Table 1. Comparison of power dissipation in elements with varying W/L ratio at driving voltage= 1 V dc supply and input voltage as 1 V square wave pulse

Channel Length, L	Optimum channel width, W	(W/L) ratio	Element	Delay (seconds)	Bulk Voltage	Power Dissipation	Power Delay Product(PDP)
180 nm	400nm	2.22	Inverter	34.8×10^{-12}	0.4 V	28 μW	9.74×10^{-16}
			Fredkin Gate	53×10^{-12}	0.4 V	89.3 μW	47.3×10^{-16}
			4:1 MUX	220×10^{-12}	0.4V	0.26 mW	5.72×10^{-14}
			8:1 MUX	233×10^{-12}	0.4 V	2.45 mW	5.7×10^{-13}
90 nm	150nm	1.66	Inverter	951×10^{-15}	0 V	51.3 μW	4.8×10^{-17}
			Inverter	949.2×10^{-15}	0.6 V	5.2 μW	4.94×10^{-18}
			Fredkin Gate	181.6×10^{-12}	0.6 V	24.2 μW	4.4×10^{-15}
			4:1 MUX	366.8×10^{-12}	0.6 V	76.6 μW	2.8×10^{-14}
			8:1 MUX	338.3×10^{-12}	0.6 V	179.4 μW	6×10^{-14}
45 nm	120nm	2.66	Inverter	21.54×10^{-12}	--	19 nW	4×10^{-19}
			Fredkin Gate	214.6×10^{-12}	--	1.8 μW	3.86×10^{-16}
			4:1 MUX	411×10^{-12}	--	5.75 μW	2.36×10^{-15}
			8:1 MUX	743.2×10^{-12}	--	9.72 μW	7.22×10^{-15}

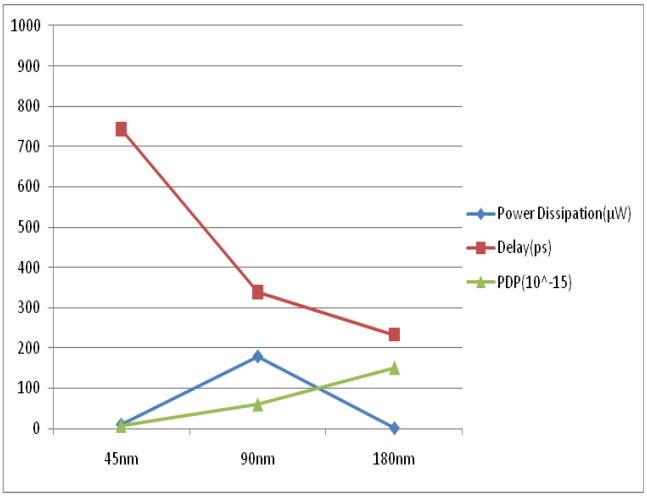

Figure 12. Comparison of various parameters with different channel length in 8:1 multiplexer.

No. of constant inputs = 0
Garbage outputs = 1
QC = 5

For n=2, No. of gates = 3 = 2^n-1
No. of constant inputs = 0
Garbage outputs = 3
QC = 15

For n=3, No. of gates = 7 = 2^n-1
No. of constant inputs = 0
Garbage outputs = 7
QC = 35

For n=N, No. Of gates = 1 = 2^n -1

A graph comparing various parameters with different channel length in an inverter circuit and an 8:1 multiplexer are shown in figure 11 and figure 12 respectively.

In 45 nm technology, the channel width cannot be reduced to more than 120nm. Thus, the use of bulk-driven technology increases the transconductance of the circuit because the W/L ratio cannot be reduced.

9. Conclusion

Decrease in channel length leads to saving of power. The results also show that the power dissipation in all the circuits in 45nm technology is least compared to 90nm and 180nm technologies. A particular width has to be found out for which the power saving is maximum. By varying the value of (W/L), we can minimise the power dissipation value. Also, an optimum value of bulk supply provided at the substrate terminal is favourable in reducing power losses. Generally, the driving voltage and input pulse magnitude are kept equal for getting the best out-

put with maximum energy saving. The inapplicability of bulk-driven voltage supply at the substrate terminal of a MOSFET in 45nm technology is because of the fixed minimum value of the (W/L) ratio. This fixed value also increases the transconductance value. The final Power-Delay product obtained for the circuit is minimum for the least channel length.

10. References

1. Abbasalizadeh S, Forouzandeh B, Aghababa H. 4 Bit Comparator Design based on Reversible Logic Gates. Lecture Notes on Information Theory. 2013 Sep; 1(3):1–3.
2. Kamaraj A, Marichamy P, Karthika DS, Nagalakshmi SN. Design and Implementation of Adders using Novel Reversible Gates in Quantum Cellular Automata. Indian Journal of Science and Technology. 2016 Feb; 9(8):1–7.
3. Gopal L, Raj N, Tham NTC, Gopalai AA, Singh AA. Design of Reversible Multiplexer/De-multiplexer. 2014 IEEE International Conference on Control System, Computing and Engineering, Penang, Malaysia. 2014 Nov.
4. Woong CJ, Roger CY. Transistor and pin reordering for leakage reduction in CMOS circuits. Microelectronics Journal (ELSEVIER). 2016; 53:25–34.
5. Mamataj S, Das B, Rahaman A. Realization of different multiplexers by using COG reversible gate. International Journal of Electronics and Electrical Engineering. 2015 Oct; 3(5):1–7.
6. Rup PN, Neha P. Generalised Approaches for ALU Design using Reversible Gates. International Journal of Computer Science and Information Technologies. 2015; 6(6):1–3.
7. Perkowski M, Jozwiak L, Kerntopf P, Mishchenko A, Al-Rabadi A. A General Decomposition for Reversible Logic. Portland University Annual Conference, 2001.
8. Noor MSK, Kamakoti V. Constructing Online Testable Circuits using Reversible Logic. IEEE Transactions on Instrumentation and Measurement. 2010 Jan; 59(1):101–09.
9. Syamala Y, Tilak AVN. Synthesis of Multiplexer and Demultiplexer Circuits using Reversible Logic. International Journal of Recent Trends in Engineering and Technology. 2010 Nov; 4(3):1–5.
10. Moumita M, Prasun G, Bishwaruup G. Design of low power fault tolerant reversible multiplexer using QCA. Third International Conference on Emerging Applications of Information Technology, IEEE. 2012.
11. Ramiro T, Marco L, Domenico A. Ultra-Low-Voltage Self-Body Biasing Scheme and its applications to Basic Arithmetic Circuits. VLSI Design. 2015.
12. Mohammadi M, Eshghi M. On figures of merit in reversible and quantum logic designs. Springer Science and Business Media, LLC. 2009.
13. Vandana S, Singh OP, Mishra GR, Tiwari RK. An Optimized Circuit of 8:1 Multiplexer using Reversible Logic Gates. International Conference on Communication, Computing and Information Technology. 2014.
14. Amaury N, Helmut S, Thomas L, Denis F. Power-Delay Product Minimization in High-Performance 64-bit Carry-Select Adders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2004 Mar; 12(3):235–44.