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Design of Dynamically Reconfigurable Input/Output Peripheral based Wireless System

B. Murali Krishna[1], G. L. Madhumati[2] and Habibulla Khan[1]

[1]Department of ECE, K L University, Vaddeswaram, Guntur – 522502, Andhra Pradesh, India; muralikrishna@kluniversity.in, habibulla@kluniversity.in
[2]Department of ECE, Dhanekula Institute of Engineering and Technology, Vijayawada – 521139, Andhra Pradesh India; madhumati70@rediffmail.com

Abstract

Background: Field Programmable Gate Arrays (FPGAs) are unlimited by applications, but fortunately limited with area. FPGAs can be integrated to various fields like system-on-chip, communication, cryptography, signal and image processing etc. **Methods**: The main purpose of this research paper is to implement multiple applications on FPGA by interfacing with various peripherals like Universal Asynchronous Receiver Transmitter (UART), General-Purpose Input/Output (GPIO) and Digital Video Interface (DVI) - Video Graphics Array (VGA) using Partial Reconfiguration (PR). **Findings:** The UART peripheral is used for dual purposes. First purpose is to switch the applications dynamically using PR, and second purpose serves a, design of *N*-bit adder and subtractor applications in serial communication, GPIO's are used to design various *Linear Feedback Shift Register* (LFSR) techniques which are applicable in cryptography system which generates random keys encrypted with message produces cipher can encrypt and decrypt data in wireless with ZigBee peripheral devices, and LFSR is used in Built-In-Self-Test to generate test patterns for a digital system under test. Digital Video Interface peripheral is used to design ZigBee based wireless video game. A comparative analysis is performed among spartan, virtex5 and virtex6 architectures. It has been observed that virtex6 architecture consumes fewer resources in comparison to Spartan and virtex5. Moreover, a wireless remote control is designed using ZigBee to provide the gaming control to the user. **Conclusion:** Applications implemented using various peripherals can be switched dynamically with loading partially configured bit streams in CF card to FPGA by providing commands in serial communication through MicroBlaze Processor.

Keywords: DVI, FPGA, GPIO's and ZigBee, Partial Reconfiguration, UART

1. Introduction

Significance of reconfigurable silicon technology has changed the electronic industry to design, simulate and implement custom hardware functionality with time to market. FPGAs use reprogrammable semiconductor *Static Random-Access Memory* (SRAM) based technology. SRAM is a volatile type of memory, its contents are erased when the power is switched off. FPGAs offer the flexibility features like high performance, low power consumption, less time to market, less expensive and compact design. Using libraries of more complex function soft macros (IP Cores like Adders, RAM, and ROM) further simplify the design process by optimizing delay, power and area1. Tremendous growth in wireless communication has enabled the researchers to use wireless portable personal devices such as mobile, Wi-Fi, (ESP8266-IOT) Bluetooth, Global System for Mobile communication (GSM), General Packet Radio Service (GPRS), data card and wireless sensor networks to append with custom applications. Communication is the process of transferring information from one point to other point either by wireless or wired communication. In these two types of communication, wireless communication has proved to be more popular. Among different wireless technologies, ZigBee technology stands on the top as it is able to

*Author for correspondence

provide short range communication between devices and users in a simple and efficient manner2. There are many types of ZigBee devices that are being used in home and industrial appliances. These modules are based on several specifications like range, power consumption, cost and operations which they perform that are related to it. One of its specifications is that, they work within a range of Miles of distance and will operate at 2.4GHz frequency.

Section 2 discusses on Partial Reconfiguration, Section 3 deals with Input / Output Peripheral Devices, Section 4 discusses about the Design Methodology, and Section 5 shows us the Simulation Results and Section 6 deals with the Physical Implementation on FPGA using Reconfigurable Modules.

2. Partial Reconfiguration

Partial Reconfiguration is a process of changing an area in FPGA without altering the other applications. Partial Reconfiguration flow is divided into two regions: Static and Dynamic. Static Region is a portion of the device that is programmed at start-up and never changes.

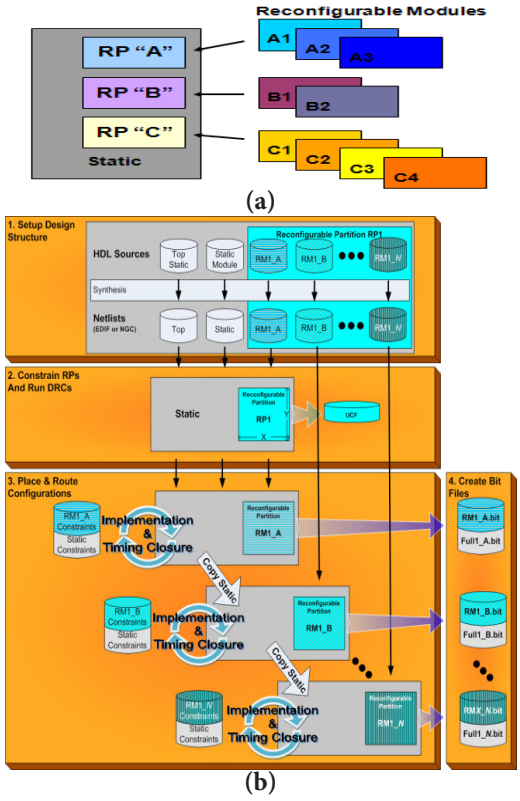


Figure 1. **(a)** Static & Dynamic Region **(b)** Partial Design Flow

Dynamic Region is a portion of the device that is reconfigured multiple times with different designs shown in Figure 1(a).

Design is sliced into reconfigurable partitions and each partition subdivided into reconfigurable modules[3]. Partial bit files are generated using partial design flow shown in Figure 1(b).

3. Input/Output Peripheral Devices

FPGA supports various Peripherals Devices like VGA, DVI, UART (RS232), PCI Express Interface, LCD, PS2, Rotary Encoder and GPIO expansion connectors etc4. In this paper UART, VGA, DVI and GPIO (XGI Expansion Headers) Peripherals are used for designing different reconfigurable modules.

3.1 UART

Universal Asynchronous Receiver Transmitter receives and transmits data in serial to parallel and parallel to serial with different Baud Rates per second with start, stop and parity bits. FPGA board consists of limited I/O's. N-Bit operations can be performed through RS-232 serial communication. UART is shown in Figure 2(a).

3.2 VGA

VGA is renowned standard interface in many applications such as video surveillance systems, industrial and medical applications. It provides a simple method to connect a system with a display for showing information or for users to interact with the system. During the evolution of PCs all kinds of display standards havebeen introduced: MGA, EGA, VGA, XGA, LCD, LED and HDMI etc. Nexys2 Spartan3E Digilent boards have a 3-bit 8-color VGA interface shown in Figure 2(b).

3.3 DVI

Digital Video Interface supports 1600x1200 resolution with 24-Bit Color through Chrontel CH7301 IC.DVI –to-VGA adaptor is used to connect conventional VGA Monitors shown in Figure 2(c). Video IIC Bus is used to control CH7301 IC supports both analog and digital signals. To read VGA Monitor parameters DVI uses IIC Bus Protocol. FPGA's available in the market supports from 3-bit to 24-bit colors depending on the application user can choose the bit color. Virtex 5 FPGA supports 24-bit colors.

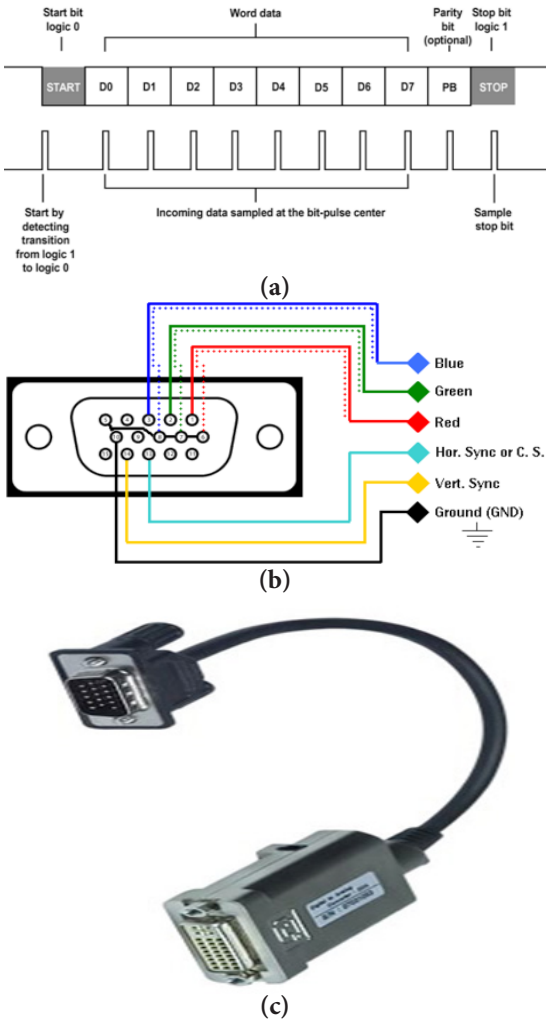


Figure 2. **(a)** UART **(b)** VGA **(c)** DVI

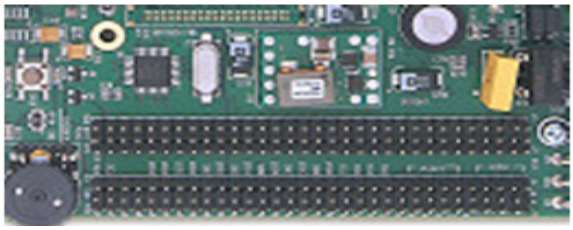


Figure 3. XGI Expansion Connectors

3.4 XGI Expansion Headers

The board contains expansion GPIO Headers shown in Figure 3 for easy expansion or adaptation of the board for other interface applications. The expansion connectors use standard 0.1-inch headers. The expansion connectors contain connections to single-ended and differential FPGA I/Os, ground, 2.5V/3.3V/5V power with various LVCMOS25 and LVCMOS33 TTL standards, JTAG chain, and the IIC bus.

3.5 ZigBee Module

ZigBee is a wireless technology suitable for short range, low power and low cost applications[5]. ZigBee protocol is developed with IEEE 802.15.4 standard. Among different wireless technologies, ZigBee technology stands on the top as it is able to provide a communication between devices and users in a simple and efficient manner. There are many types of ZigBee devices that are being used in wireless sensor and personal area network, home and industrial appliances. In this ZigBee S1 series module is used to control various appliances[6]. One of its specifications is that, they work within a range of one Mile and will operate at 2.4GHz frequency. ZigBee S1 & S2 were used to design reconfigurable video game. Comparison of ZigBee series with various parameters like Range, Power, Current, Sensitivity and supply voltage is given in Table 1.

Table 1. Comparison of ZigBee Series

Parameter	Pro	Series S1	Series S2
Indoor/urban Range	Up to 300ft (100m)	Up to 100ft (30m)	Up to 133ft (44m)
Outdoor line of Sight Range	1 mile (1600m)	Up to 300ft (100m)	Up to 400ft (130m)
Transmit Power output	63mw (18dBm)	1mW (0dbm)	2mW (+3dbm)
Data Rate	250kbps	250kbps	250kbps
Receiver Sensitivity	-100dBm	-92dbm	-98dbm
Supply Voltage	2.8-3.6v	2.8-3.4V	2.8-3.6V
Transmit Current	250mA@3.3V	45mA @3.3V	40mA @3.3V
Idle/Receiver Current	55mA	50mA	40mA
Frequency	2.4Ghz	2.4Ghz	2.4Ghz
Network Topology	Point-Point, Star and Mesh	Point-point, star, Mesh	Point-point, Star, Mesh
Addressing Options	PAN ID, Channel and Address	PAN ID, Channel and Address	PAN ID, Channel and Address

4. Design Methodology

The design hierarchy consists of top level static design and three reconfigurable partitions. Each Reconfigurable Partition (RP) consists of three Reconfigurable Modules (RM). Three Partitions are designed with different peripherals. First RM is designed with UART Peripheral [RS-232]. It consists of Adder RP-1, Subtraction RP-2, and Blank RP-3[7]. Second RM is designed with XGI Expansion Connectors to generate Random Pattern Generation which generates random keys encrypted with message produces cipher for TACIT and DNA Cryptographic Techniques can encrypt and decrypt data in wireless with ZigBee peripheral devices and BIST with different LFSR techniques to generate random test patterns shown. It consists of LPLFSR-I RP-1, Cellular Automata LFSR-II RP-2, and Blank RP-3 designed in Verilog HDL. Resource utilization of Reconfigurable Partitions for Virtex-5 FPGA Architecture is shown in Table 3. Third RM is designed a wireless video game with DVI-VGA and ZigBee Peripherals. DVI interface with IIC Bus is designed to display game logic with 640x480 screen resolution which is a major part in design and some modules must be static. Resource Utilization comparison for different FPGA architectures is shown in Table 2.

ZigBee based wireless video game is modelled and implemented on Spartan3E and Virtex 5 FPGA. This game is designed on 640x480 resolution VGA Monitor. Digilent Nexys2 Spartan3E FPGA supports 3-bit VGA that produces 8 colors where as Virtex5 FPGA supports 24-bit that produces multiple colors in DVI-VGA. Spartan3E FPGA board consists of 50 MHz and Virtex 5 FPGA consists of 100 MHz crystal oscillator. VGA peripheral supports 25 MHz clock frequency to enable graphical display. Digital clock manager IP core is used for clock division to synchronize graphical display on VGA and FPGA. Game logic is developed using Verilog HDL[7]. Wireless video game is organized in three phases. First Phase deals with VGA synchronization, Second Phase deals with ZigBee Interface whereas, Third Phase discusses about wireless keyboard design. The design methodology of game logicis broadly categorized into 3 phases:

1. First Phase illustrates game logic in VGA and is organized in five modules. VGA synchronization is dealt in first, Horizontal Counter & Vertical Counter (HC & VC) for pixel movement on screen in second, paddle movement in random directions in third, collision detection on screen in fourth and fifth module deals with score updating, if ball hits the target score will be incremented else if it hits the edges score will be decremented.
2. Second Phase describes interfacing of ZigBee with FPGA. Major part is among the different types of ZigBee's available for different applications, selection of ZigBee module for game design which supports voltage and current ratings with FPGA interface for transmission and reception of wireless data. ZigBee, Digi S1 is selected based on distance, cost and interfacing issues of Nexys2 and Virtex 5 FPGA. Two ZigBee Digi S1 modules are pre-configured as coordinator and router to work as transmitter and receiver based on distance and number of I/O's that are to be sampled. Several times ZigBee's are served as read and write to I/O configurations for coordinator and router;
3. Third phase deals with wireless keyboard. A wire board is sliced to serve as printed circuit board for hand held remote is used to play the game with users in compatible mode. ZigBee base is soldered on the board to hold ZigBee in the remote to communicate

Table 2. Resource utilization of game logic for different FPGA architectures

	Utilization		
Resource	**SPARTAN-3E**	**VIRTEX-5**	**VIRTEX-6**
No.of Sliced Flip Flops	3%	1%	1%
No.of 4 input LUTs	10%	1%	1%
No.of Occupied Slices	12%	1%	1%
IOBs	15%	5%	4%
No.of BUFGNUXs	12%	9%	9%

Table 3. Resource Utilization for RP1 & RP2 in Virtex-5 XUPV5LX110t FPGA Architectures

Resource	Utilization	Available	Utilization
Register	158	69120	1%
LUT	228	69120	1%
Slice	103	17280	1%
IO	10	640	1%
BUFG	1	32	3%

with FPGA wirelessly. When player presses the buttons ZigBee transmitter and receiver communicate and sends the control signals to FPGA to change the player direction on VGA Screen. Several control signals are used to pause, accelerate and retard the game. The reconfigurable ability to change the options like game color , score board updating, back ground color in game, increasing the chances of game life to win and lose the game makes the design even more unique[8,9]. Reconfiguration is done through Custom portable wireless technologies with ICAP Interface and SD card. To enhance the game resolution and number of Levels in game logic is based on game design and specifications. Architecture of ZYNC or ZYBO FPGAs was used for high resolution supports HDMI and levels of the game is improved with run time Partial Reconfiguration[10].

Plan Ahead Design Hierarchy for Reconfigurable Partition RP1, RP2 and VGA is shown Figure 4.

Percentage of Placement, Routing and Bit Stream generation for Reconfigurable Partitions is shown in Figure 5.

Virtex-5 FPGA, XUPV5LX110T Device Technology Schematic shown in Figure 6.

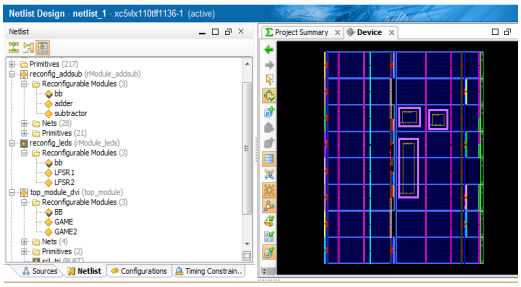


Figure 4. Plan Ahead Design Hierarchy

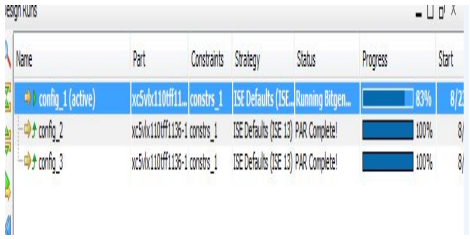


Figure 5. Place and Route - Bit Stream Generation

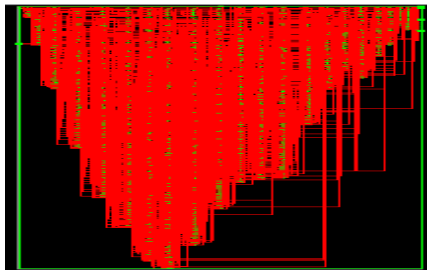


Figure 6. Technology Schematic

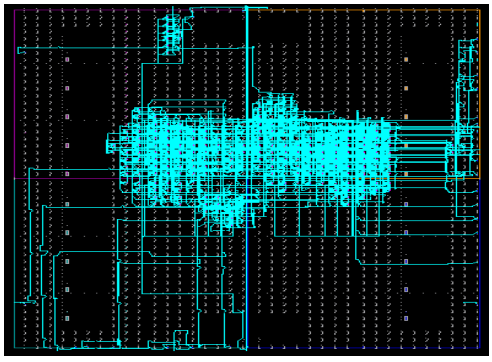


Figure 7. Routed Designs

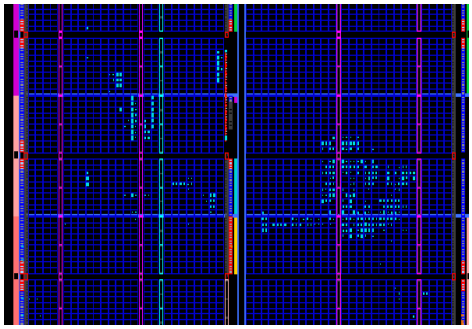


Figure 8. Floor Plan Occupancy

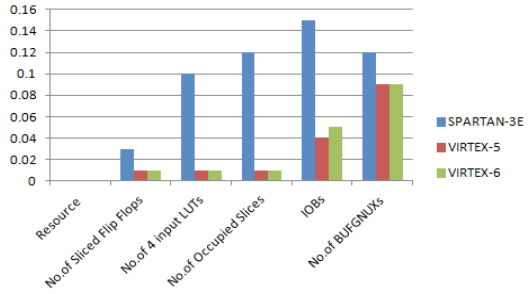


Figure 9. Resource Utilization Graph for Game Logic

Netlist of Partitions (Routed Design) is shown in Figure 7.

Area consumed for the targeted device (Floor Plan Occupancy) is shown in Figure 8.

Resource Utilization comparison for different FPGA architectures is shown in Table 2 and plot in Figure 9.

A comparison of Reconfigurable Partitions for Virtex-5 FPGA Architecture is shown in Table 3 and plot in Figure 10.

5. Simulation Results

LFSR Type I & II for Cryptography & Built in Self Test is shown in Figure 11 and 12.

Multiplexing LFSR I & II to Generate Random Test Pattern for BIST is shown in Figure 13(a)

Hardware implementation of cryptographic system with LFSR Type I & II which produces cipher can

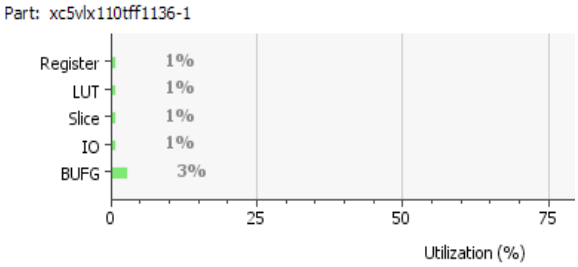


Figure 10. Resource Utilization Graph for RP1 & RP2.

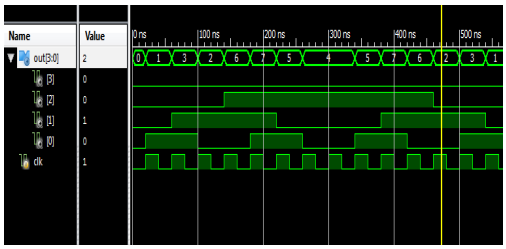


Figure 11. LFSR – I

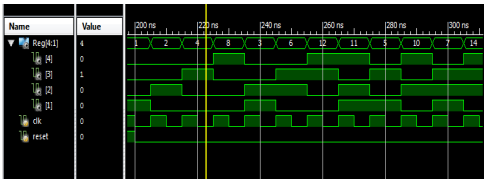


Figure 12. LFSR – II

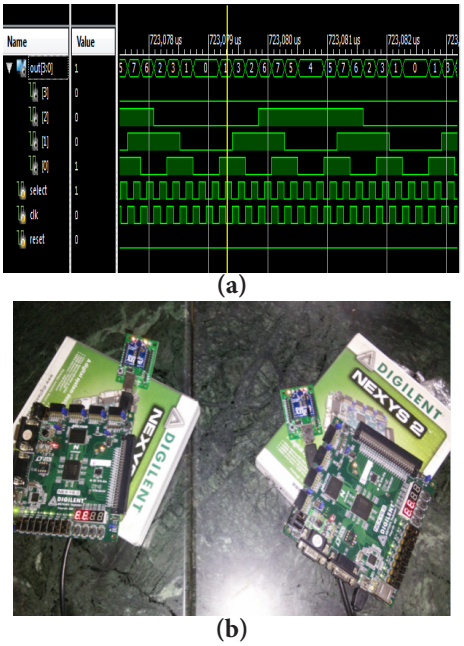


Figure 13. **(a)** Multiplexing LFSR I & II to Generate Random Test Pattern for BIST **(b)** TACIT & DNA Cryptographic Techniques with LFSR I & II for data Encryption and Decryption in wireless by Interfacing ZigBee peripheral devices.

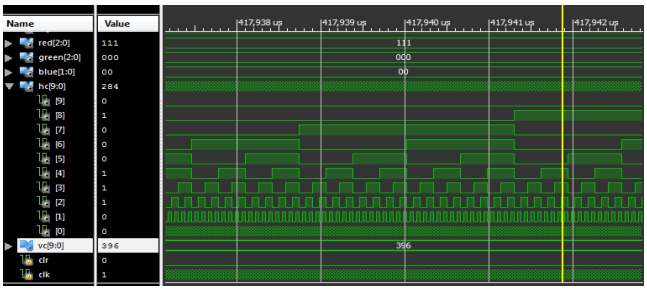


Figure 14. VGA Controller

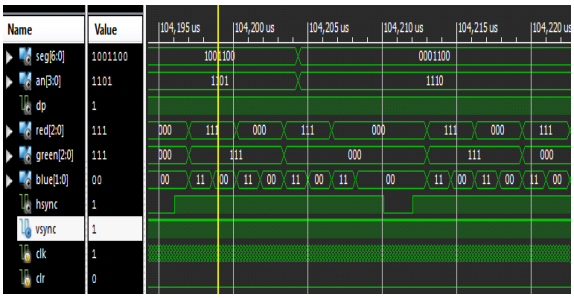


Figure 15. Sync Controller

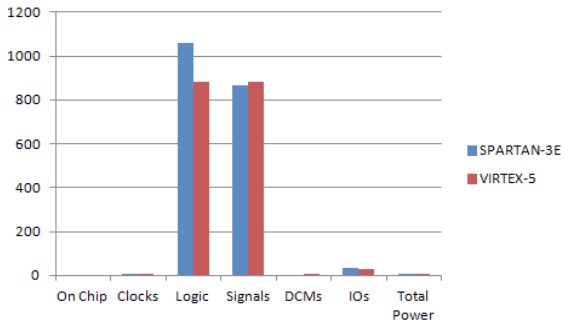


Figure 16. Power Dissipation Graph for Spartan & Virtex Devices.

be encrypt and decrypt data in wireless through ZigBee peripheral devices is shown in Figure13(b).

VGA Controller for generation of Red, Green, Blue, Horizontal and Vertical Raster signals generation to

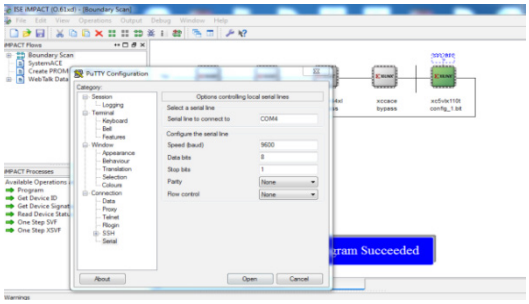
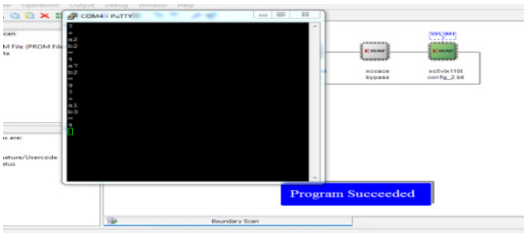
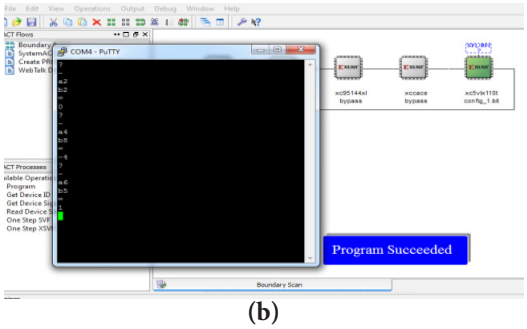


Figure 17. RS-232 Settings



(a)

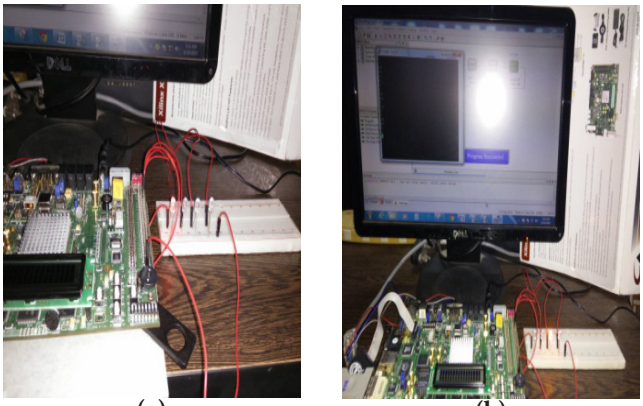


(b)

Figure 18. **(a)** Addition Operation in RS-232 **(b)** Subtraction Operation in RS-232

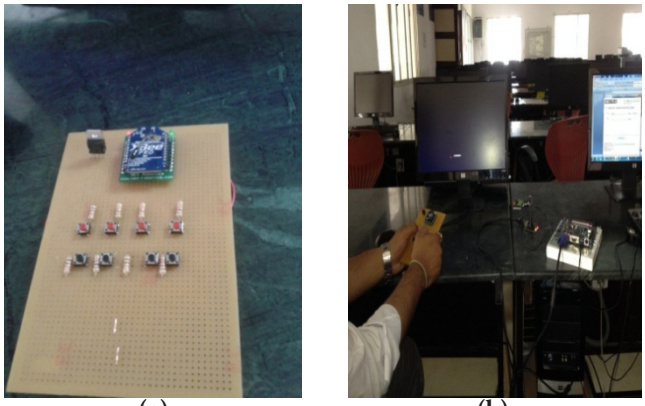
view display with standard aspect ratio (4:3) is shown in Figure 14.

Sync Controller to generate Horizontal & Vertical Signals match with Virtex-5 XUPV5LX110T Targeted Board clock frequency is shown in Figure 15.



(a) **(b)**

Figure 19. **(a)** LFSR- I XGI EH **(b)** LFSR- II through XGI EH



(a) **(b)**

Figure 20. **(a) User Plays Game with ZigBee Interface (b) Wireless Keyboard with FPGA & ZigBee**

Figure 21. **Color Bars in V5 DVI & VGA Interface**

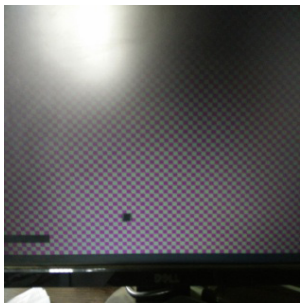


Figure 22. Game with Back Ground Color in V5 FPGA

Figure 23. Game with Suppressed Virtex5 FPGA

Figure 24. Game Logic with Back Ground in Virtex5

Power Dissipation Graph for Spartan & Virtex FPGA Architecturesis shown in Figure 16.

6. Physical View of Hardware Implementation Results on FPGA

Serial Communication Settings with Baud Rate, Data Bits, Start / Stop, Parity Bits, and Flow Control shown in Figure 17.

N-bit addition / Subtraction operation on HyperTerminal with (RS-232) Peripheral shown in Figure 18(a) and (b).

LFSR I & II to Generate Random Test Pattern for BIST using XGI Expansion GPIO Peripheralis shown in Figure 19 (a) and (b).

Wireless Video Game design with ZigBee Interface (Receiver) connected to FPGA and Wireless Keyboard ZigBee Interface (Transmitter) is shown in Figure 20 (a) and (b).

Color Bar Pattern on Virtex-5 FPGA to Test Multi Color along with Horizontal and Vertical Synchronization Settings is shown in Figure 21.

Video Game Logic with and without Back Ground Color in Virtex-5 FPGA is shown in Figure 22, 23 and 24.

7. Conclusion

Dynamically Reconfigurable applications are designed with various peripherals using Partial Reconfiguration (PR). Efficient hardware optimization, reusability, less time, cost and low power dissipation are the several advantages using PR. Partitioning of design, DRC and PR verify in plan ahead avoids logic that is not reconfigurable like clock modifying blocks (MMCM, DCM, PLL), global clock buffers (BUFG), device feature blocks (BSCAN, ICAP and PCIE). Design hierarchy should contain static logic and one or more reconfigurable partitions in each reconfigurable modules. Compare to Plan Ahead based PR several new advancements in Vivado based PR supports for latest Zync, Virtex7 & Kintex7 architectures with TCL scripting. Zync Architecture supports high performance Embedded- VLSI based SoC designs through inbuilt Cortex Processor for high throughput and better latency applications.

8. References

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