Indian Journal of Science and Technology, Vol 9(29), DOI: 10.17485/ijst/2016/v9i29/90862, August 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Multiple Scan Base Partitioning Technique to Increase the Throughput in VLSI Testing

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Abstract

Among any testing methods, scan testing is very significant for both in built and external schemes. The performance of the system should get maintained so the throughput plays major role. This paper tells about the retaining data which is hold technique and the jump process is attached to improve the throughput in VLSI testing. In order to achieve better performance the throughput is achieved by transferring the data per time and this gets increased constantly. The data in the partitions shifted sequentially when scan condition is on and when it is off the data may get corrupted so the system invalidate the testing process, the loss may get increase. In-order to solve the problem the data should get retained when the scan condition is not activated and to this process the jump technique is connected. The jump process connects to the output port when the condition is off. When compared to the first stage hold process this multiple partitions is beneficial. The implemented technique helps for the priority data, data rate and also to increase the throughput value approximately 85% to 87% as the clock frequency get reduced in the testing side. The area is reduced by 23.01% with the help of ISCAS benchmark circuit S5378when compared to the first stage hold technique where the benchmark helps to test the system.

Keywords: Hold Technique, Jump Technique, Multiple Scan Base Partition, Throughput, VLSI Testing

1. Introduction

With the fast growing and a rapid improvement in every testing process, the variation in every technology is needed and it is compulsory for all the required circuit and should test even after developing process got over in VLSI testing. The scan design creates an attractive solution for all the internal and external IC. The testing process may produce some failure and also affect the value of the route. For interior and exterior testing schemes the scan testing process produce the valuable result. There are two major sides for the scanning method, the transfer side and the detain side. In the transfer side the data is shifted and in the detain side the answers are saved. In the major designs, energy dissipated during transferring the data where the control of the detain phase is reduced because of the comparatively large number of cycles spent in each transfer and detain. The structural deprivation, extra evaporation of heat in circuit, crash of functional units and some defeat are generated because of more heat, power, delay and etc. The large percentage of the scan cells will constantly change the value in each clock cycle than normal mode of operation during scan testing these continuous switching cause delay. The connection between following test patterns engender by an Automatic Test Pattern Generator (ATPG). The transition switching is decreased by introducing the X-filling method where the unknown bits are filled. Low test power is estimated by using weighted transition metric method which achieves the average power[1].

To re-order each cell the scan cell re-arranging is used and compare the transition in each process. With the

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previous transition the comparison is done so that the re-arrangement is done easily but the time consumption is high[2]. The skip process is used to skip the unwanted segment during the shifting operation it is the complex part in that scan sub-partition reordering is not needed[3]. The performance should also get maintained parallel without any negotiation. A sub-word process with gating technique in clock is demonstrated. The particular segment power should pull down by dividing the signal into sub partition[4]. The ATPG technique is used to reduce the heat is negligible[5]. The bypassing technique in every scan design process helps to bypass the unwanted data. With the help of scan clocking in this process, the don't care data can be deactivated. The input volume can be reduced[6].The error may decrease the life time of the major circuit. Instead of using general delay minimization technique, a one level capture technique is used[7]. Low test architecture loads the data in one path continuously to reduce transition activity in other paths[8]. The input pattern transition cause sequence damage to the circuit so the dynamic partitioning is used to reduce power[9].High-Compression ratio is implemented using large scan-chain design based on XOR network technique which reduce the number of switching activity associated with it[10].

During testing the multi-phase clock scan is implemented based on controlling the clock which helps to decrease the switching activity[11]. The voltage droop and some loss is due to the higher switching and the test vector is considered and re-order is done[12]. The data shift during scanning time based on the partition is implemented. Along with this, connection technique Q-D is used to reduce power but time got increased[13]. The sub-clock power gating for reducing leakage during dynamic mode[14]. The segments are obtained from the scan architecture using partitioning technique. The obtained segments are grouped that should be compatible[15]. The time consumption is reduced by decreasing the repeating side[16]. The in-built flip-flops are modified due to the elements used in the circuit consume more power[17]. The various techniques are helped in various ways to show the improvement in all the internal and external part of the manufactured system[18].The scan output is increased by using the flipped scan chain method. The scan chain scheme is introduced using additional inverters to enhance the complexity by comparing traditional scan-chain[19]. Weighted bit position is efficient based compression algorithm in which the test patterns are reduced significantly[20].

1.1 Scan Architecture with Hold Technique

The scanning process was done using in and out operation that is bypassing the data in to the circuit and getting the response. The defects may produce by the clock distribution tree, time consumption. The main target is about the power reduction, the area minimization. The scan path is divided and multiplexer is placed in between each divided portion to select the scanned data or normal data. When the multiplexer select signal is high, the scanned part move to the next part in the circuit and the process continuous till the scan-out (output) is obtained. The active part is scanned (particular part) but the other partitions is in rest condition so the data may get degraded in the rest partition. To retain the data without any corruption or degradation, the data must be in the hold condition. So the degradation is reduced drastically. The clock signal is blocked to retain the data but skew problems occurred. The data in the testing field is very important to check all the parts of the system even after the manufacturing process got over. The Figure 1 explains the hold technique used the feed-back mechanism to reduce the failures and to retain the data. The tri state buffers are used and also the multiplexer is processed according to the select signal. When the select signal is low the process is in general function, when the select signal is high the process act at scanning mode and transfer operation take place. The flip-flop is used, to get the output at the scan-out. The Figure 2 tells the hold technique is extended for multiple partitions (chain) where the multiplexer is placed in between the hold technique. This hold technique used to retain the data even when the segment is bypassed without any corruption.

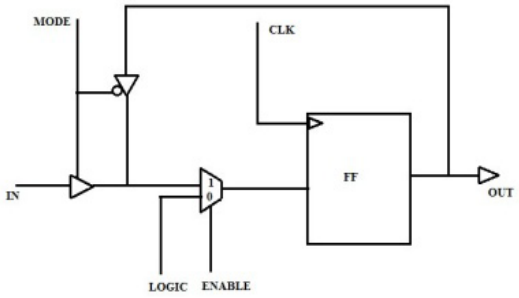

Figure 1. Hold technique.

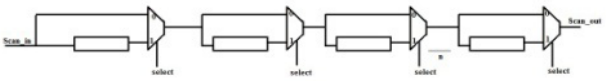

Figure 2. Partitions for the hold chain.

The data which is passed must go by the chain and get reached the scan out at last. This process is used for scanning the data in chain process. The multiplexer is placed in between each partition so that based on the select signal the data bypassed each partition. Assume, there are n the process continues till the last partition got over. The needed scan operation implemented in the partitions when the scan mode is activated. In scan operation the holding data technique is used. Hence the hold technique helped to retain the data.

2. Proposed System

The fundamental operation of the scan design is the given data should pass to the path will go around all the partition and produce the output which helps to find the transitions in each part, the scanned data is also identified and when the switching occurs the power is consumed more than in the normal functional operation. Though the area, power, speed are analyzed and corrected the important factor such as performance so the throughput of the system is analyzed. The throughput of the system is calculated based on the clock frequency. The jump architecture is one of the designs for test. The past topic summarized about the hold technique which retain the data to avoid the degradation if the single bit is passed to the chain path the process take pace and the bit which was scanned is passed to scan-out but the prior topic not succeed to summarize about the don't care bits which was not needed. The don't care bits create unwanted power consumption and also time consumption is increased and also the multiple bits execution was not summarized in the last process.

2.1 Jump Technique

Apart from the traditional structure, which transfer only one bit per clock cycle and the process accept the next bit only after completing the first bit operation. The jump architecture transfer two bits per clock cycle so that without raising the application time the required data will over to particular partition. Compared to prior work the clock frequency is reduced. The jump scan technique which avoids the threat of clock skew so that doesn't need modification to the clock trees. The Figure 3 shows the additional routing for jumping is achieved by attaching the jump architecture with the scan hold cell process. The jump scan is well-suited than existing scan hold cells. The additional computation is not needed. The jump mode gets activate only when the scan mode is in off condition. If the processor doesn't need any scan data the process can jump to the next position and also if don't care bits are found the process jumps to the jump architecture mode. The main application of this modified structure is the data rate is increased, at the same time the application time is maintained. The output displays at the scan-out. The hold cell had variables to scan the data and also for the normal mode. The jump architecture need one additional variable to enable the jump architecture. The architecture starts from the normal operation and based on the mode variable the process change the input for multiplexer. If the mode variable is high the input will move to the multiplexer. The allow signal activate based on the request and the output pass to the input for the flip-flop. If processor need to off the scan mode and to active the jump mode the scan allow variable value must be '0' and the jump mode variable must be '1'.

The jump process can use the path for several partitions. The Figure 4 explains the chain contains two routing path to route the data in the process jump path and scan path. 1) The jump path directly connects to the output port to direct the data to the scan-out when the scan enable mode is in off condition.2) The scan path gets activate when the scan enable is in on condition. The scan cell can place in the increasing order from the scan chain to scan out. The data is passing to the port according to the required path. In the chain path if the process want to do the normal mode scan enable will be 0 and if the

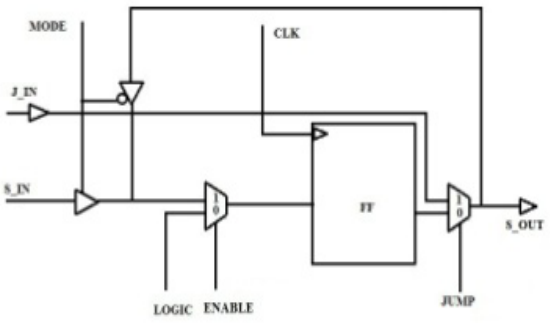

Figure 3. Jump technique.

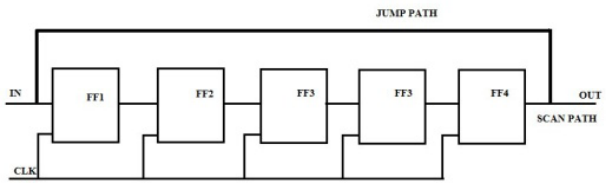

Figure 4. Proposed Hold-jump partitions technique.

process need the scan then the enable will be in 1 and the process continues with this flow if the last summarized modes are in off then the path jump to the jump path. This process helps to get the value which was scanned and also the normal functionally operated values.

This jump and scan path is useful in every testing side for getting the appropriate value. The ISCAS'89benchmark circuits are used for this architecture. The test pattern generation is used to activate the benchmark circuits and the output is used for the implemented process. The result of the benchmark circuits are set as input to the needed process. Though the throughput is increased by attaching the jump mode in the hold technique the area is slightly increased. The throughput of the system is calculated based on the data rate and also based on clock frequency. As the clock frequency is reduced and the data rate is increased the throughput is increased.

3. Experimental Result

The ISCAS 89 benchmark circuits are used for getting the result. The Table 1 tells about the implemented process with the help of benchmark circuit the clock frequency is found and based on the data rate, the throughput is calculated where Figures 5 and 6 shows the graph. The experimental conclusion explains about the throughput value for 2, 4, 6, 8, 10 partitions .The graph presented tells the throughput value for the prior work and also the presented work. In the graph the presented wok throughput value is increased constantly. The s1512 and s5378 bench mark circuits are used here. The area is compared with the first stage hold technique where Table 2explains the comparison.

Table 1. Comparison of area and throughput

Benchmark circuits	Partitions	Area Existing	Area Proposed	Throughput Existing	Throughput Proposed
S1512	2	2333	2053	21.71	293.63
	4	2230	2504	20.92	151.16
	6	2310	2501	21.71	151.15
	8	2386	2501	21.70	151.15
	10	2469	2502	21.69	151.16
S5378	2	4812	4539	17.35	172.61
	4	4789	4991	16.47	170.61
	6	4790	4992	18.13	170.50
	8	4865	4992	17.55	170.20
	10	4861	4994	16.47	170.61

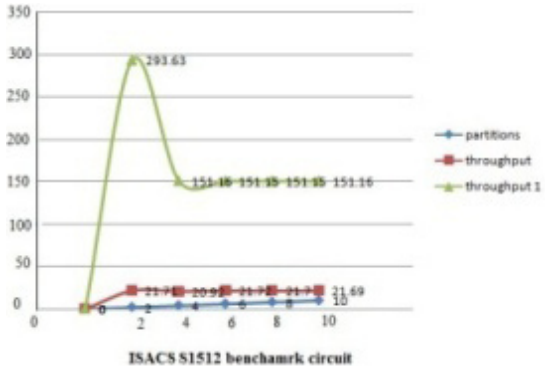

Figure 5. Throughput comparison for S1512.

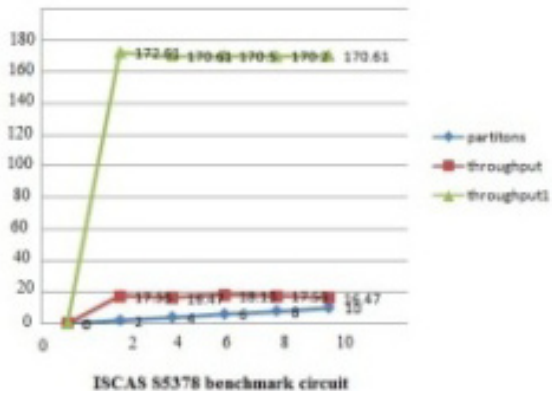

Figure 6. Throughput comparison for S5378.

Table 2. Area comparison result

Benchmark circuits	Area[7]	Area [present work]	Decreased percentage
S5378	41.98	18.97	23.01

4. Conclusion

The hold technique where the data in the partitions shifted sequentially when scan condition is on and when it is off the data may get corrupted so the system invalidate the testing process, the loss may get increase. In-order to solve the problem the data should get retained when the scan condition is not activated and to this process the jump technique is connected. The jump process connects to the output port when the jump enable is in on condition. The implemented technique increase the throughput approximately 85% to 87% based on the clock frequency and also based on the data rate. The area consumption is reduced by 23.01 % when compared to the first stage hold technique. The ISCAS'89 benchmark circuits are used to get the clock frequency and area.

5. References

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