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Recognization of Delay Faults in Cluster based FPGA using BIST

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Abstract

This paper discussed about the increasing complexity of Field-Programmable Gate Array (FPGA) in finding delay faults using BIST technique. It is a major challenge for FPGA for highest troubles shoot text and delay circuit quickly. Built-in-self-test method is a simple solution compared with expensive test equipment for the automatic transmission. Herein, the erection designed for the detection of delay faults in the second coefficient of FPGA resources Digital Signal Processing (DSP) block, FPGA board interconnects, Look-Up-Tables (LUT) and etc. The authors suggest comprehensive plan diagnose Bister to improve the effectiveness of the control logic, which diagnose all CLB 2 x 3 BIST are faulty. The overall process for the simulation has been done by tool Xilinx FPGA Vertex FPGA. The results show a significant improvement over previous methods.

Keyword: BIST, CLB, Delay Fault, FPGA, LUT, ORA

1. Introduction

The Field Programmable Gate Array (FPGA) access is a widely accepted design applications for small and medium operational flexibility and the development of low cost. FPGA reconfiguration material allows the use of the functions and features that are not specific integrated Ferrari (ASIC) available. Test methods for FPGA listening reconfigure multiple FPGA scene a small part of FPGA hardware noticed under normal applications simultaneously "the other, most of those who can work". It is possible to have multiple logical block components (CLB), which is coupled to[3-6], having about 80% of testing the specific compounds of the FPGA area. Test can detect hidden defects. Ten years is an integrated self-test[7-10]. These methods are popular in the test and the diagnosis of a variety of flaws FPGA. "This method was one of two design makes Bister roving linear diagnosis (Bank)[9] is proposed. Bister proposals avoid affecting the diagnosis will tell us the extent of the difference between loud. Technology to achieve most animal's functional diagnosis - testing intelligent based on three Programmable Logic Block (PLB), Test Pattern Generator (TPG) and Output Response Analyzer (ORA). This process[11] as a programmable logic developed on the basis of ultrasound. The proposed approach combines the techniques of mass scale sowing unsafe failures. Work[12] analyzed the timing behavior of Look-Up-Tables (LUT) in FPGA. The author has demonstrated that the delay functions independently hunt in the LUT.

Proposed, a clear structure of[13] to detect a defect in the LUT of SRAM, which is based on FPGA. Test architecture is the same as proposed in[6], but the Output Response Analyzer (ORA) technology[14] is used to online testing and off line What observed openings delay FPGA .By using self-testing area (star)[15] the leading architecture, troubleshooting tests from stick-to-failure, shortcomings and delays in the FPGA connections. There[2,16] was diagnosed delayed FPGA resources. Standard LUT delay dynamic model, FPGA (RC), declare resistor-capacitor. [12]In this model, the residues may be from n stages cascade SRAM cells in each phase of a set of vertical (2: 1) multiplexer[6,12,13]. The reason why the delay LUT testability proposed[6,13] have a number of disadvantages. Moreover,

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one of the drawbacks of these defenses behind Flip-Flop is up delay circuit in the LUT.

There are also predicting many challenging time for LUT. Long cables used pm transfer may be delayed. We propose a new method, an error delay fault of diagnosis in FPGA cluster[6,13]. The goal is to use logic and routing approach to diagnose the fault delay in FPGA-based cards. The delay is a bug in all major components of the FPGA. Curriculum can be used in a network test Xilinx JBits 3.0 API (Application Program Interface) and XHWI (Xilinx hardware interface) Virtex-II FPGA[17] to give a little knowledge and a little stream objectives of the committee otherwise FPGAs are composed of a two-dimensional array of programmable connections and is connected to the CLB[17]. CLB rejected by the logic element and storage element (flip-flop). Moreover, function generators, CLB multiplexers, arithmetic logic unit and SRAM's. Some modern components dedicated FPGA can be avoided if the coefficient and "SDG mathematical functions, DSP filters and complicated arithmetic operations of a general FPGA feeding without routing sources. The communication between the CLB made a programmable connection network, consists of a programmable control cable points of the matrix violated specification ORA delay defects are modeled in the source routing connection where weakening of the logic of failure. [18]There are many models used late in FPGA components of behavior.

The delay is the main delay to traffic, the slow deterioration of the FPGA devices. Delays are ignored, as defined by the change (s) in an amount, the time which causes a change in the output. This model has already led to the most commonly used model is the passage, which ends up being logical diagram errors, delaying the progress and transition of logic gates. There are two types of errors transition slow raise (T-S-R) and transition slow fall (t-S-F)[8,10]. The seeds are often moved as part of the French seed used wire network. Seed breakpoint, wire machine integrated "with the end of breaking the border and seed potatoes seeds multiplexer to indicate a common base output is con pieces GURABO. The analysis of the model components delays the proposed[19-21]. The delay in a wire segment can be modeled in number of ways. Each accuracy level and calculation vary RC model is relatively accurate and easy to calculate timber RC combine connect multiple bottom segment of the CLB through pipe.

2. Proposed Method

2.1. LUT Test using the BUT Configuration

Expansion LUT application error eliminates the disadvantages of the year[6,13] have shown the way. The connection between BUT and TPG and between LUTs within BUT are established by wires of different lengths (long wires, local wires).The delay is caused by different wires may interfere with the test. Therefore better detect errors, the effect of the error (LUT, long telephone poles) to consider apart. In order to solve this problem, D flip-flop IP address associated with the largest power LUT left as shown in Figure 1a. Left-LUT cannot be tested and is considered a permanent part of TPG. State S-T-R S-R-R and S-T-F functions f (A0, A1... N-1) = 0 and f (A0, A1... N-1) = 0, respectively. If there is no delay in the chain, and they had spent LUT output. The clock is connected to D Flip-Flop is more than six times to a signal TPG LUT is a free state error. Changing the filter configuration as shown in Figure 1b used for short distances, for detecting errors in the middle of the length of the wire, and local. During the test production line. Figure1a shows the actual value and that of Figure 1b of the output we reported that the delay caused by the delay in the pipeline and a short iron. N 2 n vectors that is necessary to the LUT after the test.

2.2. Testing of MULTIPLEXERS using BUT Configuration

FPGAs are a pair of multiplexers that are used to perform the logic. Therefore, it is important to assess the multiplexers. Some internal FPGA plywood and developers have no control over those resources. Multiplexers to test their enclosure, as shown in Figure 2. The only rules plywood CLB configuration and functionality of the application under test. For example, Xilinx Vertex-II[17], FPGA, (16: 1) detention multiplexer configuration can be adapted to each of multiplexers (MUXF5, MUXF7, MU*XF6, MUXF8) as shown testing. A*ppropriate test vectors applied to the line of the selected input test line. Additional costs for advising the error S-R-R and S-T-F. 2n-test vectors are required to all inputs (2n: 1) to test multiplexers. N line test application-test vectors, which is similar to the "against Jonson, as specified in the order. The decisions (to test 2n-1) are, the selection *of the N-line testing vectors.* When a fault is detected by ORA by configuring smaller multiplexer chain, the faulty location can be identified by the divide and conquered rule.

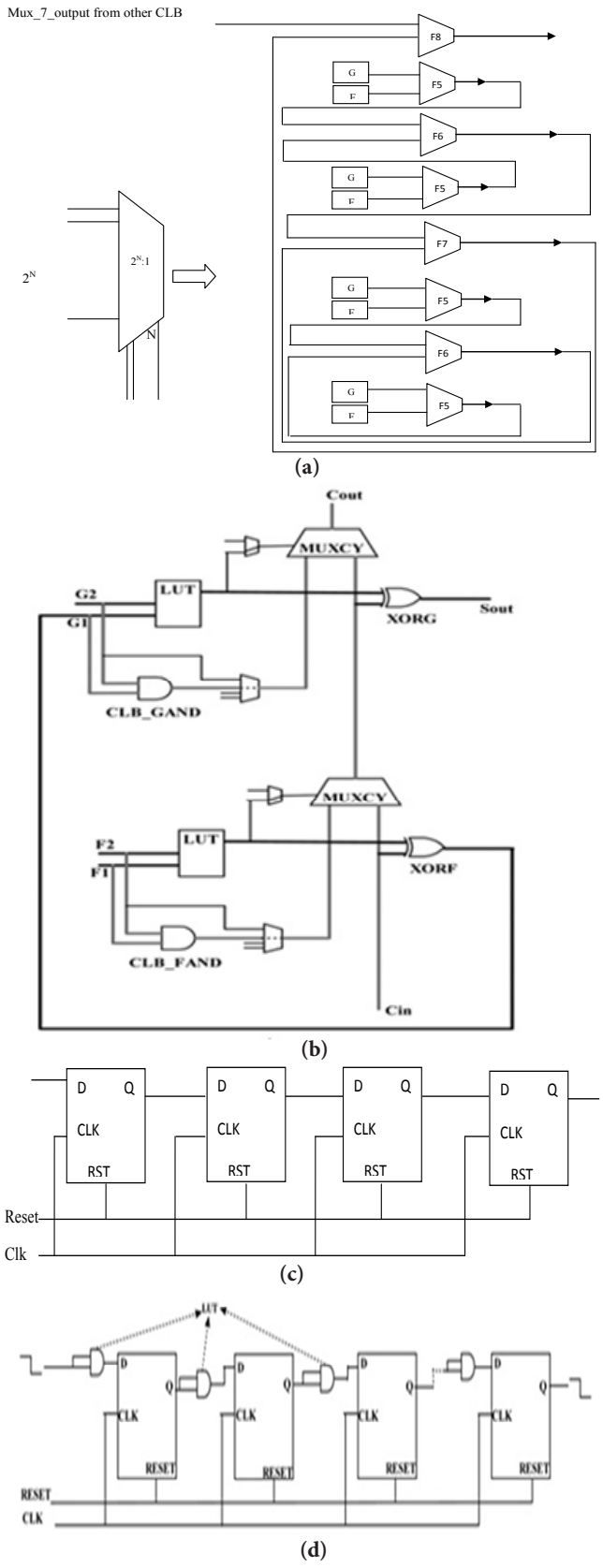


Figure 1. Testing various resources CLB..

3. Testing Arthematic logic using BUT Configuration

CLB of the FPGA contains arithmetic logic units and interconnects. Those who do not program the FPGA have tested detailed work. For example retardation because "sum" and carry propagation"(paths includes all communications multiplexers and other means) in a Xilinx FPGA, we internment recovery, but the adder carrier report k-bit" sum "output of the adder is connected used with the input of the next adder. Vectors Testing, an transition to low → high, and instead of an adder spread from one stage to a second stage adder, as shown in figure 2. Figure 2, the red lines are the typical paths and logic means, and the black line represents the quantity of partners and logic resources. LUT and exclusive OR (XOR) generally carries a logic of total and MUXCY (multiplexer adder carry example link is CLB FPGA) and a second multiplexer used in the construction of production and distribution of the logic. The process starts with the amount of boats and low paths and place a high transition, made "F1F2→XOR →G1G2→cout t 'through the introduction of F1 and" 1 "to the low-high transition in the same way of introducing G2 = F1 = "1" and u = 0. This amendment makes the transition from "F1F2→XOR →G1G2→cout". Data from laboratory tests with various vectors are shown in Figure3.

4. Testing D-flip-flop using BUT Configuration

The basic element consists of D flip-flop IP connected to the LUT. (2: 1 MUX)[17] FI, configurable multiplexer, may take a developer to extend well beyond the BEC, D flip-flop, or the path that leads to the production of the same CLB through D flip-flop. Figure 2 shows the configuration of the test in different ways. If there is no delay in one or more flip-flops by chain S-T-R, S-T-F transition delay test, and the clock is the ORA of the line flip-flop. No representations are connected to the network. Delay spread may have occurred over the entire chain, and can be demonstrated by the ORA. It cannot provide the exact location of the fault to be found in the legal proceedings.

5. Implementation of BIST

5.1. Output Analyzer Analysis

Circuit consists BIST Test Pattern Generator (TPG) and an Output Response Analyzer (ORA). Comparing and

Test Vector Order	Input terminal of the BUT				path	Transition
	G2	F1	F2	Cin		
1	0	0	0	0		Initializes all paths to "0"
2	0	1	0	1	cinMuxcyout	
3	1	1	0	0		
					F1F2 xor G1G2 Cout	
4	0	0	0	0		
5	1	1	0	1	cinMuxcyout	
6	0	1	0	0		
7	1	1	1	0	F1F2 Muxcyout	
8	1	0	0	0		

Figure 2. Analysis of CLB and sequence of delay-fault test.

analyzing the output signals from two targets tank model changed as shown in Figure 3. The two XOR gate inputs and outputs of two goals. In Figure 3, the XOR gates have been observed to give a "0" if no delay.

When producing a delay of the XOR gate twice and T Flip Flop generates a square wave, a factor which is equal to the input wave. Where t S or S, R-T-F unchanged, the production of the T flip-flop transition. ORA event can be considered as limiting the scan memory, or to drive to work. The whole event is a success/failure, unless the game/missing. Flip-flop with the representation in Figure 3, the amount of the index/length of the delay. Set line can be measured with a delay. If you try little to XO oscillation, as shown in Figure 3. The two counters, one of which is N bits, the second K-bit counter is used to measure the delay time purposes. When the overflow from the n-bit counter. It will be a counter increases k bits. If N is the number of n-bit counter and K k-bit counter, so that the delay be equal to (N * F + NT), NT excess of the maximum number of n-bit counter. The width of the second counter is selected action in view of the expected maximum delay. If the result is "zero", then we can conclude that the error break.

5.2. Test Methodology for BIST Implementation

The new logic (2 x 3) Structure of Bister, as shown in Figure4 is a fully diagnose Bister. Y 1, Y 2, Y 3 is an end view BIST. The first and third output assemblies relative to try to compare the output signal of the first and third set. All sessions CLB evaluation (2 x 3) Bister required, as shown in Figure4. Redundant (✓) if both inputs are in the same position, otherwise it will not work (x).

Case 1: If CLB. In all that time, actually, '' signal. Therefore, there is no mistake.

Case 2: If default CLB (diagnosis): Bister-test response is similar to the line A-series. The associated fault line. TPG is the CLB defect, faulty test vector as a target. Jacquet two errors, they will be the same answer. Therefore responses Y1, Y3 "go" signal. This makes E2 reason. "Each session lasts bist so if someone CLB standard, then the answer is 'no'. Therefore, Figure 4, we can say CLB-A.

Case 3: If the defect of the two CLB (two diagnosable): standard, as shown in Figure4 is formed in response to the line "C" in Figure4. Remove the CLB is now completely in the figure4 CLB over to the table.

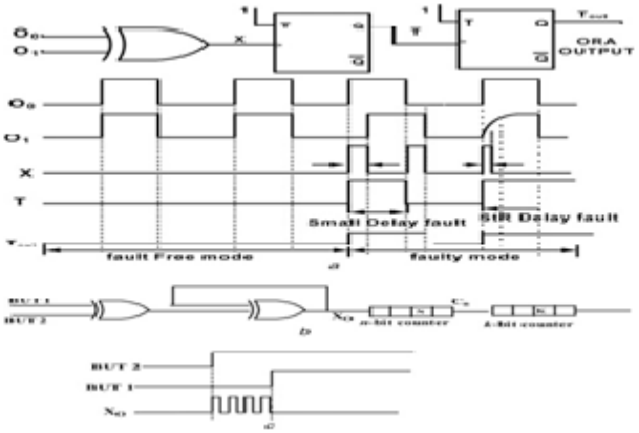
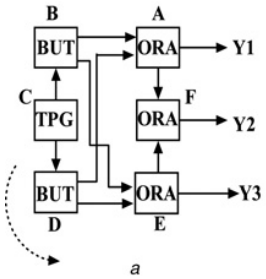


Figure 3. ORA Configuration.



Sessions / CLB	S 1	S 2	S 3	S 4	S 5	S 6
A	ORA Y1	ORA Y2	ORA Y3	BUT	TPG	BUT
B	BUT	ORA Y1	ORA Y2	ORA Y3	BUT	TPG
C	TPG	BUT	ORA Y1	ORA Y2	ORA Y3	BUT
D	BUT	TPG	BUT	ORA Y1	ORA Y2	ORA Y3
E	ORA Y3	BUT	TPG	BUT	ORA Y1	ORA Y2
F	ORA Y2	ORA Y3	BUT	TPG	BUT	ORA Y1

b

Figure 4. Structure of BISTer.

Case 4: If we CLB patients (diagnosed three) S2, S3, S4, an airline Figure 4 are all "no." This deficiency may be caused by a malfunction or defective targets. In S1, Y1 and Y3 "no" answer. This may be due to the failure of an ORA. E2 reaction "only" if both ORA1 and A3, or both, are impeccable. Thus, it is demonstrated that BEC "F" is the infinite intact. To remove all the CLB, albeit in accordance with the figure 4.CLB remains determined than ever.

Case 5: If CLB four patients (diagnosis) Fault line. 3D makes the online abde. Only Y 2 is "only" S1 and S4. BEC as "F" and "C" seems to be perfect.

Case 6: If CLB (five diagnosed) Y 2, Y 3 and Y 1, the coefficients (more) S1, S2, and S6, respectively. Error, as shown in Figure 4. CLB time 'F' intact.

Case 7: If all patients with CLB (schedule) of the total production 'successful', as shown in Figure4. This shows that each CLB damage. We make use of the mobile-STAR (Rotate) in order to test the error. V-STAR and STAR-H with respect to the perpendicular line by means of water is necessary to test in the online test. STAR field trials moved to the right side of the two lines and two lines of fi phone. FPGA (W x H), all 6 × [M {/} 3] with depicting mandatory testing where G> L, delay corresponding set of horizontal and vertical metal part and the input (CIP) can be controlled by both H and V star ester [1, 14, 15]. "Metal Test (Wut) tested simultaneously. A Wut, for example, is selected, easily. The means test capable will ℓ test that the number of the son in the (W x H) with FPGA idols., ℓ /., p, m / sec, wherein R, ℓ (where ℓ is to be divided large requires proven in two parts, and r is the maximum number of cables), m> σ s and the sum of the number of rows and the number of H - Stelo number of V -STAR.

2D field model CLB FPGA Xilinx Virtex-II, four-input LUT (CLB 32 inputs and eight lines) and FL-FL IP ops eight. Each CLB "0" is complete and a "1" in a bad state. 6 CLB used to build the structure Bister. Bister walk CLB functions and results of a cyclic series of experiments are shown in the table, see. 8 in each test. So if CLB Lemma 1 and Figure 4 give incorrect filed and diagnose the size of our ability to compare difficulties Bister CLB three different models mistakes. (I) defect CLB are unevenly distributed (ii) inadequate poorly distributed CLB group wrong distribution CLB defect cluster probability density function (PDF) = W / (m + 1) 2, where m is the Manhattan distance c is a constant. (III) a high interference cluster (a defect of the defective cluster CLB PDF = W / (m + 1)). To compare the results, we make two mistakes density parameter diagnostic overlap. The density is defined as a defect alarm FPGA CLB 1000, and diagnostic coverage is defined as a percentage of the disease diagnosed well[9]. Figure 5 is a comparison of our work[9,22]. Figure 5 we say that we achieved 100% of the fault coverage, compared with the previous work. This improvement was achieved by diagnosing the nature of our Bister. We simulate the function blocks Bister (TPG but GOLD category A) Vertex-II (xc2v1000) and Vertex-V (xc5VLX50) FPGA. ISE7.1 and Modelsim 6.0 is used to simulate a Vertex-II and Vertex FPGA in simulated ISE12.1. 5 speeds - The simulation is carried out at a temperature. Conditions

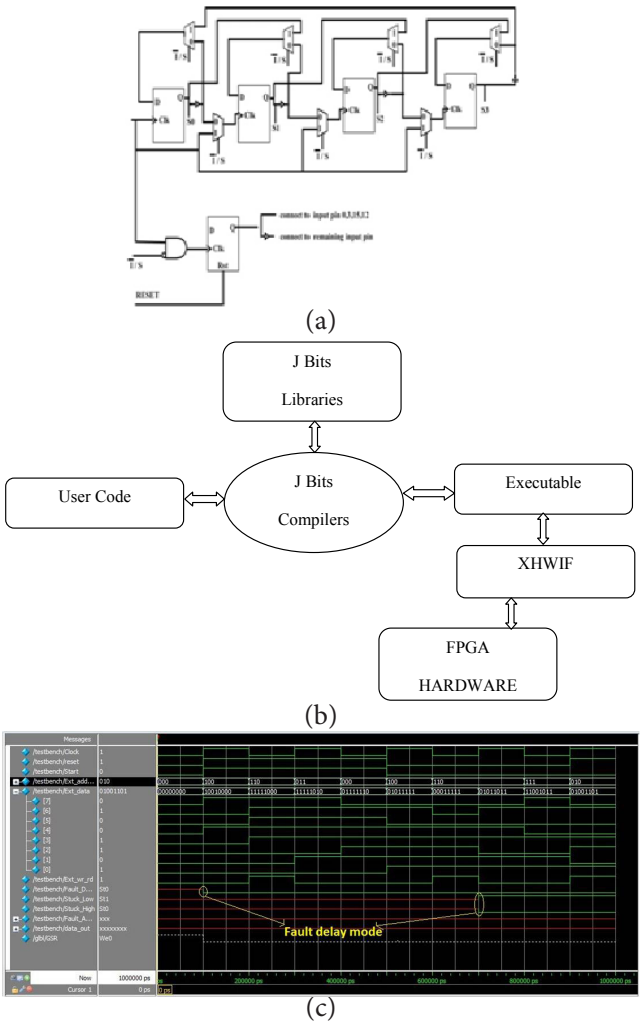


Figure 5. **(a)** D-Flip-Flop with MUX for diagnosing of faults. **(b)** execution flow. **(c)**. simulation result of delay fault mode.

inefficient emulate the expansion of the MAS. No use of the test with a test bench VHDL. Local restorations are fully recovered normal function block. For example, a delay faults testing TPG photo multiplexers. One of the input clock, a zero, and an I/O line selection. If the selection of the line I / O is "0", GPT has a second counter that Johnson counter is active.

Figure 5 Comparison of the ongoing work[9,22]. The comparison is made in our work and fast-Di (2 x 3BISTer)[9] STAR (3 x 2 Bister)[9,22]. Therefore, the ability to perform a number of errors transported to the strong error in the cluster addresses .8 MHz clock is also a bit counter and the clock frequency dividing means, which is used by the "F". "F" is dependent on the maximum time of path interference, and f is a five-ORA to stabilize the output before the next series of experiments. The frequency divider circuit outside STAR performed unused portions of the FPGA. Figure 5 shows the simulation result which shows the delay faults. Simulated Bister structure is implemented in the Vertex-II FPGA Configuration CLB.JBits API designer's access to FPGA resources (CLB, IOB, PIP, etc.). A small stream of income for FPGA is.

loaded via API XHWIF and compared to internal configuration access port (ICAP). XHWIF (Xilinx hardware interface) interface with different FPGA Request communicate the FPGA selection. XHWIF was then used to read the data from the FPGA. I (0: 7), typically a rigid ICAP write memory, and the reverse reads E (0, 7) of the pin. Locked CCLK EC[17] the pins are control pins. You can choose a specific group and CLB has configuration structure Bister

5.3 Power Analysis

The power calculation of finding the delay faults has been shown in above figures. Drastically the power gain has been occurred while giving the input signals and clock

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.000	3	---	---
Logic	0.000	292	1408	20.7
Signals	0.000	385	---	---
IOs	0.000	29	108	26.9
Total Quiescent Power	**0.019**			
Total Dynamic Power	**0.000**			
Total Power	**0.019**			

(a)

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.001	3	---	---
Logic	0.000	292	1408	20.7
Signals	0.000	385	---	---
IOs	0.000	29	108	26.9
Total Quiescent Power	**0.019**			
Total Dynamic Power	**0.003**			
Total Power	**0.022**			

(b)

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.003	3	---	---
Logic	0.000	292	1408	20.7
Signals	0.000	385	---	---
IOs	0.000	29	108	26.9
Total Quiescent Power	**0.019**			
Total Dynamic Power	**0.005**			
Total Power	**0.024**			

(c)

Figure 6 **(a)**. power calculation before applying clock and input signals. **(b)**. power calculation after applying clock signals. **(c)**. power calculation after applying input signals.

signals. Figure 6(a) shows the power calculation before applying the signals. Figure 6(b) shows after applying the clock signals. Figure 6(c) shows power calculations after applying the input signals.

6. Conclusion

This article presents a method for testing a delay caused in different clusters with the aid of FPGAs. The proposed test method can be used to take advantage of reduced access STAR both online and off line testing. The proposed BIST method can test all sources (such as LUT, flip flop, an arithmetic logic unit, a multiplier, multiplexers and DSP devices) in modern FPGAs charge extra effort. The increases proposed new full diagnosis clear structure BIST logic test efficiency. Clear structure in earlier work to diagnose proposed 2-2, shows the presence of two closely BIST CLB con figuration. The proposed structure is an intelligent diagnostic resolution of 100% to 100% coverage of the video by the methods previously proposed, only the resolution of diagnosis of 86% to 30% of the density of defects. We have achieved a significant improvement compared to the previous BIST proposed method. We replicate the error delay longer string in case of failure, compared with intact. We have our proposed plan Xilinx Vertex-II and V FPGAs, ISE tools, ModelSim.

7. References

1. Das N, Roy P, Rahaman H. Build-in-self-test of FPGA for diagnosis of delay fault. IEEE ASQED. 2011; 54–61.
2. Das N, Roy P, Rahama H. New technique for testing of delay fault in cluster based FPGA. IEEE MWSCAS. 2011; 1–4.
3. Harris IG, Menon PR, Tessier R. BIST-based delay path testing in FPGA architectures. IEEE ITC. 2001; 932–8.
4. Das N, Ghosh S, Rahaman H. Detection of single stuck-at and bridging faults in cluster-based FPGA Architectures. Proc VDAT. 2007; 205–12.

5. Das N, Roy P, Rahama H. On line testing of single feedback bridging fault in cluster based FPGA by using Asynchronous element. IEEE IOLTS. 2008.
6. Girard P, Heron O, Pravossoudovitch S, Renovell M. Delay fault testing of look-up table in SRAM-based FPGA. J Electron Test, Theory Appl. 2005; 21:43–55.
7. Abramovic M, Breuer MA, Friedman AD. Digital system testing and testable design, Wiley-Addison, 1994.
8. Stroud C, Wijesuriya S, Hamilton C. Built-in self test of FPGA interconnect. Int Test Conf. 1998. p. 404–11.
9. Dutt S, Verma V, Suthar V. Build-in-self-test of FPGA with provable diagnos abilities and high diagnostic coverage with application to online testing. IEEE TCAD. 2008; 27:309–26.
10. Abramovici M, Stroud CE. BIST based delay fault testing in FPGA. J Electron Test. 2003; 19:549–58.
11. Lai L, Chen WT, Rinderknecht T. Programmable scan based logic build-in-self-test. 16th IEEE Asian Test Symp. 2007; 371–7.
12. Girard P, Heron O, Pravossoudovitch S, Renovell M. Defect analysis for delay-fault in FPGAs. 9th IEEE IOLTS. 2003; 1–5.
13. Girard P, Heron O, Pravossoudovitch S, Renovell M. An efficient BIST architecture for delay fault in the logic cell of symmetrical ARAM-based FPGAs. J Electron Test, Theory Appl. 2006; 22:161–72.
14. Smith J, Xia T, Stroud C. An automated BIST architecture for testing and diagnosing FPGA Interconnect. J Electron Test. 2006; 22:239–53.
15. Abramovici M, Emmert JM, Stroud CE. Roving STARs: an intregated approach to on-line testing, diagnosis, and fault tolerance for FPGAs in adaptive computing system. Third NASA/DOD Workshop. 2001; 73–92.
16. Das N, Rahaman H, Banerjee I. BIST to diagnosis delay fault in the LUT of cluster based FPGA. IEEE ICNCC. 2011; 252–6.
17. Xilinx Corp: Available from: www.xilinx.com
18. Rahaman H, Mathew J, Pradhan DK. Transition fault testability in bit parallel multipliers over GF(2 m). IEEE VLSI Test Symp. (VTS07), Berkeley, California, USA. 2007 May 6–10; 422–30.
19. Cheng C-K, Liillis J, Lin S, Cheng N. Interconnect analysis and synthesis, Wiley-Interscience, 2000.
20. Chen WY, Gupta SK, Breuer MA. Analytical models for crosstalk exicitation and propagation in VLSI circuits. IEEE TCAD. 2002 Oct; 21:1117–31.
21. Das N, Roy P, Rahaman H. On-line detection of crosstalk fault in FPGA using BIST model. IEEE VDAT. 2011.
22. Abramovici M, Emmert JM, Stroud CE. On-line BIST and BIST-based diagnosis of FPGA logic block. IEEE Tnans VLSI Syst. 2004; 12(12):1284–94.