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Design of Low Power Digital Clock on FPGA using Different IO Standards

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Abstract

Objective: This paper analyzes the power of a digital clock with the help of Xilinx ISE V-14.2 and executing it on virtex-6 FPGA and Spartan 3E FPGA. **Methods:** On FPGA we use Verilog HDL to synthesize the clock where the targeted device is FPGA. Analysis of different IO Standard on Xilinx software depicts the least power consumption for 2 different frequencies. **Findings:** With the results portrayed in the paper we get a combination of perfect low power consuming IC design. Xilinx XPower analyzer has been used to analyze the power consumption of digital clock based on FPGA. Further power utilization using different IO standards at different frequency has been decreased effectively. The device when operating at 50 Mega Hertz and 100 Mega Hertz frequency the reduction of power is attained. **Application:** This low power consuming IC design will be useful wherever digital clock is used and energy efficiency is to be attained.

Keywords: Digital Clock, Energy Efficiency, FPGA, IO Standards, Low Power Design, Power Consumption

1. Introduction

A field-programmable gate array is an IC designed for use by designer or customer after its manufacture- therefore called as "field-programmable" also known as FPGA. The FPGA arrangement, generally specified using HDL similar to the one used for the application specific IC (ASIC) (to specify the configuration circuit diagrams were used previously, as they were for ASICs, but this is rare now). We use Digital clock to display the time digitally. Earlier, the power analysis was done by using hardware components which was very complex. If any component is not working or is to be changed in circuitry whole circuit is to be replaced. This problem got resolved by software analysis of power using Xilinx ISE 14.2 XPower analyzer. With the help of XPower analyzer we can change the value of different components such as capacitance, current, voltage, temperature. We are calculating the power at different frequency using different IO standard. We are calculating the least power of digital clock as shown in Figure 1. There are many different ways of calculating the power analysis in Xilinx software such as plan ahead, where we can change drive strength and calculate power and see the reduction in power.

In Figure 2, the graph indicates the variation in power at frequency 50MHz for different Iostandards.

In Figure 3, the graph indicates the variation in power at frequency 100MHz for different IOstandards at Virtex-6 FPGA. Minimum power on Virtex-6 FPGA is for IOstandard LVCMOS12 at a frequency 50MHz which is 0.713 W.

In Figure 4, the variation in power on Spartan 3E FPGA at frequency 50MHz for different IOstandards than Virtex-6. The minimum power calculated is at LVCMOS25 at frequency 50MHz which is 0.080W.

Table 1 represent the power consumption by digital clock in Spartan 3E FPGA at frequency 50MHz using different IO standards. We have used different IO standard in Spartan 3E than in Virtex-6 and calculated the power consumed.

2. Related Work

In Verilog Hardware Description Language, a simple architecture is implemented[1]. Xilinx ISE Simulator Tool has been used to simulate the present algorithm and is implemented in Verilog HDL[2]. FPGA control has been

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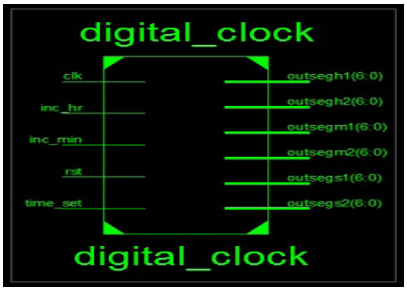

Figure 1. RTL schematic of FPGA.

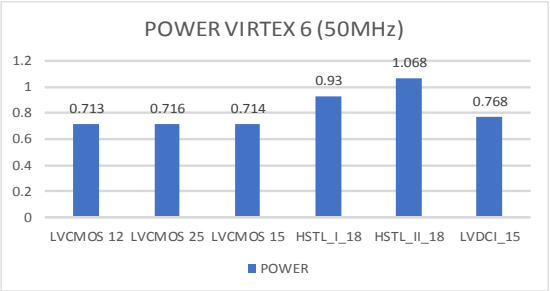

Figure 2. Power dissipation on Virtex-6 FPGA for 50 MHz.

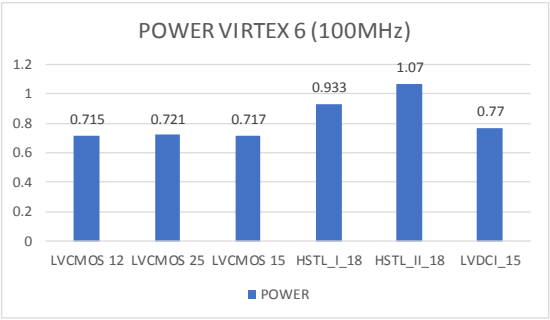

Figure 3. Power dissipation on Virtex-6 FPGA for 100 MHz.

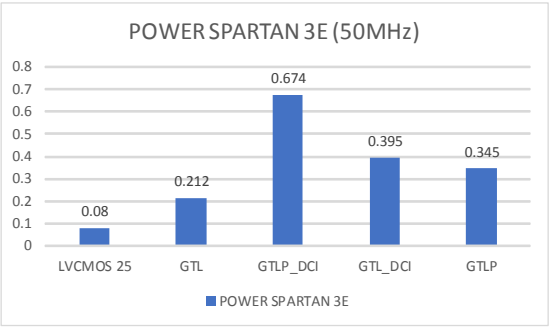

Figure 4. Power dissipation on Spartan 3E FPGA for 50MHz.

Table 1. IO standards used in spartan3E

IOSTANDARD	50MHz
LVCMOS25	0.080W
GTL	0.212W
GTLP_DCI	0.674W
GTL_DCI	0.395W
GTLP	0.345W

used to validate the theoretical and simulation results[3]. As execution of digital clock undergoes HDL, we have selected Xilinx platform also it is quite simpler and takes less time. Moreover, there isn't any need to make unique program set for FPGA unlike other methods[4]. Power dissipation factor depends on supply voltage, frequency of operation and load capacitance[5]. Power is analyzed with variation in frequency and change in IO standards[6]. For processing logics FPGA uses hardware as it does not have an operating system[7].

3. Methodology

While calculating the power we are creating a User Constraints File (UCF) file which plays an important role is defining the IOstandards and is playing an important part in analyzing the power of a digital clock. The power of digital clock in Virtex-6 is calculated at 6 different IOstandards mentioned in Table 2 at 2 different frequencies.

4. Results

Power consumption factor would be discussed here. Table 3 signifies the power consumed in watts (w) by clock, logic, signals and IO's. Statements used for implementing a digital clock is defined as logic. Power consumed by Virtex 6 field programming would be discussed below:

Table 3 signifies the power consumption by logic, clock, IOs and signals. Here the total logic used is given by the User while available signifies the total logic available in Xilinx and total utilized logic percentage is given by utilizations. The total power at LVCMOS12 is 0.715W.

In Table 4, we compare the total power consumed at a Frequency of 50MHz at IOstandard LVCMOS25. The total power at LVCMOS25 is 0.721W.

Now we can see the IO standard is changed to LVCMOS15. The power consumed will be 0.717W as shown in Table 5.

Table 2. IO standard used in Virtex-6

IO standards	100MHz	50MHz
LVCMOS12	0.713W	0.715W
LVCMOS25	0.716W	0.721W
LVCMOS15	0.714W	0.717W
HSTL_I_18	0.930W	0.933W
HSTL_II_18	1.068W	1.070W
LVDCI_15	0.768W	0.770W

Table 3. When Frequency=50MHz and IOstandard= LVCMOS12

On-chip	Available	Utilization	Used	Power(w)
signals	_	_	154	0.000
logic	46560	0.2	114	0.000
clock	_	_	2	0.003
IOs	240	19.6	47	0.002

Table 4. When Frequency=50MHz and IOstandard=LVCMOS25

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
logic	46560	0.2	114	0.000
Clock	_	_	2	0.003
IOs	240	19.6	47	0.006

Table 5. When Frequency=50MHz and IOstandard= LVCMOS15

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.003
IOs	240	19.6	47	0.003

Now we are vary the IOstandard to attain the low power consumption level in digital clock. The power consumption at IO standard HSTL_I_18 is 0.933W as shown in Table 6.

By changing the IOstandard to HSTL_II_18, we observe that value of power consumption is increased to 1.070W as shown in Table 7.

In Table 8, we compare the power consumed at frequency 50MHz at IOstandard LVDCI_15. Power consumed comes out to be 0.770W.

In Table 9, we change the frequency to 100MHz and draw a comparison between the power consumption at

Table 6. When Frequency=50MHz and IOstandard= HSTL_I_18

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.003
IOs	240	19.6	47	0.214

Table 7. When Frequency=50MHz and IOstandard= HSTL_II_18

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.003
IOs	240	19.6	47	0.214

Table 8. When Frequency=50MHz and IOstandard= LVDCI_15

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.003
IOs	240	19.6	47	0.055

Table 9. When Frequency=100MHz and LVCMOS12

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.001
IOs	240	19.6	47	0.001

different IOstandards. The power consumed at IOstandard LVCMOS12 is 0.713W.

We are changing the IOstandard to LVCMOS25 to see the change in power consumption i.e. 0.716W as shown in Table 10.

At IOstandard LVCMOS15 the power consumption decreases than with LVCMOS25 i.e. 0.714W as shown in Table 11.

In Tables 12 and 13, we are comparing the power consumption increases from 0.930W to 1.069W.

In Table 14 the power consumed at IOstandard LVDCI_15 is 0.768W. Thus, in Virtex-6 the best frequency at which digital clock functions is 100MHz and IOstandard is LVCMOS12.

Table 10. When Frequency=100MHz and IOstandard= LVCMOS25

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.001
IOs	240	19.6	47	0.003

Table 11. When Frequency=100MHz and IOstandard= LVCMOS15

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.001
IOs	240	19.6	47	0.001

Table 12. When frequency= 100MHz and IOstandard= HSTL_I_18

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	**154**	**0.000**
Logic	**46560**	**0.2**	**114**	**0.000**
Clock	_	_	**2**	**0.003**
IOs	**240**	**19.6**	**47**	**0.213**

Table 13. When frequency=100MHz and IOstandard= HSTL_II_18

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.003
IOs	240	19.6	47	0.347

Table 14. When frequency= 100MHz and IOstandard= LVDCI_15

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	154	0.000
Logic	46560	0.2	114	0.000
Clock	_	_	2	0.001
IOs	240	19.6	147	0.054

Secondly, we will use Spartan 3E at different IOstandards than in used in Virtex-6 at a single frequency which is 50MHz.

The power consumed by using IOstandard LVCMOS25 is 0.080W displayed in Table 15.

The power consumed by using IOstandard GTL has been increased to 0.212W as shown in Table 16.

The power consumption got increased by using IOstandard GTLP_DCI i.e. 0.674W as shown in Table 17.

The power consumption decreased to 0.395W as shown in Table 18.

Table 15. When frequency = 50MHz and IOstandard= LVCMOS25

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	263	0.001
Logic	1536	16.9	259	0.001
Clock	_	_	2	0.001
IOs	124	37.9	47	0.050

Table 16. When frequency = 50MHz and IOstandard= GTL

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	263	0.001
Logic	1536	16.9	259	0.001
Clock	_	_	2	0.001
IOs	124	37.9	47	0.183

Table 17. When frequency = 50MHz and IOstandard= GTLP_DCI

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	263	0.001
Logic	1536	16.9	259	0.001
Clock	_	_	2	0.001
IOs	124	37.9	47	0.643

Table 18. When frequency = 50MHz and IOstandard= GTL_DCI

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	263	0.001
Logic	1536	16.9	259	0.001
Clock	_	_	2	0.001
IOs	124	37.9	47	0.366

Table 19. When frequency = 50MHz and IOstandard= GTLP

On-chip	Available	Utilization	Used	Power(w)
Signals	_	_	263	0.001
Logic	1536	16.9	259	0.001
Clock	_	_	2	0.001
IOs	124	37.9	47	0.315

Now in Table 19 the power consumption decreased to 0.345W.

The least power consumption in Spartan 3E at 50MHz is 0.080W at IOstandard LVCMOS25.

5. Conclusion

The least power utilization of digital clock at different IO standards and at different FPGA has been confirmed using XPower analyzer. Design has been tested at 50MHz, 100MHz for Virtex-6 FPGA at different IOstandards and 50MHz at Spartan 3E FPGA at different FPGA. Changing the IOstandards results in decrease in IOs power.

6. Future Scope

Virtex-6 Field Programmable Gate Array is the device targeted in this paper. The outcome of this design on power consumption can be re-investigate on 45-nm Spartan-6. The Performance, Power and Design productivity can be redefined with latest innovative 28nm FPGA Artix-7, and Virtex-7 and Kintex-7 and future 16nm Ultra Scale FPGA. Application of these techniques on large circuits have more scope.

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