

Design and Simulation of a Multi-channel Neural Recording Microsystem with Inductive Power Telemetry Link

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Abstract

Neural micro-probing not only allows us to access the brain signals, it is also one of the key tools to achieve a better understanding of the fundamental mechanisms of the brain and nervous system. This knowledge is extremely essential to implement complex neural prosthetics. Considering the importance of the size, power consumption, and accuracy, in this Paper, a compact, low-power eight-channel implantable neural recording microsystem is presented. To this end, Time Division Multiplexing (TDM) method is used for multiplexing 8 input channels. Thus, only one Analog to Digital Converter (ADC) block is used, resulting in a small circuit size and low power consumption. Also, a new structure of Amplitude-Shift Keying (ASK) modulation technique with simple configuration and low power consumption is proposed and applied. This system is designed in TSMC 0.18 μm CMOS technology with 1.8 V power supply and simulated with HSPICE. The total power consumption of the system is measured to 2 mW. Neural signals recorded from auditory cortex of a guinea pig are used as the inputs of the eight channels of the system. Total RMS error between inputs and outputs caused by the system is 2.8%.

Keywords: ASK Modulation, Implantable Microsystems, Multichannel Neural Recording, Time Division Multiplexing

1. Introduction

Neural microprobes are among the most useful technologies to understand the fundamental mechanisms of the brain at a cellular level and are one of the key tools that are used by neuroscientists, nowadays. Accordingly, microelectrode arrays and multi-channel neural recording systems have been developed in recent years ¹⁻⁶. Due to the large number of recording channels, these systems naturally produce a huge amount of data that should be transmitted out of the body to be further processed or analyzed ⁷⁻¹⁰. However, in order to increase the number of channels, circuits with higher speed and data rates are required ¹¹. Spike detection methods are another approach to decrease the required data capacity while increasing

the number of channels ¹²⁻¹⁴. However, in some applications, recording and transmitting detailed neural signals, is desirable, where low power circuits with high data rate are required. This is especially the case when wireless power transmission is desirable. Depending on the requirements, different methods of power supplying of the implantable micro-systems might be used, and each method has its own advantages and disadvantages. For instance, despite simplicity, power supplying by battery limits the system performance (due to the limited energy density and short lifetime of batteries). Rechargeable batteries also have large sizes and more importantly they are bio-incompatible^{14,15}. So, wireless power transferring was proposed and used in ^{16,17}. The most commonly-used method for wireless transfer¹⁸ of power and data to biomedical implantable

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microsystems is based on inductive coupling between two mutually-coupled coils: the primary coil, which is on the external side and transmits the Radio Frequency (RF) power, and the secondary coil which is on the implantable side and receives the RF energy¹⁴. In implantable recording microsystems, size, power consumption and accuracy are important factors. Especially in multi-channel neural recording designing a microsystem with compact size and low power consumption is very challenging. In order to address these issues, in this paper an eight-channel implantable neural recording microsystem is designed in which TDM technique and power transferring via inductive link is used. A new ASK modulator with low power consumption is presented and used in the system that is suitable for power telemetry.

2. System Description

The block diagram of the proposed neural recording microsystem is depicted in Figure 1. All inputs of the channels are analog signals with a bandwidth less than 10 KHz. Thus, based on the Nyquist sampling theorem, the minimum sampling rate of each channel should be at least 20 KHz. Therefore, the clock frequency of the

Analog Time Division Multiplexer (ATDM) is 160 KHz to be multiplexed between eight channels. Output signals of the TDM are then digitalized by a 10-bit Analog to Digital convertor (A/D). The pipeline outputs of the A/D are passed to the data packer block to packaging these data with five start bits and one parity bit. In this configuration, when the load signal goes high the data packer loads a Parallel-In Serial-Out shift register (PISO) and data packets are sent serially to the ASK modulator block with a 2.56 MHz clock. A 10 MHz clock frequency is selected for ASK modulator. It is worth mentioning that a clock signal with higher frequency for the demodulation of the received signal in the receiver side provides higher level of simplicity in the demodulation and also in achieving a more accurate output signal. However, an increase in the modulation frequency results in more power loss. So, medium frequency is applied to compromise between the accuracy and power consumption. Apparently, two clock frequencies are required for different sections of the system; one at 160 KHz and the other one at 2.56 MHz. These signals are generated in the clock generator block. This block also provides the load signal for the data packer when transmission of each packet is completed. Power supply for the system is provided with external setup and transfer to the implant part via inductive link.

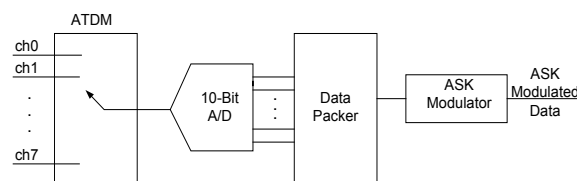


Figure 1. The block diagram of the presented 8-channel neural recording microsystem.

3. Circuit Level Design of the multichannel Neural Recording System

In this section, circuit implementation of each block of the proposed system is presented. First, two general blocks are described; clock generator and power source. Then other blocks, namely the time division multiplexer, data packer, and ASK modulator blocks shown in Figure 1, are explained, respectively.

3.1 Clock Generator

As explained in the previous section, two different clock signals are required in the system. *clk1* for ATDM and ADC, and *CLK* for data packer. *clk1* is a 160 KHz pulse, while the frequency of *CLK* signal is 16 times greater than *clk1*, i.e. 2.56 MHz. Both of the clock signals should be non-overlapped with their complementary signals. Figures 2a, and 2b show the circuit implementation for generating both the *CLK* and *clk1* and their non-overlapping complementary. The circuit shown in Figure 2c generates the load signal required for the data packer.

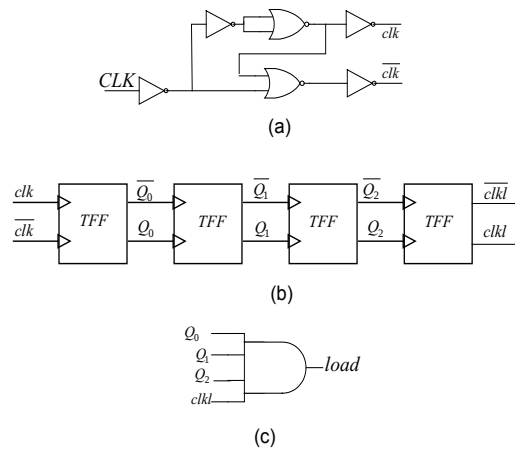


Figure 2. (a,b) the circuit implementation for generating both clk and $\overline{clk}$ and their non-overlapping complementary. (c) the load signal needed for data packer.

3.2 DC Power Source

In order to have a fully implantable system, power should be wirelessly transferred to the implanted part. So, as shown in Figure 3 the required power for all parts of the system is provided in external side (in AC) and is transferred to the implanted side via an inductive telemetric link (L_{tank} , C_{tank}). After receiving the power signal through

the LC tank, it is rectified and regulated¹⁹. Capacitance C_s eliminates the large ripples of the output signal of the rectifier, and at the output of the regulator an acceptable 1.8 VDC signal is achieved. In applications where a DC voltage with less ripple is required, the output of this circuit can be sent to V_{GS} reference voltage regulator.

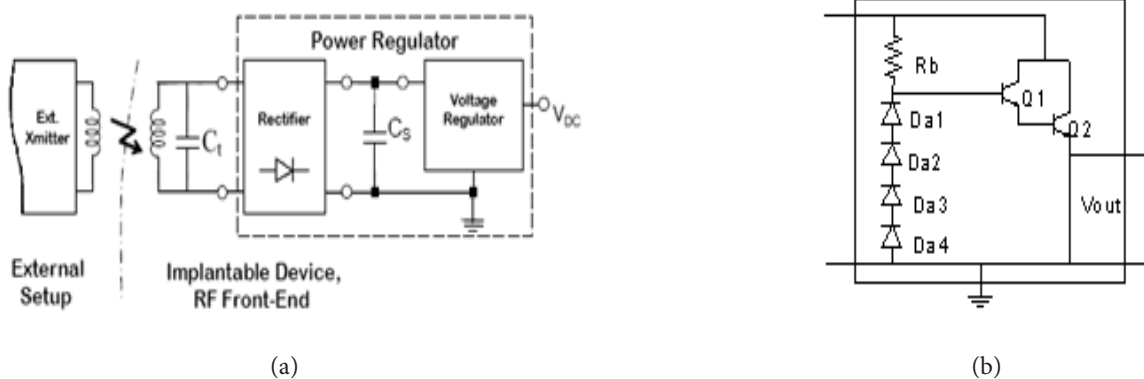


Figure 3. (a) The block diagram of the DC power source and (b) the circuit of the voltage regulator.

3.3 Time Division Multiplexer

This block is an analog multiplexer that successively multiplexes between eight neural channels²⁰. The schematic of this block in circuit level is shown in Figure 4. The designed 8-channel ATDM is composed of a 3-bit counter, eight 4-input NAND gates and eight transmis-

sion gates. The outputs of a 3-bit counter are used as the selection inputs of the multiplexer to determine the output channel. As mentioned in the previous section the sampling rate of each channel should be at least 20 KHz. Therefore, the clock frequency of the ATDM, which is multiplexed between eight channels, is 160 KHz.

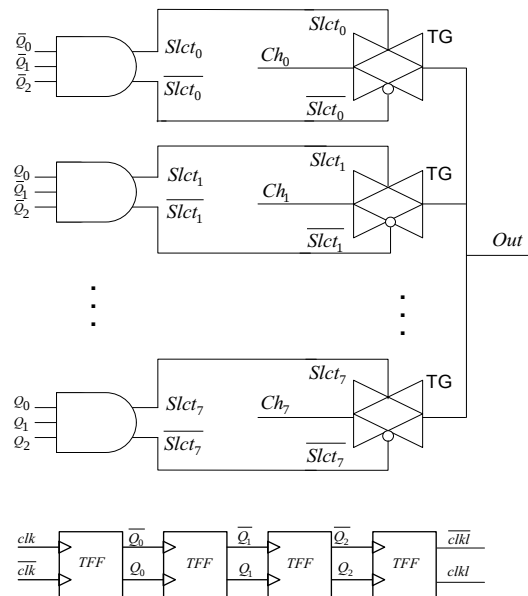


Figure 4. Implementaion of 8-channel ATDM by a 3-bit counter, NAND gates and taransmission gates.

3.4 Data Packer

Figure 5 depicts the circuit diagram of the data packer. In each cycle of the clk , a 10-bit digital word, which is produced by the ADC block, enters to the data packer. Each packet consists of 16-bit: five start bits, 10 data bits and a parity bit. When the load signal goes high, this

packet is loaded to a parallel-in serial-out shift register and by each clock cycle, one shift occurs in PISO so that the data goes out serially. The serial output of the PISO is the inputs of the ASK modulator block.

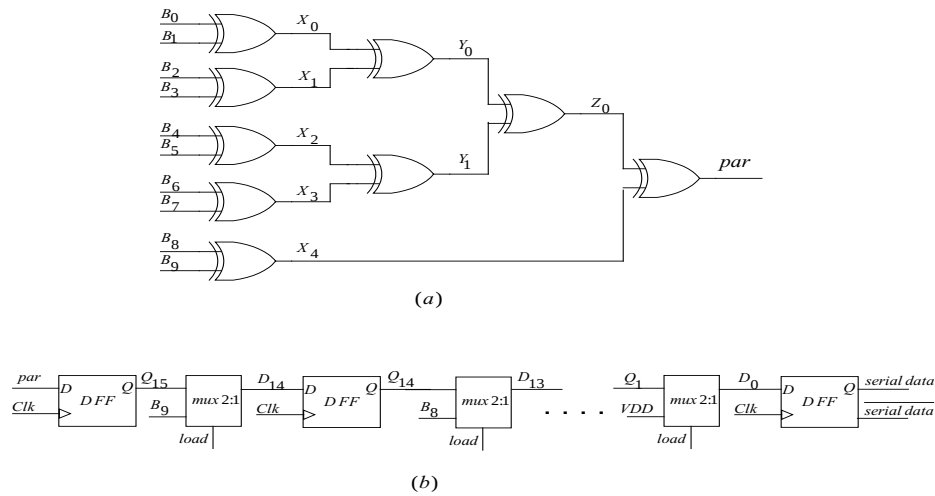


Figure 5. circuit diagram of the (a) parity generator and (b) data packer..

3.5 ASK Modulator

ASK technique in modulator is more susceptible to noise and disturbances rather than FSK and PSK. This is because noise and disturbances directly affect the amplitude of the signal²¹. Despite this disadvantage, ASK is a widely used modulation scheme due to its simple configuration and subsequently its low power consumption. These are important features in the design of implantable devices^{22–24}. Thus, an ASK modulator, which benefits from a simple circuit and low power consumption is used in this paper.

The supply voltage of the circuit is 1.8V. Thus, low-voltage level (logic 0) and high-voltage level (logic 1) of the ASK modulated signals should be take values between ground (0 V) and 1.8 V. To this end, the ASK modulator shown in Figure 6 is proposed. In this circuit, signals *osc* and $\overline{osc}$ are outputs of a ring oscillator. The amplitude of the ring oscillator's outputs varies between 0 and 1.8V. A DC level shifter is used to reduce the peak amplitude of the *osc*, so that it oscillates with an amplitude of 1.1 V. Based on the value of the input data, either *osc* signal (i.e. 1.8 V) or its reduced amplitude (i.e. 1.1 V), is selected by complementary switches to appear at the output pin of the ASK modulator. With this procedure, ASK modulation is performed.

It is worth mentioning that, in order to further decrease the power consumption of the ASK circuit, another diode connected MOSFET can be added below M3 so that the low-voltage level (logic 0) of ASK modulation decreases to 0.7 V. This also results in an easier demodulation in receiver side.

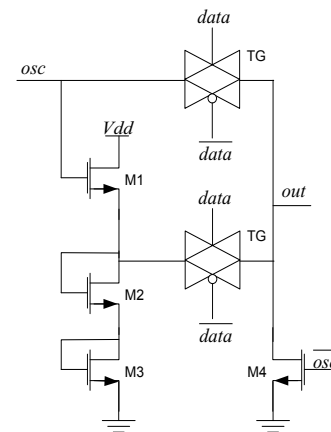


Figure 6. A circuit diagram for ASK modulator.

4. Simulatoin Results

Different blocks of the microsystem are designed using TSMC 0.18 μ m CMOS. Each block is designed as a subcircuit and simulated separately. The simulations are carried out with Hspice software.

Figure 7 shows the output of the 1.8 V DC power supply. As it is seen, the ripple of the DC voltage is very small. The simulation results show a peak-to-peak voltage ripple of 2.1mV. One sample output waveform of ATDM is depicted in Figure 8. In order to test the block, eight DC voltages are used as the inputs of the eight channels. As it is seen in Figure 8. In each clock cycle one of the inputs is selected sequentially. Figure 9 is the serial output bits of the data packer under condition of constant inputs. These inputs are: 1.8, 1.8, 0, 0, 0, 1.8, 0, 0, 1.8, 0. So, as it

is seen in Figure 9 the output packet consists of five start bits (equal to 1.8 v), inputs, and the parity bit. The output is checked based on multiple inputs and accuracy of this block is approved. Figure 10 shows the waveform of the modulated output of the ASK modulator block. In order to test this block a pulse signal is used. As it is seen, the pulse signal is modulated in two levels; 1.8 V and 1.1 V. The final outputs tested of the system is also shown in Figure 11. The simulation results approve the correct and accurate functionality of all the blocks. The microsystem is built with these blocks. The output waveform of the system, which is demodulated in Matlab and is compared with the input, shows the RMS error of 2.8%. The average power consumption of the system in Hspice simulation is 2mW. This is the total power that the entire blocks of the system take from DC power supply (V_{DC}).

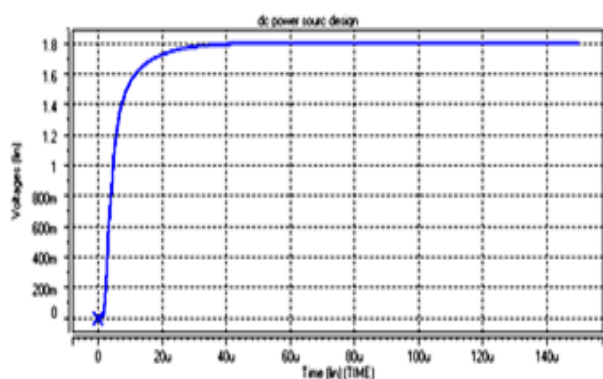


Figure 7. The output of DC power source, 1.8v DC voltage.

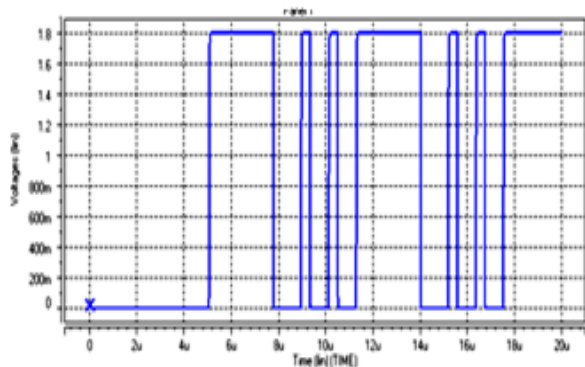


Figure 9. The serially output bits of data packer.

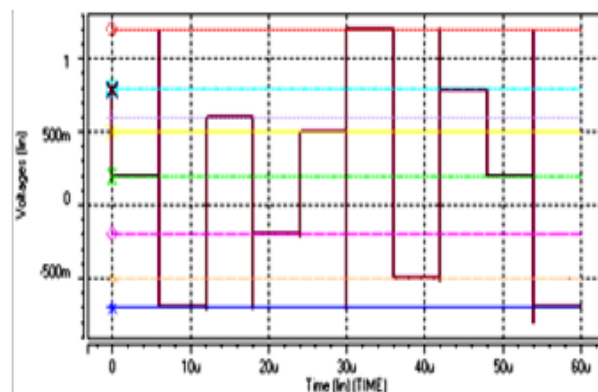


Figure 8. The output of ATDM, inputs are DC signals.

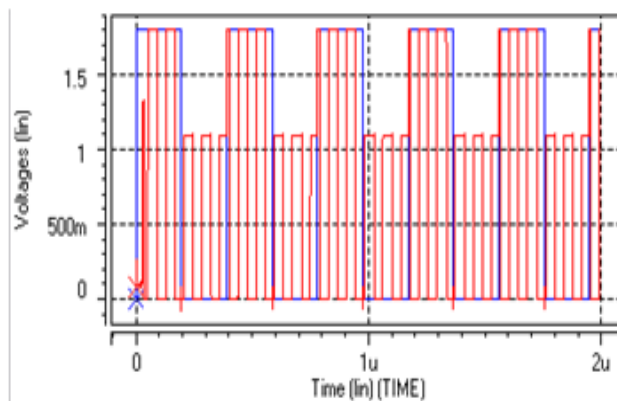


Figure 10. The output waveform of ASK modulator.

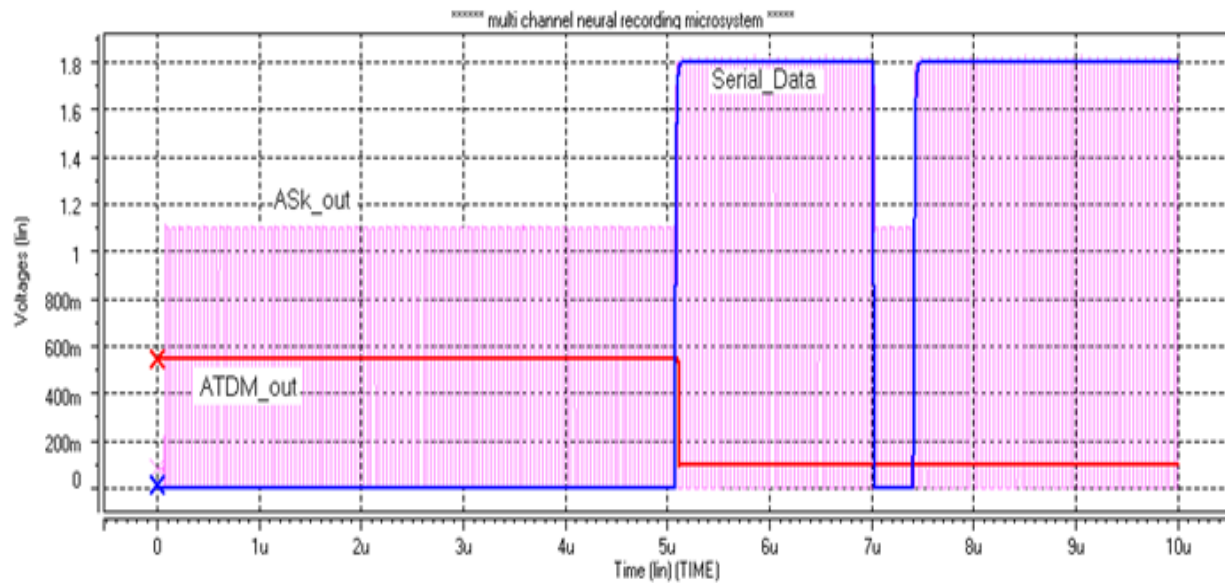


Figure 11. The final outputs of the tested system.

5. Conclusion

This paper presents a low power multi-channel neural recording microsystem. The input signals of this system are eight neural recorded signals from auditory cortex of a guinea pig. The bandwidth of each channel is 10 KHz. Input channels are multiplexed by an ATDM with a 160 KHz clock signal (20 KHz sampling rate for each channel based on Nyquist theorem). A 10-bit pipeline A/D, a data packer for packaging the data in 16-bit and an ASK modulator for modulating the serial data are used. This implantable microsystem is designed using TSMC 0.18 μ m CMOS technology and simulated with HSpice. The total power consumption of the system is estimated to be 2 mW. Decreasing the level of the signal in the ASK modulator can result in even lower power consumption.

6. References

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