Indian Journal of Science and Technology, Vol 9(13), DOI: 10.17485/ijst/2016/v9i13/87911, April 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Design of Prefix Adder Amalgamation Reversible Logic Gates using 16 Bit Kogge Stone Adder

P. Michael Preetam Raj, Bhaskaruni Sandeep*, D. Sai Mallik Reddy, P. Ramanjaneyulu and Sakhamuri Sai Pravallika

Department of Electronics and Communication Engineering, KL University, Guntur - 522502, Andhra Pradesh, India; michael7@kluniversity.in, sndpbhaskaruni@gmail.com, saimallikd.reddy@gmail.com, yamilittlestar9999@gmail.com, s.saipravallika96@gmail.com

Abstract

Objective: VLSI integer adders are critical elements in general purposed DSP and DSPA processors. These used in design of ALU, floating point arithmetic data paths and address generation units. Parallel prefix adders rely on simple cell design. Modern FPGAs utilize fast carry chain for optimization ripple carry adder. **Methods/Analysis**: Design of the delay models and cost analysis by VLSI embedded system is done in this paper. Prefix adder with reversible logic gates utilizing 16 bit kogge stone adder have been design using PERES logic. **Findings**: Methodology is based on the fact that a parallel prefix adder can be represented as a graph consists of carry operator nodes. The adder structure has minimum logic depth and binary tree structure with minimum fan-out. From the simulate results this is formed that computational path net delay for 16 X16 bit prefix adder using reversible logic is 20.828 ns with Kogge Stone Adder is reading to 17.247ns. **Novelty/ Improvement**: The multiple based on 16 bit Kogge Stone Adder is formed to be less efficient than the case of reversible adder in term of delay and power analysis.

Keywords: Kogge Stone Adder, Logic Gates, Prefix Adder, Peres Gate, Reversible Logic Gate

1. Introduction

A large amount of the research and development endeavors in the area of digital electronics have been utilized towards increasing the speed and complexity of single chip digital systems[1]. However by drastic changes power consumption of individual components is resulting to reduce the device reliabilities. Now a day's power is rapidly becoming one of the most important issues in digital system design. The power consumption is indispensable in the areas of communication, consumer electronics etc. The elevated operation speed and the tremendous action on the adder circuits in recent microprocessors, leads toward high power utilization. The existence of several implementation engines in present processors extra aggravates the problems. VLSI integer adders are significant elements in common purpose and DSPA processors at the same time as they are utilize in the design of ALU, in floating points, arithmetic data paths, and during address generation units. Parallel prefix adders are proper for VLSI accomplishment given that they rely on the utilize of simple cells and maintain regular connections between them. In designated, most present FPGAs utilize a fast carry sequence which optimizes the carry path for the simple Ripple Carry Adder (RCA)[2]. This paper proposed design reduces the power consumption and cost analysis for development of VLSI, Embedded Systems in real time technology. Analyzing the prefix adder amalgamation reversible logic gates using 16 bit kogge stone adder in FPGA, DSPA are designed.

2. BackGround and Mechanism of PPA and RLG

2.1 Parallel Prefix Adder Mechanism

The field of inversion is shown in Figure 1. Kogge Stone proposed the parallel prefix adder for low fan-out and high logic[3]. Brent Kung adder design smallest number of scheming nodes[4], Han-Carlson adder is design between

*Author for correspondence

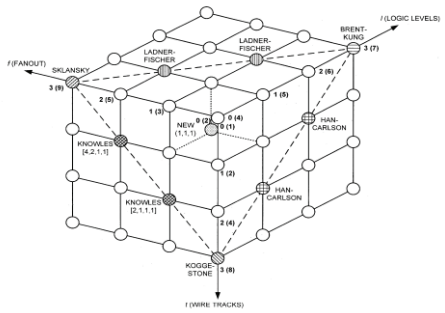


Figure 1. Field of inversion.

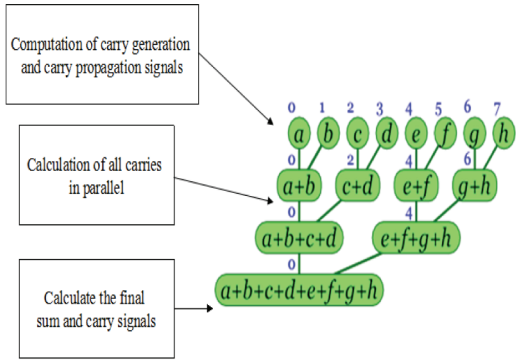


Figure 2. Parallel prefix adder mechanism.

nodal count low logic depth[5] and improved fan-out. Author[6] developed an interconnecting node topology. Authors[7] proposed a general design high depth parallel prefix network[7]. In[8] proposed minimum delay parallel prefix area for logarithmic adder for fan-out[8]. Some more adders are designed by[9] to being minimal depth form-inimal depth for n-bit adder[9]. The Figure 2 showing the mechanism for parallel prefix adder Table 1.

Table 1. Compares some of the parallel prefix networks under consideration

Architecture	Classification	Logic Levels	Max Fanout	Tracks	Cols
Brent-Kung	(M-1, 0, 0)	M + (M – 1)	2	1	L/2
Sklansky	(0, M-1, 0)	M	L/2 + 1	1	L
Kogge-Stone	(0, 0, M-1)	M	2	L/2	L
Han-Carlson	(1, 0, M-2)	M + 1	2	L/4	L/2
Knowles [2,1, . . ., 1]	(0, 1, M-2)	M	3	L/4	L
Ladner-Fischer	(M-2, 1, 0)	M + (M – 2)	3	1	L/2
Ladner-Fischer	(1, M-2, 0)	M + 1	L/4 + 1	1	L/2
Ladner-Fischer + helpers	(1, M-2, 0)	M + 1	L/4 + 1 + helpers	2	L/2
(1, 1, M-3)	(1, 1, M-3)	M + 1	3	L/8	L/2

2.2 Reversible Logic Gate

In[10] proposed energy dissipation circuit for reversible quantum operations are reversible. They are many designed have been proposed to ensured implementing any Boolean function using RLG[10], such as Feynman gate, NFT gate, ISLAM gate represented in Figure 3.
Condition for implementation of RLG

- Number of inputs should be equal to the number of outputs.
- For Every input pattern should be a unique output pattern.
- A piece output will be used only once, no fan out is allowed.

The main aim of using RL namely significantly to reduced heat dissipation and power consumptions apprehend in a sustainable approach[11,12].

3. Methodology

To propose the adders pedestal on FPGA and DSPA, procedure is to cram the adder with their benefits and limitations. Making design on verilog code. Realization and synthesis are done on the Xilinx ISE Design Suit. After synthesisation the simulation results are

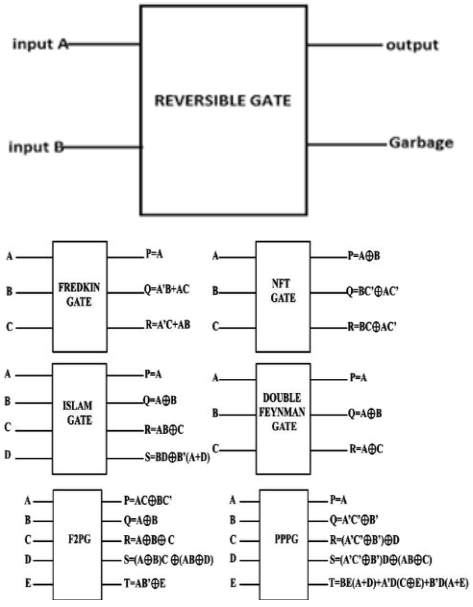


Figure 3. Reversible gate and different types of reversible logic gates.

synchronized. Software used Xilinx ISE Design Suit 14.7, ISIM simulator.

A PPA can be represented as a PPG consisting of carry operator nodes. This adder configuration has minimum logic depth, and full binary tree with minimum fun-out, resulting in a fast adder but with a large area.

4. Proposed High Speed 16 bit Kogge Stone Adder using Prefix Adder Reversible PERES Logic Gates

The proposed high speed 16 bit KSA using prefix adder RLG is shown Figure 6. Main premise of the design is to abolish enormous delays in overall for carry computations. So the depth logicis put forward to design is optimum. Designing 16 bit prefix reversible adder by using logic gates has been realizethrough the help of CMOS logic be appropriate in FPGAS and DSP,common logic constructs are only inverter functions, so that cascading odd cells and even cells provide the results of abolish inverts between those two cells. Two inputs of each stages will be given to XOR gate and AND gate such that it appears as half adder circuit. But by using the XOR and AND gate the time delay and power consumption are more. For this by removing both the gates (XOR and AND) are Kogge Stone Adder. Replacing with reversible logic gates like PERES GATE, applying this gate to reduce both time delay and power consumption as shown in Table 2. The topology of the design is uncomplicated to reduce impedance matching. The finishing stage of the design gives the computational signal as one output and carry signal as other output as represented in Figure 5 and Figure 6. This can overcome various problems in existed adders taking the two conditions C_{in} = 0 and C_{in}= 1 shown in Figure 7 and Figure 8.

Table 2. Power consumption for 16 bit Kogge Stone Adder and 16 bit reversible Kogge Stone Adder

Name of the Adder	Area	Delay (pico seconds)	Power (nW)
Kogge Stone Adder	786686	2389	37086958.406
Reversible Kogge Stone Adder	786688	2060	33932884.418

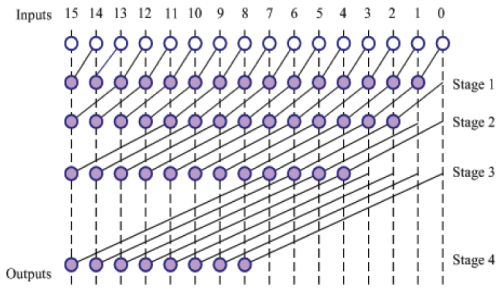
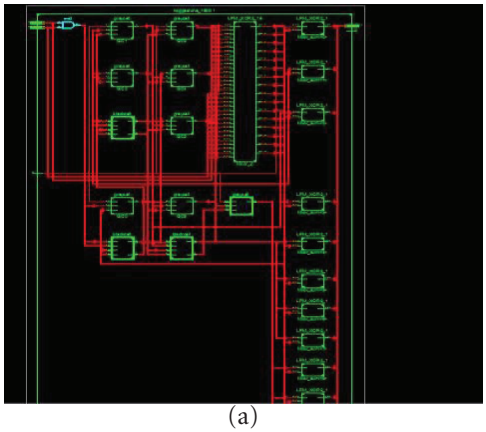
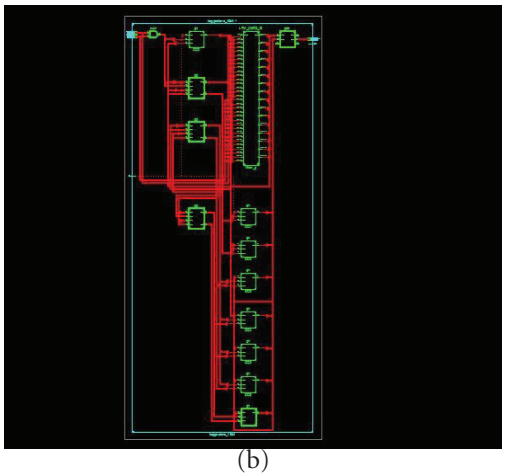


Figure 4. 16-bit Kogge-Stone adder.



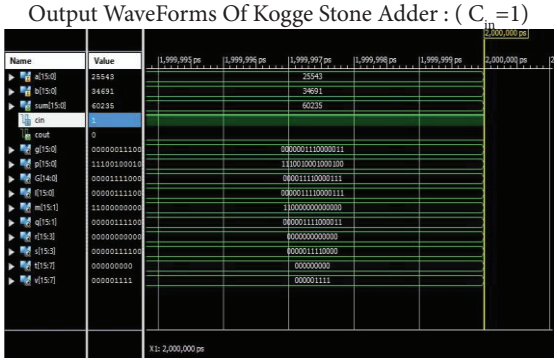
(a)



(b)

Figure 5. RTL schematic layout of Kogge Stone adder using Xilinx. **(a)** Representing the generation and propagation of the16 bit kogge stone adder. **(b)** In the reversible Kogge Stone adder we have Removed " And " and "ex-or" gates are removed and Peres Gate is included as reversible logic gate The Grey cells represent both generation and propagation of reversible Kogge Stone Adder.

Output WaveForms Of Kogge Stone Adder : (C_{in}=1)



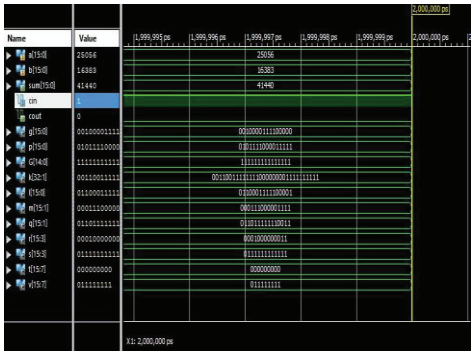
In the Kogge Stone Adder If the C_{in} = 1 then the output has carry 1 then we get the value with adding "1" to the original output and time taken to run this x1 = 2,000,000 ps.

Output Wave forms of Kogge Stone Adder : (C_{in} = 0)

In the same way if the C_{in} = 0 then the ouput has carry 0 then we get the original value where as for this time taken was increased x1 = 3,000,000 Ps

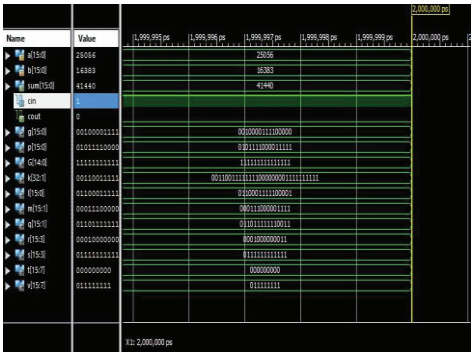
Figure 6. Representing Output Wave Forms Of Kogge Stone Adder (C_{in} = 1), (C_{in} = 0).

Output WaveForms of Reversible Kogge Stone Adder : (C_{in} = 0)



In the Reversible Kogge Stone Adder we taken C_{in}=0 then the output has Carry 0 so that the output time taken to run is X1=1,001,701 ps in the Kogge Stone adder the x1 value in C_{in}=0 was high compared to reversible kogge stone adder

Output WaveForms of Reversible Kogge Stone Adder :(C_{in}=1)



In the Reversible Kogge Stone Adder If the C_{in}=1 then the output has carry 1 then we get the value with adding "1" to the original output and time taken to run this x1=2,000,000 ps.

Figure 7. Representing Output Wave Forms of ReversibleKogge Stone Adder (C_{in}=1), (C_{in}=0)

```
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O             6   1.218   0.844  a_1_IBUF (a_1_IBUF)
 LUT2:I0->O            3   0.704   0.566  BC1/P11 (N01)
 LUT4:I2->O            2   0.704   0.451  GC1/G1 (q<1>)
 LUT4:I3->O            1   0.704   0.455  GC5/G_SW1 (N47)
 LUT4:I2->O            2   0.704   0.482  GC5/G (s<5>)
 LUT3:I2->O            1   0.704   0.595  GC9/G13_SW0_SW1 (N55)
 LUT4:I0->O            2   0.704   0.526  GC9/G13 (GC9/G13)
 LUT2:I1->O            1   0.704   0.424  GC9/G17 (v<9>)
 LUT4:I3->O            1   0.704   0.499  GC13/G8 (GC13/G8)
 LUT4:I1->O            1   0.704   0.455  GC13/G23 (v<13>)
 LUT3:I2->O            1   0.704   0.420  j15/Mxor_q_Result1 (sum_14_OBUF)
 OBUF:I->O                 3.272          sum_14_OBUF (sum<14>)
----------------------------------------
Total                     17.247ns (11.530ns logic, 5.717ns route)
                                   (66.9% logic, 33.1% route)
```

(a)

```
                          Gate     Net
Cell:in->out      fanout  Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O             2   1.218   0.622  B_0_IBUF (B_0_IBUF)
 LUT3:I0->O            2   0.704   0.526  ir1c1/pgo1 (r2c1)
 LUT3:I1->O            2   0.704   0.526  ixor16/Mxor_S_Result<2>11 (N3)
 LUT3:I1->O            2   0.704   0.526  ir2c3/pgo1 (r3c3)
 LUT3:I1->O            2   0.704   0.526  ixor16/Mxor_S_Result<4>11 (N4)
 LUT3:I1->O            2   0.704   0.526  ir5c5/pgo1 (r6c5)
 LUT3:I1->O            3   0.704   0.535  ixor16/Mxor_S_Result<6>11 (N5)
 LUT4:I3->O            1   0.704   0.424  ir6c11/pgo41 (ir6c11/pgo41)
 LUT4:I3->O            1   0.704   0.455  ir6c11/pgo89_SW0 (N36)
 LUT3:I2->O            2   0.704   0.526  ir6c11/pgo89 (r5c11)
 LUT3:I1->O            2   0.704   0.482  ixor16/Mxor_S_Result<12>11 (N7)
 LUT3:I2->O            3   0.704   0.531  ir5c13/pgo1 (r6c13)
 MUXF5:S->O            2   0.739   0.526  ir4c15/pgo_f5 (r5c15)
 LUT3:I1->O            1   0.704   0.420  gcout/pgo1 (Cout_OBUF)
 OBUF:I->O                 3.272          Cout_OBUF (Cout)
----------------------------------------
Total                     20.828ns (13.677ns logic, 7.151ns route)
                                   (65.7% logic, 34.3% route)
```

(b)

Figure 8. **(a)**Delay for 16 bit RKSAdder. **(b)** Delay for 16 bit KS Adder.t

5. Conclusion

Thus a design of prefix adder amalgamation reversible logic gates using 16 bit kogge stone adder. From the simulation outcomes it is observed that the computational path

net delay for 16X16 bit prefix adder using reversible logic gate is 20.828 ns and the computational path delay for 16X16 bit prefix adder using reversible logic gate Kogge Stone adder is 17.247 ns. Also by observing the power consumption for 16 bit kogge stone adder and 16 bit prefix adder kogge stone adder usingreversible adder observed power delay/ variation 329 pico seconds/3154073.988nW. The multiplier using 16 bit prefix adder kogge stone adder using reversible adder is much more efficient than the multiplier using 16 bit kogge stone adder in expressions of delay and power consumption.

6. References

1. Hagleitner C, Hierlemann A, Lange D, Kummer A, Kerness N, Brand O, Baltes H. Smart single-chip gas sensor microsystem. Nature. 2001; 414(6861):293–6.
2. Youngjoon K, Kim L-S. 64-bit carry-select adder with reduced area. Electronics Letters. 2001; 37(10):1.
3. Ghosh S, Ndai P, Roy K. A novel low overhead fault tolerant Kogge-Stone adder using adaptive clocking. Proceedings of the Conference on Design, Automation and Test; Europe. 2008 Mar 10. p. 366–71.
4. Brent RP, Kung HT. A regular layout for parallel adders. IEEE Transactions on Computers. 1982 Mar; 1(3):260–4.
5. Sudhakar SM, Chidambaram KP, Swartzlander Jr EE. Hybrid han-carlson adder. IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS); 2012 Aug 5. p. 818–21.
6. Sklansky J. Conditional-sum addition logic. IRE Transactions on Electronic Computers. 1960 Jun; 9(2):226–31.
7. Ladner RE, Fischer MJ. Parallel prefix computation. JACM. 1980 Oct 1; 27(4):831–8.
8. Stan MR, Franzon PD, Goldstein SC, Lach JC, Ziegler MM. Molecular electronics: From devices and interconnect to circuits and architecture. Proceedings of the IEEE. 2003 Nov; 91(11):1940–57.
9. Zhu H, Cheng CK, Graham R. Constructing zero-deficiency parallel prefix adder of minimum depth. Proceedings of the ASP-DAC Asia and South Pacific Design Automation Conference; 2005 Jan 18-21. p. 883–8.
10. Barenco A, Bennett CH, Cleve R, Di Vincenzo DP, Margolus N, Shor P, Sleator T, Smolin JA, Weinfurter H. Elementary gates for quantum computation. Physical Review A. 1995 Nov 1; 52(5):3457.
11. Srinivasan B, Arunkumar S, Rajesh K. A novel approach for color image, steganography using nubasi and randomized, secret sharing algorithm. Indian Journal of Science and Technology. 2015 Apr 1; 8(S7):228–35.
12. Nandal A, Vigneswaran T, Rana AK. Booth multiplier using reversible logic with low power and reduced logical complexity. Indian Journal of Science and Technology. 2014 Apr 13; 7(4):525–9.