Input/output Buffer based Vedic Multiplier Design for Thermal Aware Energy Efficient Digital Signal Processing on 28nm FPGA

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Abstract

Multiplier is used for multiplication of a signal and a constant in Digital Signal Processing (DSP). 28nm technology based Vedic multiplier is implemented with use of VHDL HDL, Xilinx ISE, Kintex-7 FPGA and XpowerAnalyser. Vedic multiplier gains speed improvements by parallelizing the generation of partial products with their concurrent summations. In this work, we are exploring the feasibility of Vedic multiplier in Data Encryption Algorithm, DSP, reliable system, multimedia and fault tolerant systems. In our work, we are using 11 different IO standards from HSTL (High Speed Transistor Logic) and LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) family. IO standards are used to match the impedance of transmission line, input/output port and device. The energy-efficient multipliers play a significant role in portable computing and communication systems also. Here we are using Field Programmable Gate Array (FPGA) in order to reduce the development cost. The development cost for Application Specific Integrated Circuits (ASICs) are high in compare to FPGA. Selection of the most energy efficient IO standards in place of signal gating is the main design methodology for design of energy efficient Vedic multiplier.There is 68.51%, 69.86%, 74.65%, and 78.39% contraction in total power of Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_II in place of HSTL_II_DCI_18 at 56.7°C, 53.5°C, 40°C and 21°C respectively.

Keywords: 💬

1. Introduction

Matrix multiplier for high-speed digital signal processing applications is implemented using spice and 90nm CMOS Technology[1]. The functionality of the circuitry was verified and propagation delay along with dynamic power consumptionsare performance parameter[1]. In this work, we are extending our work from 90nm Technology to 28nm technology and replacing matrix multiplier with Vedic multiplier and migrating from Spice to Xilinx ISE and XPower Analyzer. 250nm Based Multiplier architecture

for two's complement numbers leads to high performance digital signal processing systems with low power consumption[2]. The computation sharing multiplier targets the contraction of power consumption by removing redundant computations within system by computation reuse[2]. Our design is 28nm technology based Vedic multiplier that also gain speed improvements by parallelizing the generation of partial products with their concurrent summations. Modulo 2n + 1 multiplier are critical components in different data security applications like International Data Encryption Algorithm (IDEA), DSP,

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and fault-tolerant systems of high reliability and fault tolerance[3]. In this work, we are exploring the feasibility of Vedic multiplier in IDEA, DSP, reliable system and fault tolerant systems. Field Programmable Analog Array is used for energy efficient mixed-signal computation using 350nm CMOS analog IC. Analog IC is used for digital enhancements to increase compatibility in embedded anlog-digital systems[4]. Analog IC has 78 Computational AnalogBlocks (CABs)[4]. In our work, we are using 11 different IO standards. IO standards are used to match the impedance of transmission line, input/output port and device. Low power multiplier is in demand for multimedia and DSP systems[5]. A low-power signed pipelined truncated multiplier is able to dynamically detect multiple input combinations and deactivate unnecessary transitions in non-effective ranges to reduce the power utilization[5]. Vedic multiplier is parallel in nature. Therefore, it always works efficiently in compare to pipelined architecture by parallelizing the generation of partial products with their concurrent summations. A pipelined fixed width Baugh Wooley multiplier provides four configuration modes (CMs) and uses low-power schemes to achieve the energy efficient pipelined reconfigurable design[6]. In our work, Baugh-Wooley multiplier is replaced with Vedic multiplier and IO standards[20-21] is used to achieve energy efficiency in DSP multiplier. Demand of portable computing and communication systems is growing day by day. Energy efficient multipliers play an important role in portable computing[7]. Baugh-Wooley algorithms are used for multiplication in multiplier. Bough-Wooley multipliers areimplemented on Field Programmable Gate Array (FPGA). The development cost of FPGA based design is cheaper than Application Specific Integrated Circuits (ASICs) design[7]. In our work, we are also making power-efficient multiplier based on Vedic formula and we are implementing our energy efficient Vedic multiplier on Kintex-7 FPGA in place of going for ASIC design of Vedic multiplier. x86-compatible Floating Point Multiplier (FPM) design provide better performance in perspective of low cost, low power and compatibility[8]. Vedic multiplier is also low cost and low power solution for digital signal processing that is compatible with 28nm technology. In DSP, Multiplier is generally used for multiplication of a signal and constant. In various application, an input or output signal is iteratively multiplied by predefined constants[9]. These temporal repetitions may be eliminated in the design of high performance Reconfigurable Constant Multiplier (RCM)[9]. Here, Vedic

multiplier is proposed to use in multiplicationof a signal by constant. Digit-serial implementation styles are one of the best digital signal processing systems with moderate sampling rates[10]. Multipliers are the backbone of DSP specific computations[10]. Gain in sample speed can be traded with contraction in supply voltage resultingthat result in low power consumption[10]. Here, we are doing impedance matching with the help of HSTL[18,20] class I, HSTL class II, and LVCMOS I/O standard[19,20] in place of scaling of power supply voltage. Due to presence of feedback loop, Digit-serial architectures based on unfolding techniques cannot be pipelined beyond a certain level[11]. In reference[11], design methodology for bit level pipelining of digit serial architectures is discussed. The SNR (signal noise ratio) of Digital filter based on truncated multiplier is better than filter with standard multiplier[12]. Our Vedic multiplier is also designed to use in Filter in future. Error-compensation biases are mapped to low-error area-efficient fixed-width multipliers suitable for VLSI implementation and digital signal processing application[13]. The main focus of our design is power. Our design is power-efficient Vedic Multiplier. Two-dimensional (2-D) signal gating schemes is used inenergy efficient array multiplier design[14]. This signal gating deals with gating lines for both multiplicand and multiplier operands[14]. Different regions of the multiplier are dynamically turned off as per the precision of each operand[14]. In our work, we are using energy efficient IO standards in place of signal gating to design energy efficient multiplier. VLSI implementation of hardware efficient truncated multiplier using modified booth algorithm is proposed for signed bit multiplication, such that the average absolute error is kept minimum[15]. This work is also VLSI implementation of hardware efficient multiplier design only we are using Vedic multiplier in place of Booth multiplier. Time complexity of logical circuits is estimated, whereaslogical circuits are constructed from elements of an optical element base[16]. This concept of optical multiplier can be integrated with Vedic multiplier. We have also study different FPGA based techniques[17–21].

2. Schematic of Digital Signal Processor Specific Vedic Multiplier

The Vedic multiplier is designed using structure modeling that consists of 4 two-bit Vedic multiplier,

3 four-bit full adders as presented in Figure 1. The schematic of Vedic multiplier is using look up table (LUT) in Virtex-6. Out of 22 LUTs, it has 1 LUT2, 11 LUT4 and 14 LUT6.

3. Simulation of Green Communication Specific Vedic Multiplier

Here, A and B are four bit vector and s is product of these two vector. A is taken as 10 unsigned decimals i.e. 1010 binary number and B is also taken as 8 unsigned decimals i.e. 1000 binary number. The product of these two bit vector is stored in S bit vector which is of 8 bit. In Figure 2, stimulus is in unsigned decimal format. We can see the results in binary, hexadecimal, signed, unsigned etc. format.

4. Low Power and Thermal Aware Design using HSTL-I Input/ output Buffer and 28nm FPGA for DSP

In order to simplify Investigation, we will use HID_18 in place of HSTL_I_DCI_18, H_I in place of HSTL_I and HID in place HSTL_I_DCI in this paper.

4.1 Total Power Investigation using HSTL Input/output Buffer on 28nm

There are 62.15%, 63.85%, 69.85% and 75.08%contraction in power utilization by Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_I in place of HID_18 at 56.7℃, 53.5℃, 40℃ and 21℃ respectively as presented in Table 1 and Figure 3.
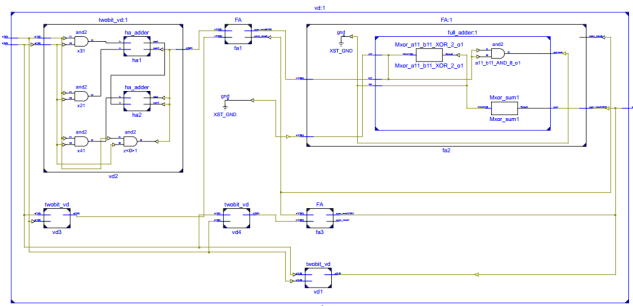

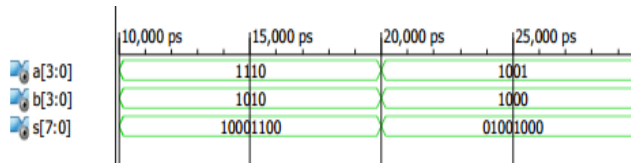**Figure 1.** RTLschematic of DSP specific vedic multiplier.

Figure 2. Waveform of thermal aware energy efficient vedic multiplier.

Table 1. Powerutilization of HSTLbased vedic multiplier on 28nm FPGA

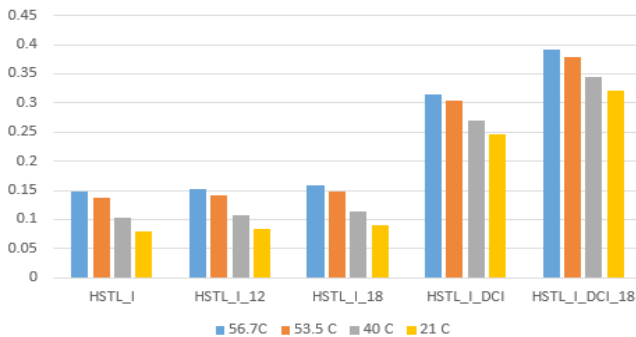|	**H_I**	**H_I_12**	**H_I_18**	**HID**	**HID_18**
56.7℃	0.148	0.152	0.158	0.315	0.391
53.5℃	0.137	0.141	0.147	0.304	0.379
40℃	0.104	0.107	0.114	0.270	0.345
21℃	0.080	0.083	0.090	0.246	0.321

Figure 3. Powerutilization for different ambient temperature using HSTL.

4.2 Leakage Power Investigation using HSTL Input/output Buffer on 28nm

There is 1–2% contraction in power utilization by Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_I_12 or HSTL_I in place of HID_18 at 56.7℃, 53.5℃, 40℃ and 21℃ respectively as presented in Table 2 and Figure 4.

4.3 I/O Power Investigation using HSTL Input/output Buffer on 28nm

There is 86.02%, 84.95%, 82.8% and 26.88% contraction in I/O (Input/Output) power utilization by Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_I, HSTL_I_12, HSTL_I_18, HID respectvely in place of HID_18 at 56.7℃, 53.5℃, 40℃ and 21℃ as presented in Table 3 and Figure 5.

Table 2. PowerUtilization of HSTL Based Vedic Multiplier on 28nm FPGA

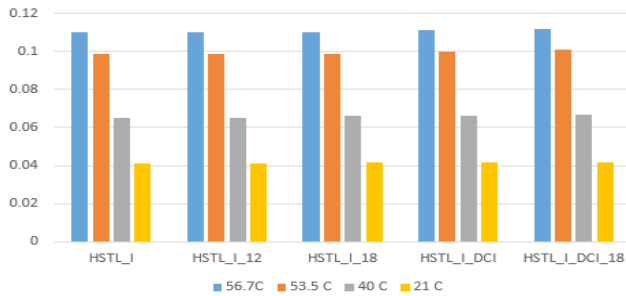|	H_I	H_I_12	H_I_18	HID	HID_18
56.7°C	0.110	0.110	0.110	0.111	0.112
53.5°C	0.099	0.099	0.099	0.100	0.101
40°C	0.065	0.065	0.066	0.066	0.067
21°C	0.041	0.041	0.042	0.042	0.042

Figure 4. Powerutilization for different ambient temperature using HSTL.

Table 3. Powerutilization of HSTLbased vedic multiplier on 28nm FPGA

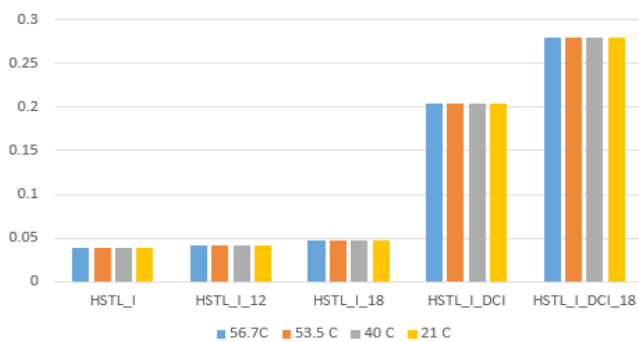|	H_I	H_I_12	H_I_18	HID	HID_18
56.7°C	0.039	0.042	0.048	0.204	0.279
53.5°C	0.039	0.042	0.048	0.204	0.279
40°C	0.039	0.042	0.048	0.204	0.279
21°C	0.039	0.042	0.048	0.204	0.279

Figure 5. I/O power utilization for different ambient temperature using HSTL.

4.4 Thermal Investigation using HSTL Input/output Buffer on 28nm

There is minor contraction in junction temperature of Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_I, HSTL_I_12, HSTL_I_18, HID respectvely in place of HID_18 at 56.7°C, 53.5°C, 40°C and 21°C as presented in Table 4 and Figure 6.

5. Low Power and Thermal Aware Design using HSTL-IIInput/output Buffer and 28nm FPGA for Digital Signal Processing

In order to simplify Investigation, we will use H_IID18 in place of HSTL_II_DCI_18, H_II in place of HSTL_II and H_IID in place HSTL_II_DCI in this paper.

5.1 Total Power Investigation using HSTL II Input/output Buffer on 28nm FPGA

There is 68.51%, 69.86%, 74.65%, and 78.39% contraction in total power of Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_II in place of HSTL_II_DCI_18 at 56.7°C, 53.5°C, 40°C and 21°C respectively as presented in Table 5 and Figure 7.

Table 4. Junction Temperature of HSTLbased vedic multiplier on 28nm FPGA

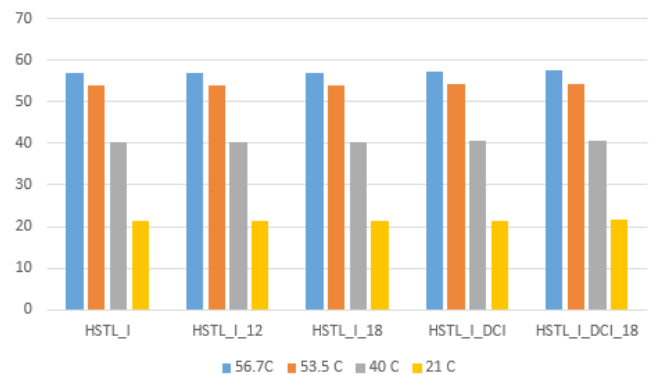|	H_I	H_I_12	H_I_18	HID	HID_18
56.7°C	57	57	57	57.3	57.5
53.5°C	53.8	53.8	53.8	54.1	54.3
40°C	40.2	40.2	40.2	40.6	40.7
21°C	21.2	21.2	21.2	21.5	21.7

Figure 6. Junction temperature for different ambient temperature using HSTL.

Table 5. Powerutilization of HSTLbased vedic multiplier on 28nm FPGA

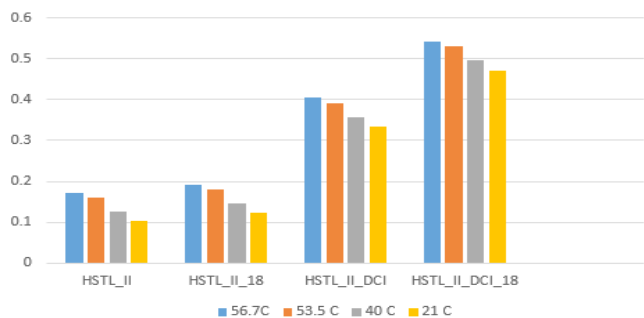|	H_II	H_II_18	H_II_D	H_II_D18
56.7°C	0.171	0.191	0.404	0.543
53.5°C	0.160	0.180	0.392	0.531
40°C	0.126	0.146	0.358	0.497
21°C	0.102	0.122	0.334	0.472

Figure 7. Total power versus ambient temperature.

5.2 Leakage Power Investigation using HSTL II Input/output Buffer on 28nm FPGA

There is minor contraction in total power of Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_II in place of HSTL_II_DCI_18 at 56.7°C, 53.5°C, 40°C and 21°C respectively as presented in Table 6 and Figure 8.

5.3 IO Power Investigation using HSTL II Input/output Buffer on 28nm FPGA

There is 85.81% contraction in IO Power utilization of Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_II, HSTL_II_12, HSTL_II_18, HSTL_II_DCI respectvely in place of HSTL_II_DCI_18 at 56.7°C, 53.5°C, 40°C and 21°C as presented in Table 7 and Figure 9.

5.4 Thermal Investigation using HSTL II Input/output Buffer on 28nm FPGA

There is minor change in junction temperature of Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_II, HSTL_II_12, HSTL_II_18, HSTL_II_DCI respectvely in place of HSTL_II_DCI_18 at 56.7°C, 53.5°C, 40°C and 21°C as presented in Table 8 and Figure 10.

Table 6. Leakage power utilization of HSTLbased vedic multiplier on 28nm FPGA

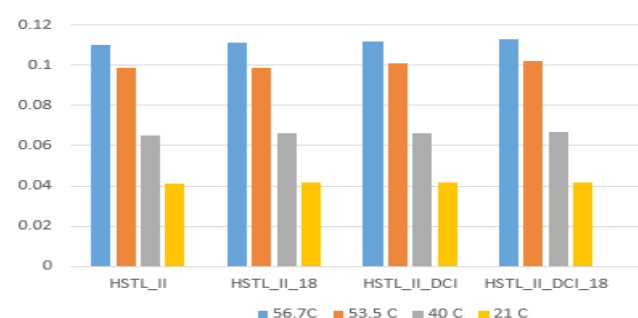|	H_II	H_II_18	H_II_D	H_II_D18
56.7°C	0.110	0.111	0.112	0.113
53.5°C	0.099	0.099	0.101	0.102
40°C	0.065	0.066	0.066	0.067
21°C	0.041	0.042	0.042	0.042

Figure 8. Leakage power versus ambient temperature.

Table 7. IO Powerutilization of HSTLbased vedic multiplier on 28nm FPGA

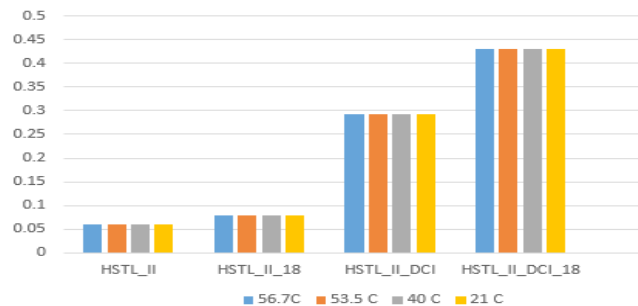|	H_II	H_II_18	H_II_D	H_II_D18
56.7°C	0.061	0.080	0.292	0.430
53.5°C	0.061	0.080	0.292	0.430
40°C	0.061	0.080	0.292	0.430
21°C	0.061	0.080	0.292	0.430

Figure 9. IOpower versus ambient temperature.

Table 8. Junction temperature of HSTLbased vedic multiplier on 28nm FPGA

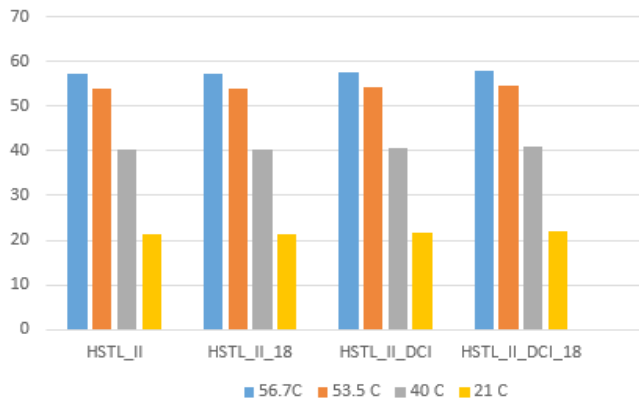|	H_II	H_II_18	H_II_D	H_II_D18
56.7°C	57.1	57.1	57.5	57.8
53.5°C	53.8	53.9	54.3	54.6
40°C	40.3	40.3	40.7	41.0
21°C	21.2	21.3	21.7	22.0

Figure 10. Junction emperature versus ambient temperature.

Table 9. Powerutilization of LVCMOS based vedic multiplier

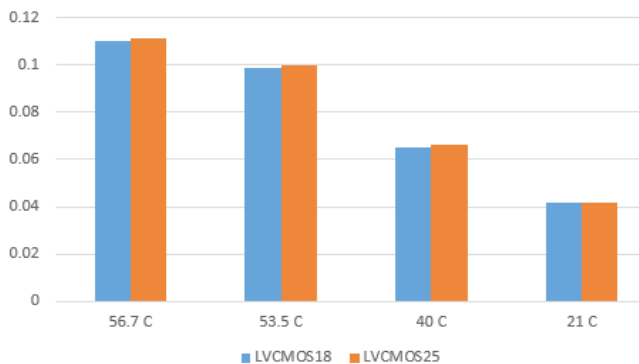|	LVCMOS18	LVCMOS25
56.7°C	0.110	0.111
53.5°C	0.099	0.100
40°C	0.065	0.066
21°C	0.042	0.042

Figure 11. Powerutilization versus ambient temperature.

6. Low Power and Thermal Aware DSP Design using LVCMOS Input/output Buffer and 28nm FPGA for DSP

6.1 Total Power Investigation of LVCMOS Input/output Buffer and Different FPGA

There is minor change in power utilization when we use LVCMOS18 IO standards in place of LVCMOS25 IO standards as presented in Table 9 and Figure 11.

6.2 Thermal Investigation of LVCMOS Input/output Buffer and Different FPGA

There is no change in junction temperature when we use LVCMOS18 I/O standards in place of LVCMOS25 I/O standards as presented in Table 10 and Figure 12.

7. Hardware Implementation

After connecting FPGA with laptop using JTAG Cable, we click on configure target device and change dual in line switch to provide input and we observe value of dual in line switch on red LED and output of program on green LED as presented in Figures 13–15.

Then we are providing two inputs. One is 11 that are presented in Figure 14 as both third and fourth red LED glow. Other is 01 that is presented in Figure 14 as first led is glowing (corresponding to 1) and second led is not glowing (corresponding to 0).

Then we are providing two inputs. One is 11 that are presented in Figure 15 as both third and fourth red LED glow. Other is 11 that is also presented in Figure 15 as first led is glowing (corresponding to 1) and second led is also glowing (corresponding to 1).

Table 10. Junction temperature of LVCMOS based vedic multiplier

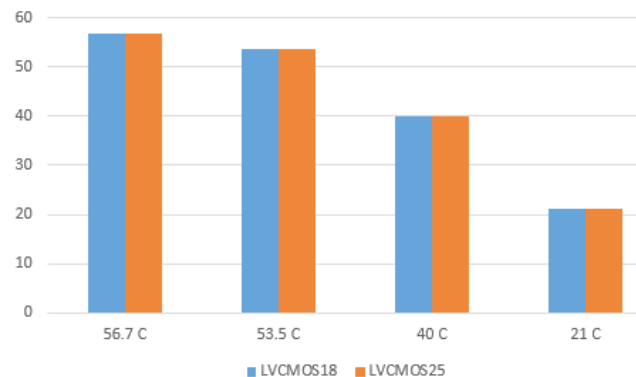|	LVCMOS18	LVCMOS25
56.7°C	56.9	56.9
53.5°C	53.7	53.7
40°C	40.1	40.1
21°C	21.1	21.1

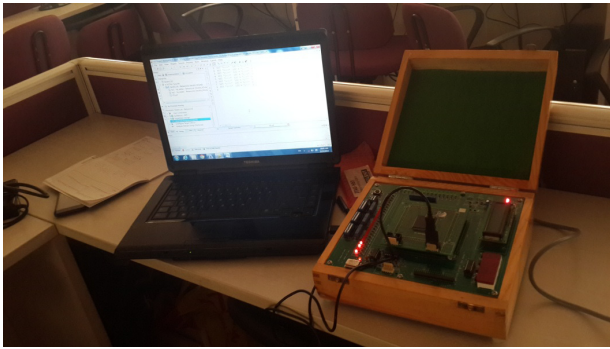**Figure 12.** Junction temperature versus ambient temperature.

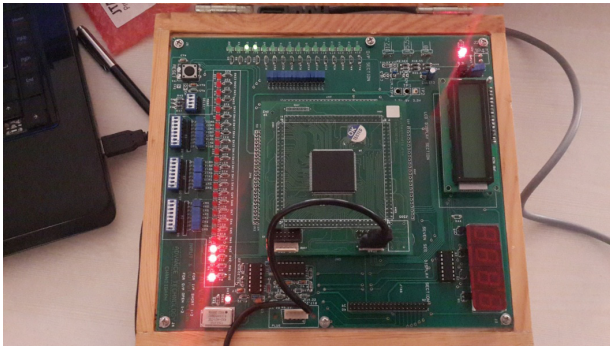**Figure 13.** Initially FPGA Connected with Laptop.

Figure 14. When input (Red LED) is 11 and 01 then output (Green LED) is 0011.
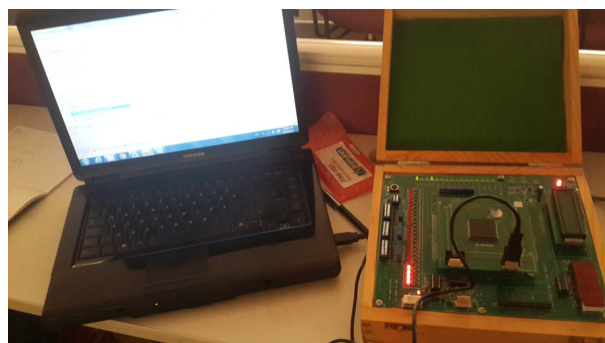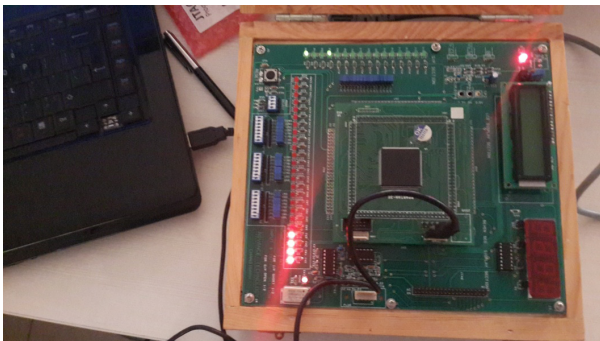

Figure 15. When input (Red LED) is 11 and 11 then output (Green LED) is 1001.

8. Conclusion

This 28nm technology based Vedic multiplier is more power efficient than 40nm technology based FPGA. Vedic multiplier gains speed improvements by parallelizing the generation of partial products with their concurrent summations. Among 11 different IO standards from HSTL (High Speed Transistor Logic) and LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) family, we find that LVCMOS18 is the minimum power consumer among LVCMOS family, HSTL_I is the minimum power consumer among HSTL class I family and HSTL_II is the minimum power consumer among HSTL class II family. Our design is Field Programmable Gate Array (FPGA) based because the development cost for Application Specific Integrated Circuits (ASICs) are high. There are 62.15%, 63.85%, 69.85% and 75.08% contraction in power utilization by Vedic multiplier on 28nm Kintex-7 FPGA, when we use HSTL_I in place of HID_18 at 56.7ºC, 53.5ºC, 40ºC and 21ºC respectively.

9. Future Scope

Here, the application of Vedic multiplier is limited to digital signal processing. In future, we can also use this Vedic multiplier in Data Encryption Algorithm, green communication, reliable system, multimedia and fault tolerant systems. In future, we can also go for ASIC implementation of Vedic multiplier. This design is implemented on 28nm technology based FPGA. In future, we can also go for ultra-scale FPGA, 3D ICs and SoC based Vedic multiplier design.

10. References

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