

Comparative Analysis of Cascaded Multilevel Inverter for Phase Disposition and Phase Shift Carrier PWM for Different Load

A. Ramesh Babu*

Department of Electrical and Electronics Engineering, Sathyabama University, Chennai, India;
rameshbabuaa@gmail.com

Abstract

This paper presents the optimized harmonic elimination stepped waveform technique to improve the output waveform of 7-level Cascaded Multilevel Inverter (CMLI) fed induction motor. The CMLI with separate DC source is used generate a 7-level output with three H-bridge and 12 switch's. The working of 7-level CMLI is analyzed by phase disposition and phase shifting pulse width modulation with bipolar and unipolar modes of operation. The performance of CMLI is examined by various parameters such as THD, power factor, motor current, motor speed and torque. The presented result carried out using MATLAB/simulink. The simulation result for phase disposition and phase shift carrier PWM were compared. The 7-level CMLI hardware with phase shift carrier modulation was developed to validate simulation result.

Keywords: CMLI, Phase Disposition, Phase Shift Carrier, Single Phase Asynchronous Induction Motor, THD, Unipolar and Bipolar

1. Introduction

The multilevel inverters are very much popular in high power application such as electric utility; AC drives in industry and hybrid electric vehicle due to their high voltage & power handling ability, Low THD, reduced EMI and Easy power device selection³. The conventional H-bridge inverter output voltage has desirable harmonics due to that the shape of the output is not sinusoidal. This leads to create unnecessary heating loss, which result in reduction of the efficiency. Many types of multilevel inverters are discussed⁴ Diode Clamped Multilevel Inverter (DCMLI), Flying capacitor multilevel inverter and Cascaded Multilevel Inverter (CMLI). Among these multilevel converters the CMLI is best suited¹⁻⁴ for high power application due to their number of component used, cost and reliability. The other converters like DCMLI and FCMLI are restrict the power range of opera-

tion use more number of capacitor⁵. The main objective of CMLI is to reduce THD value below 5%, for that many Pulse widths modulation technique has been proposed. The selective harmonic minimization has proposed to minimize the lower order harmonic⁶ but it is not able to reduce the THD value. Among them sinusoidal pulse width modulation is best suited for MLI due to its low THD, low voltage stress across switch and can operate lower switching frequency. The sinusoidal modulations with different strategies are discussed Phase disposition, phase opposition disposition, alternate phase opposition disposition and phase shift⁷⁻⁹. The 5-level CMLI hybrid phase disposition PWM technique able to reduce THD to 25% and alternate Phase Opposition and Disposition (APOD) reduces to 17%^{10,11}.

*Author for correspondence

The sinusoidal PWM based modified cascaded multilevel inverter was proposed¹². The simulation and analysis multilevel inverter fed induction motor is proposed to reduce THD value¹³. The THD value of CMLI is reduced by increasing the number of level, but the level increases more which leads to increase complexity of circuit and maintain imbalance output voltage. Hence the proposed work selected 7-level CMLI with phase disposition and phase shift carrier PWM for both bipolar and unipolar modes of operation.

2. Proposed 7-level Cascaded Multi Level Inverter

The concept of this multilevel inverter is based on connecting H-bridge inverters in series to get a various level output. The output multilevel inverter is calculated is addition each bridge.

$$\text{Output voltage } V_o = V_{o1} + V_{o2} + V_{o3} \text{-----}(1)$$

Where V_{o1} , V_{o2} , V_{o3} is each H-bridge output voltage.

The level of the output voltage is desired by number dc source used in the inverter. It is determined by $L=2S+1$ where L is number of level and S is source used.

The multilevel inverter using the cascaded converters with separate DC sources is discussed here. The cascaded multilevel inverter synthesizes a desired voltage from several independent sources of DC voltages. The multilevel inverter is popular in high-power AC supplies due to PWM technique. The PWM signals are obtained by comparing high frequency carrier with fundamental frequency reference signal. For 7 level inverter we need to have 6 carrier signals. If the reference signal is high compared to carrier switch is on and vice versa. The amplitude and frequency modulation index desired output voltage magnitude and frequency. It is expressed by,

$$\text{Amplitude modulation } L_a = \frac{A_r}{(L-1).A_c} \text{-----}(2)$$

$$\text{Frequency modulation } L_f = \frac{f_c}{f_r} \text{-----}(3)$$

The switch's S1-S4 each converter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. The switching of MOSFETs by different PWM technique is to obtain the 7-level output voltage. For

implementing prototype, MOSFET is selected due to its fast switching nature. But the simulation carried out using Ideal switch. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. The THD value is determined by using equation (1).

$$THD = \sqrt{\sum_{n=3,5,7,\dots,\infty} V_n^2} \text{-----}(4)$$

One of the advantages of this type of 7-level CMLI is that it needs less number of components comparative to the Diode clamped or the flying capacitor.

2.1 Switching Pattern

The 7-level CMLI circuit diagram with ideal switch as shown in Figure 1. Each Inverter Bridge is capable of generating three different levels of voltage outputs. When the positive group switches are turned on, the voltage produced by the bridge is positive. When the negative group switches are turned on the voltage across that particular bridge is negative. The switching pattern for different voltage levels is given in Table 1.

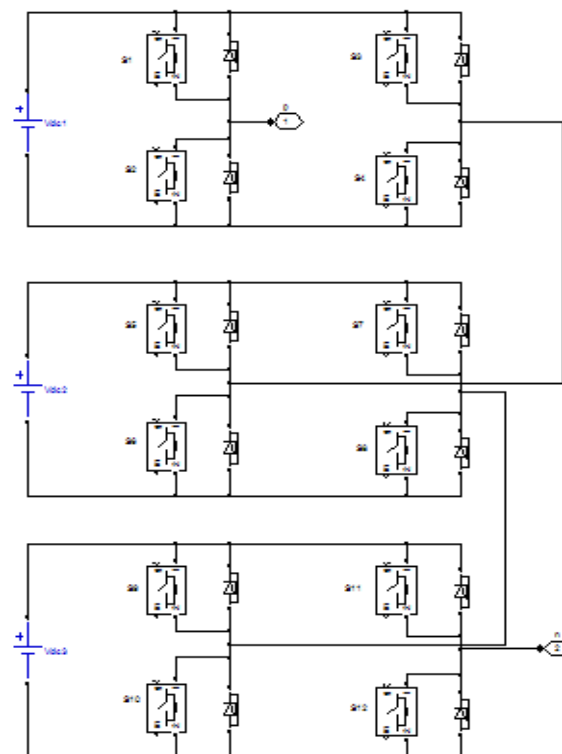


Figure 1. 7-level CMLI circuit diagram.

Table 1. Switching pattern for 7-level CMLI

Sw	$3V_{dc}$	$2V_{dc}$	V_{dc}	$0V_{dc}$	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$
S1	1	1	1	1	0	0	0
S2	0	0	0	0	1	1	1
S3	0	0	0	1	1	1	1
S4	1	1	1	0	0	0	0
S5	1	1	0	0	0	0	0
S6	0	0	1	1	1	1	1
S7	0	0	0	0	1	1	1
S8	1	1	1	1	0	0	0
S9	1	1	1	1	0	0	0
S10	0	0	0	0	1	1	1
S11	0	1	1	1	0	1	1
S12	1	0	0	0	1	0	0

3. Simulation Result

The simulation diagram of 7 level CMLI is shown in Figure 2. It consists of sub system, single phase capacitor start-run induction motor, Power factor measurement block, speed and torque measurement. The sub system consist of 7 level CMLI is made up of 12 ideal switches and control techniques block. The motor input power factor calculated by measuring active power and rms value of voltage and current.

There are different control techniques available for a cascaded H-bridge MLI. Among all those techniques, PWM control technique which produces less Total Harmonic Distortion (THD) values is most preferable. In PWM technique, modulated signal can be of pure sinusoidal, third harmonic injected signals and dead band signals. The carrier signal is a triangular wave. For generating triggering pulses of MLI, pure sinusoidal wave as modulating signal and multi carrier signal which is of triangular in shape have been considered. For a m-level MLI, m-1 carrier signals are required. For generation of triggering pulses to the cascaded MLI, carrier signals are

constructed for different modulation indices using PD and PS control techniques. Output phase voltage has been measured using all the techniques. THD analysis for the PD and PS control techniques in both bipolar, unipolar mode of operation for different modulation indices has been presented in this paper.

3.1 Phase Disposition with Bipolar Switching

The Figure 3 indicate Circuit diagram for generation of Phase disposition with Bipolar switching. The phase disposition modulation was carried out by comparing six carrier signals with sinusoidal reference signal. The six carrier signal was generated with different amplitude same phase. The amplitude of six carrier signals varies +2 to +3, +1 to +2, 0 to 1, -1 to 0, -2 to -1 and -3 to -2. These six carrier signal with frequency of 2Khz was compared with reference sinusoidal signal six PWM signal were obtained. These six PWMs are applied to positive switches of H-bridge. The complementary of these PWM signals are applied to negative switches. As a result totally

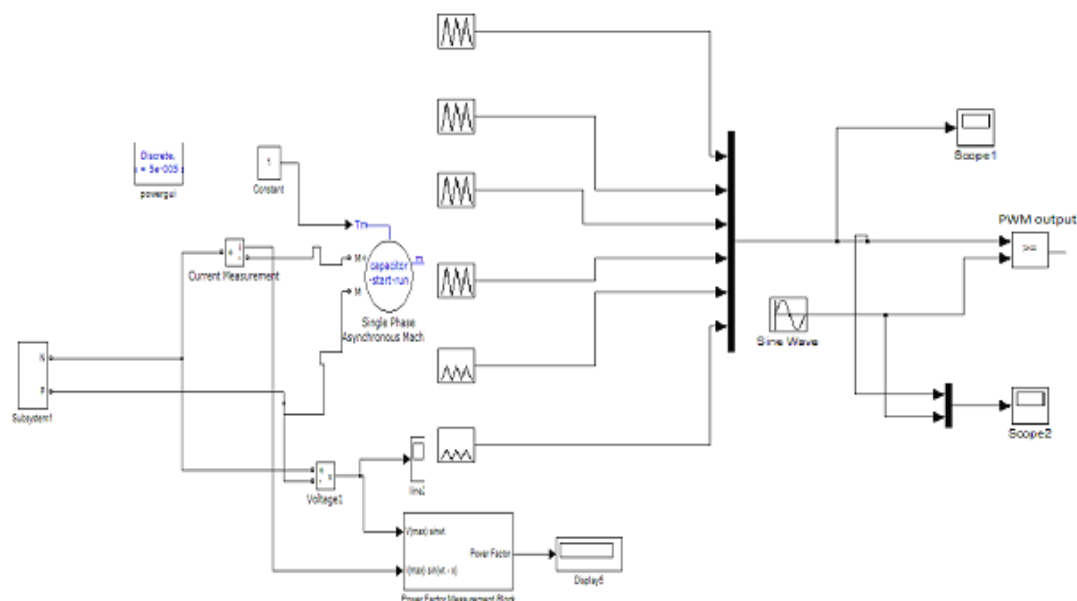


Figure 2. Simulation diagram of 7 level CMLI with induction motor.

12 PWM signals are generated for 12 switches. The Figure 4 shows that carrier and reference sinusoidal signal of phase disposition modulation.

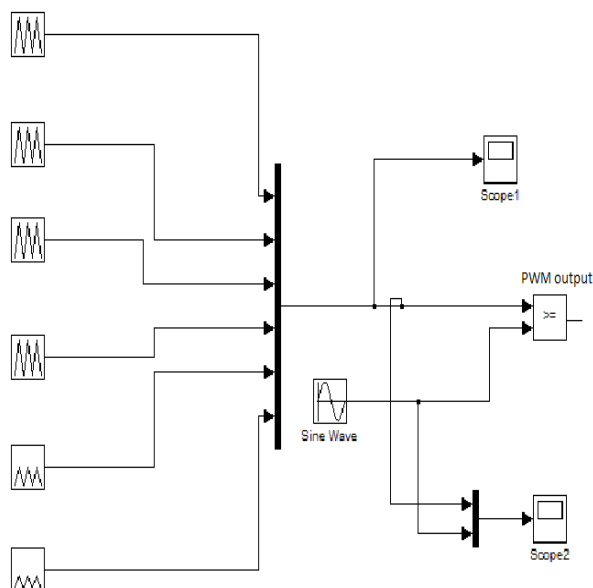


Figure 3. Circuit diagram for generation of Phase disposition with Bipolar switching.

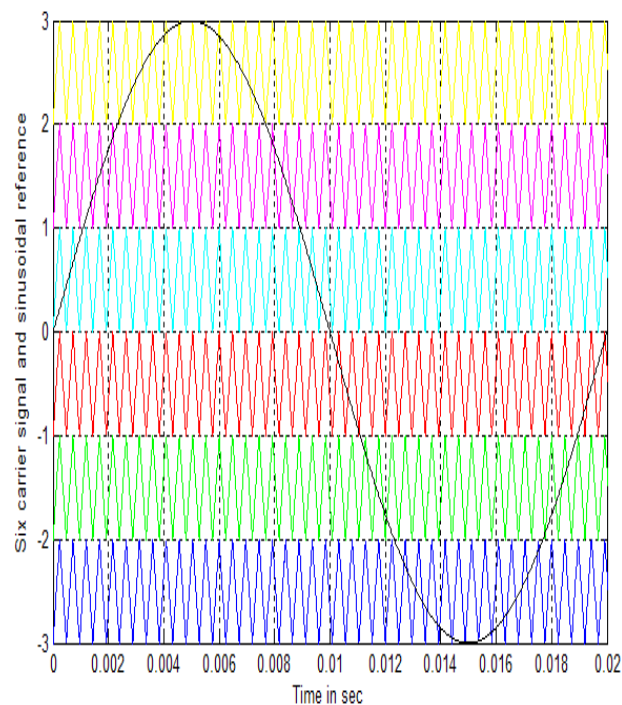


Figure 4. Carrier and reference signal of phase disposition modulation with bipolar switching.

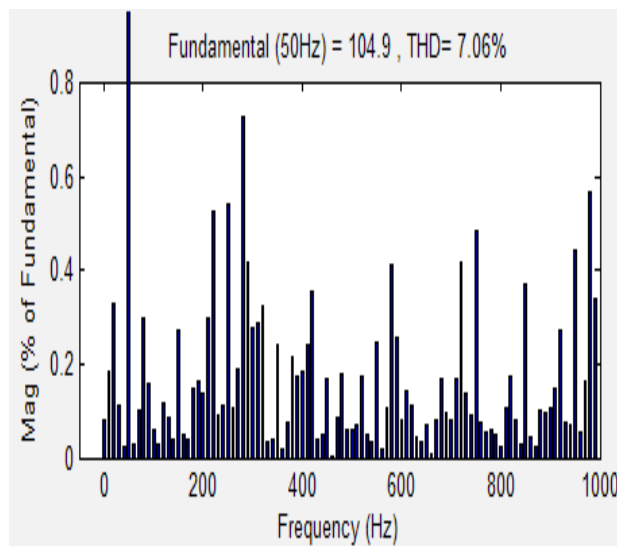


Figure 5. FFT analysis of load voltage for phase disposition bipolar switching.

Figure 5 indicates FFT analysis of load voltage for phase disposition bipolar switching. The THD value measured at the load voltage is 7.06% for RL load. For single phase induction motor speed and electromagnetic torque developed is shown in Figure 6. It shows that speed of 1320 rpm and torque of 3.745 Nm.

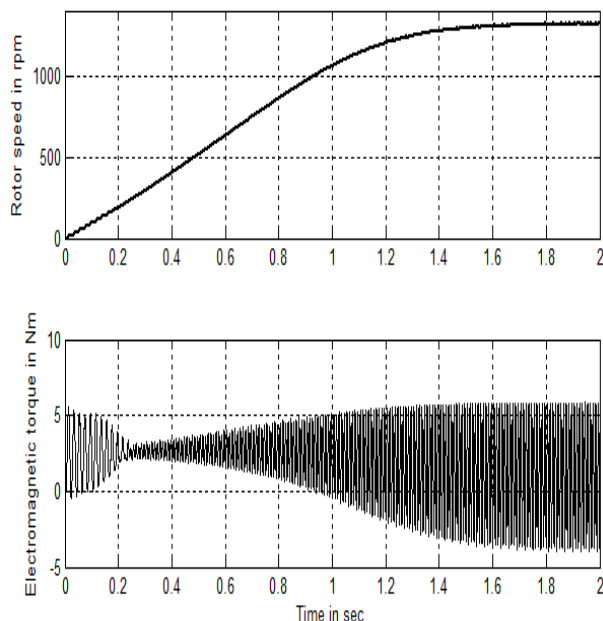


Figure 6. Speed and torque of induction motor at load torque of 1 Nm for phase disposition bipolar switching.

3.2 Phase Disposition with Unipolar

Figure 7 indicates the Circuit diagram for generation of Phase disposition with unipolar switching. The phase disposition modulation was carried out by comparing three carrier signals with two reference sinusoidal signal. The three carrier signal was generated with different amplitude same phase. The amplitude of three carrier signal varies +2 to +3, +1 to +2 and 0 to +1. The six PWM signal were obtained by comparing three carrier signals with two complementary reference sinusoidal signals. The rest of six PWM signal obtained by complementary of these PWM signal. Hence the 12 PWM signals are generated for 12 switches. The Figure 8 shows that carrier and reference sinusoidal signals of phase disposition modulation.

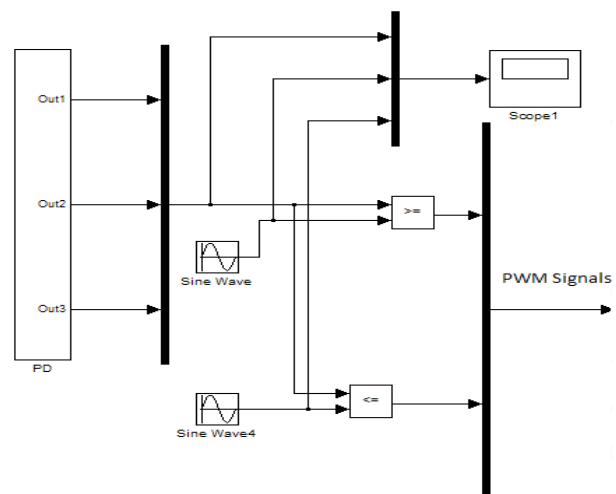


Figure 7. Simulation diagram for generation of Phase disposition with Unipolar switching.

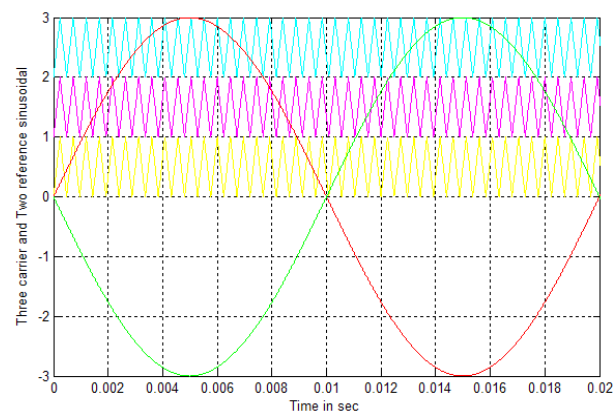


Figure 8. Carrier and reference signal of phase disposition modulation with unipolar switching.

Figure 9 shows that FFT analysis of load voltage for phase disposition bipolar switching. The THD value measured at the load voltage is 7.04% for RL load, when single phase induction motor as load, speed and electromagnetic torque developed. Figure 10 shows that speed of 1320 rpm and torque of 3.745 Nm.

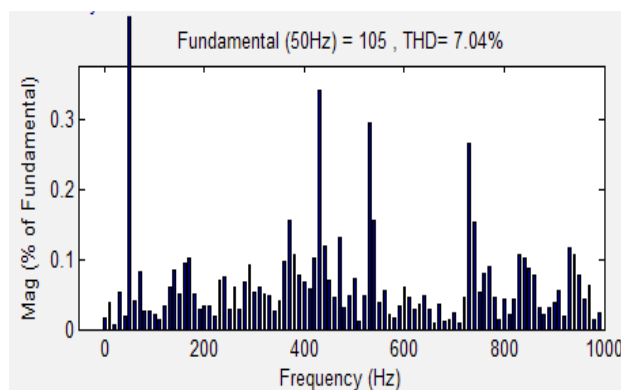


Figure 9. FFT analysis of load voltage for phase disposition bipolar switching.

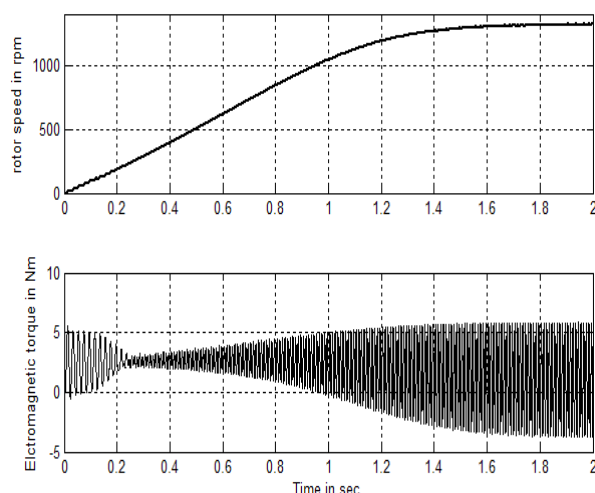


Figure 10. Speed and torque of induction motor at load torque of 1 Nm for phase disposition unipolar switching.

3.3 Phase Shift Carrier with Bipolar

The Figure 11 shows that carrier for phase shift bipolar modulation. The phase shift modulation was carried out by comparing three carrier signals with two reference sinusoidal signal. The three carrier signals are generated by 120 degree phase shift with constant magnitude of +2 to -2. The carrier signals are compared with sinusoidal and complementary sinusoidal as a result six PWM signals are generated.

The Figure 13 indicates that three carrier signals and two sinusoidal signals. The remaining six PWM can be obtained by complementary of previous six PWM signals for negative switches of H-bridge. The Figure 12 illustrates simulation diagram of phase shift PWM for bipolar switching.

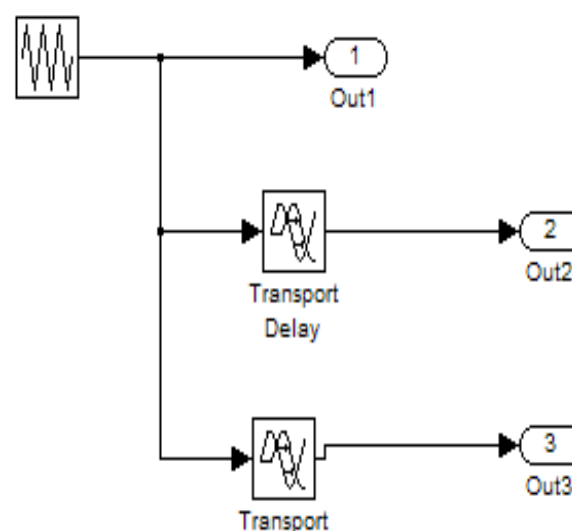


Figure 11. Simulation diagram for carrier generation of phase shift with bipolar

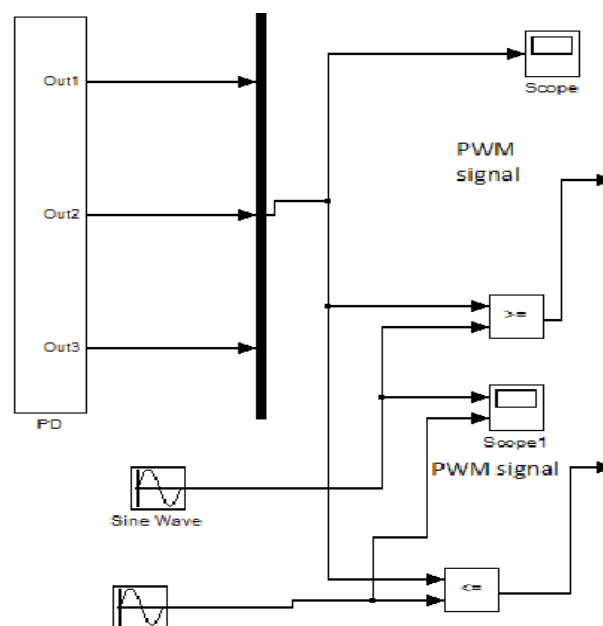


Figure 12. Simulation diagram for PWM generation of phase shift with bipolar.

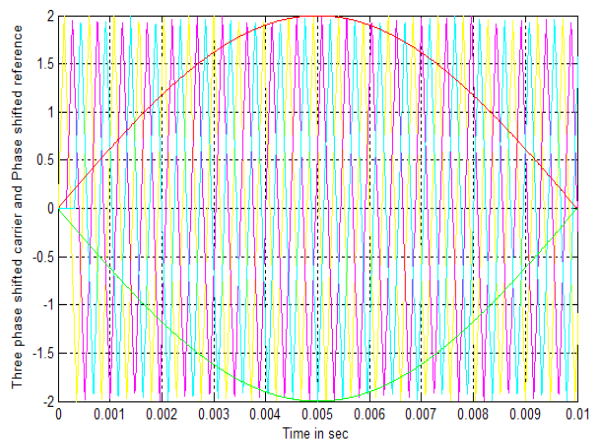


Figure 13. Carrier and reference signal of phase shift modulation with bipolar switching.

The 7 level CMLI load voltage THD value measured is 5.45 for RL load as shown in Figure 14. The speed and torque of single phase induction motor is shown in Figure 15. The speed and torque values are 1318rpm and 3.865 Nm.

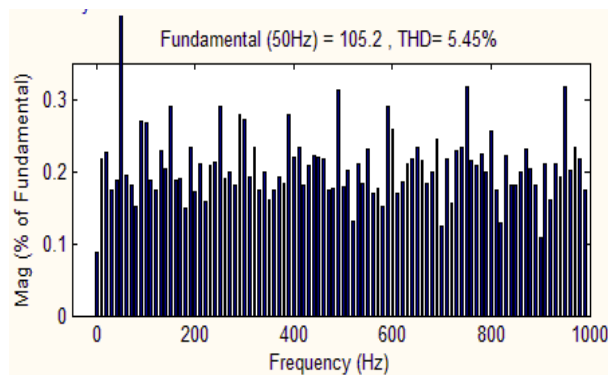


Figure 14. FFT analysis of load voltage for phase shift modulation with bipolar switching.

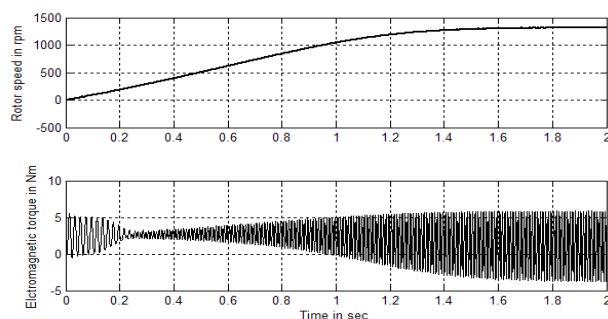


Figure 15. Speed and torque of induction motor at load torque of 1 Nm for phase shift bipolar switching.

3.4 Phase Shift Carrier with Unipolar

The Figure 16 shows that generation of carrier for phase shift unipolar modulation. The unipolar phase shift modulation was carried out by comparing six carrier signals with one reference sinusoidal signal. The six carrier signals are generated by 60 degree phase shift. The carrier signals are compared with sinusoidal and complementary sinusoidal as a result six PWM signals are obtained. The remaining six PWM can be obtained by complementary of previous six PWM signals. The Figure 17 illustrate phase shift PWM for bipolar switching.

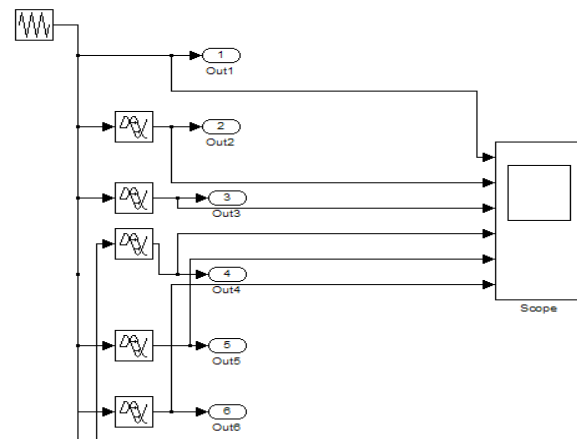


Figure 16. Simulation diagram for PWM generation of phase shift with unipolar.

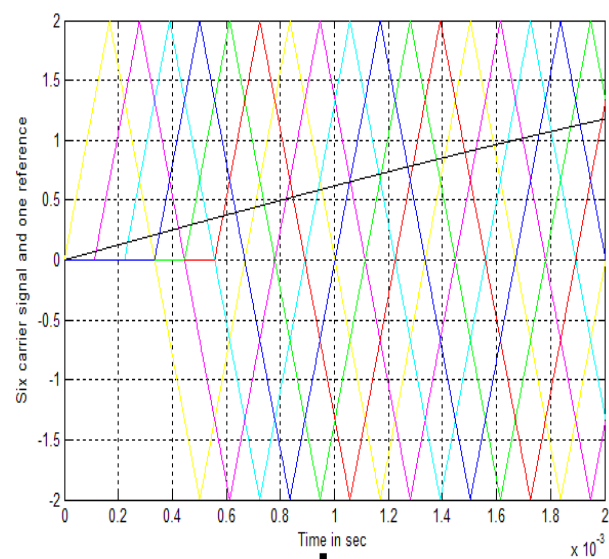


Figure 17. Carrier and reference signal of phase shift modulation with unipolar switching.

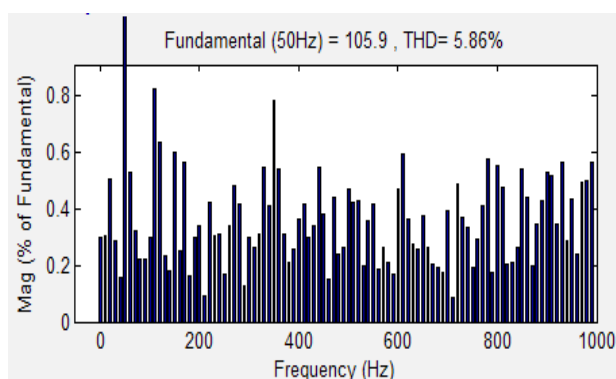


Figure 18. FFT analysis of load voltage for phase shift modulation with bipolar switching.

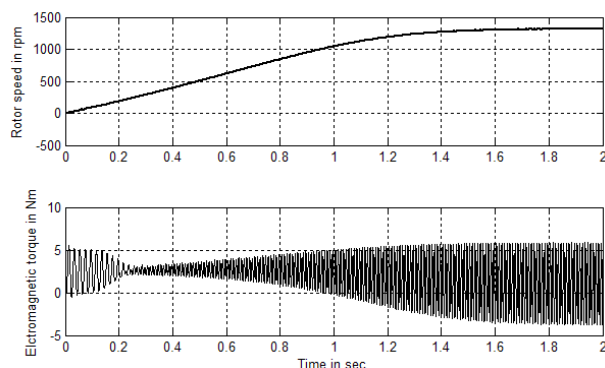


Figure 19. Speed and torque of induction motor at load torque of 1 Nm for phase shift unipolar switching.

The Figure 18 shows that the FFT analysis of load voltage for phase shift modulation with bipolar switching. The THD value measured at the load voltage is 5.86% for RL load. For single phase induction motor speed and

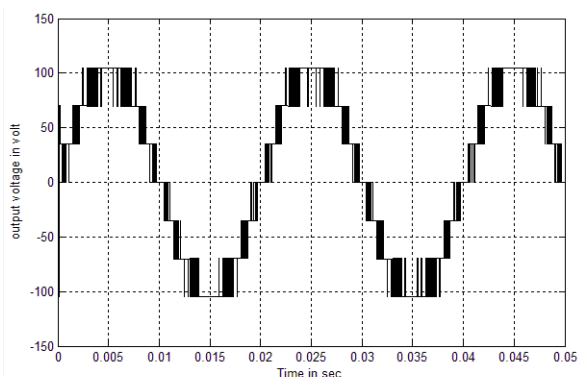


Figure 20. Output voltage of 7 level CMLI.

electromagnetic torque developed is shown in Figure 19, the motor speed of 1321 rpm and torque of 3.77 Nm.

3.5 Load Voltage & Voltage Stress

The simulated load voltage of 7 level CMLI is 105 volt- age i.e. shown in Figure 20. The RL load and motor load output voltage THD values are tabulated in Table 2 and 3. The phase shift carrier modulation provides better THD compared other modulation technique.

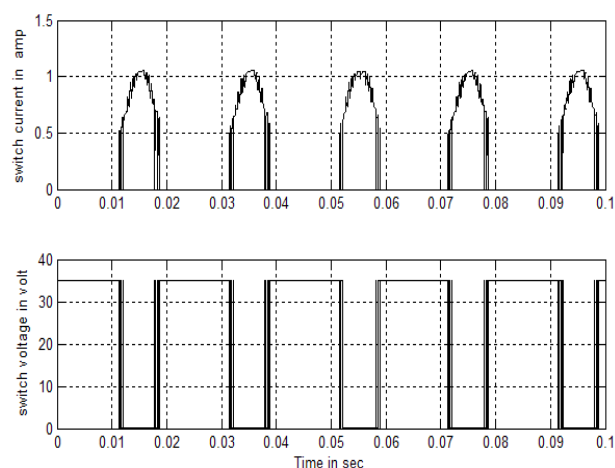


Figure 21. Switch current and voltage for phase disposition with RL load.

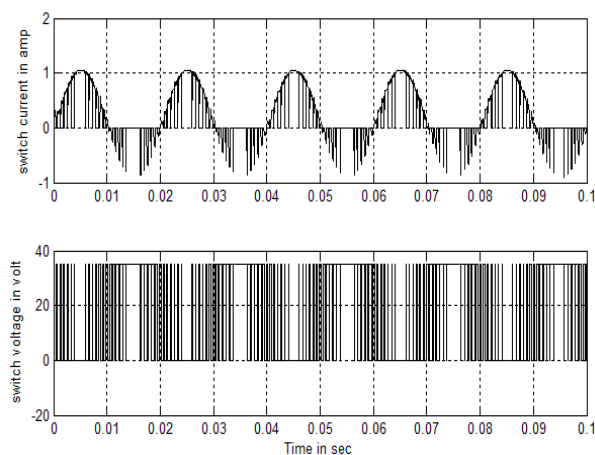


Figure 22. Switch current and voltage for phase shift with RL load.

The voltage stress across the switch for phase disposition and phase shift modulation shown in Figure 21 and 22. The value of voltage stress across the switch is 35 volt.

3.6 Simulation Specification

- Input voltage : 35 volt
- Output voltage : 105 volt
- Switching Frequency : 2 KHz
- Switch : Ideal switch
- RL load : $100+j6.28\Omega$
- Motor : Capacitor start-run
- Power factor : 0.98
- THD : 1.57%

3.7 Comparison Result

The Table 2 indicates that comparison of different modulation technique of 7 level cascaded multilevel inverter. From these results we conclude that phase shift carrier modulation have better result compared to phase disposition modulation. The THD value of phase shift carrier modulation is 5.45 and the power factor is 0.982.

Table 2. Comparison of different modulation of 7 level CMLI with RL load

Modulation	THD	Power factor	Output volt	Voltage stress
Phase Disposition - Bipolar	7.06	0.98	105	35
Phase Disposition – Unipolar	7.06	0.98	105	35
Phase Shift – Bipolar	5.45	0.982	105	35
Phase Shift - Unipolar	5.91	0.982	105	35

The Table 3 illustrates that Comparison of different modulation of 7 level CMLI with single phase induction motor for load torque of 1 Nm. From those result we know that phase shift carrier modulation provides better result compared to phase disposition modulation. The phase shift carrier with unipolar modulation obtains the THD value of 1.57%. The voltage stress across the switch, power factor and capacitor voltage are same for all modulation. The phase shift carrier with unipolar provide developed torque of 3.770 Nm. Hence the phase shift carrier modulation has chosen for implement the hardware.

Table 3. Comparison of different modulation of 7 level CMLI with single phase induction motor for load torque of 1 Nm

Modulation	PD-bipolar	PD-unipolar	PS-bipolar	PS-unipolar
Main winding current in amp	1.4	1.49	1.48	1.39
Auxiliary winding current in amp	0.749	0.746	0.744	0.748
Capacitor voltage in volt	160	160	160	160
Rotor speed in rpm	1320	1320	1318	1321
Torque developed in Nm	3.745	3.713	3.685	3.77
THD in %	18.08	6.39	18.08	1.57
Power factor	0.978	0.978	0.978	0.978
Voltage stress in volt	35	35	35	35

4. Experimental Result

The Experimental setup for 7 level CMLI for phase shift carrier modulation shown in Figure 23. The hardware consists of cascaded 7-level inverter, FPGA controller, PC, JTAG, Buffer circuit, Opto isolator, and Driver circuit and 1 Φ induction motor. The specification of all hardware components are tabulated in Table 4. The 7 level CMLI consists of three single phase H-bridge inverters connected in series. Each inverter needs one DC source. The DC voltage is acquired from bridge rectifier connected to a. c. supply. Each switch associated with snubber to provide over voltage protection. A capacitor is connected across the Dc voltage to reduce the ripple. The output of the H-bridge inverter is used to fed an single phase AC induction motor. The required PWM pulses for firing the

switches are generated from the FPGA processor. The PWM signals are applied to gates of the MOSFET IRF840. The FPGA configuration is generally specified using a Hardware Description Language (HDL), FPGA processor consists of PLL, ADC (analog to digital conversion), DAC (Digital to Analog Conversion), serial port etc. Personal computer is used to write programs for the FPGA in XILLINX software platform. JTAG is an IEEE standard high Speed Protocol which is used to interface the FPGA controller and the Personal computer. The written coding is loaded to FPGA through JTAG emulator. Frequency & Modulation index keys are used to give input to the FPGA controller. Frequency key is used to vary the output frequency of the inverter. Modulation index key is used to vary the output voltage of the inverter. The switching signals which are generated by the Field Programmable Gate Array logic (FPGA) are fed to Opto isolator to isolate the PWM signals from high voltage section. These PWM signals are fed Driver IR2110. The driver circuit appropriately in order to provide the required Gate to Source voltage of the MOSFETs. The power switches are driven by a driver circuit, which switches according to the switching signals generated by the FPGA. Finally the inverter generates 7-level output voltage.

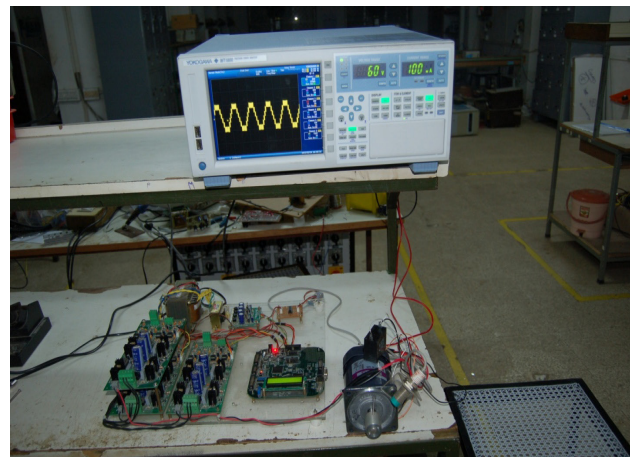


Figure 23. Experimental setup for 7 level CMLI for phase shift carrier modulation.

4.1 Algorithm for PWM Generation

- Generate the single phase sine wave with 50 Hz. For generating the 50 Hz use LUT and up counter. Take 200 samples at the sampling period of 10 kHz. LUT has the sine sample array and up counter holds index of array. Increment the array by counter and load the

sample from LUT, control the counter for sampling at particular rate.

- Quantize the sine samples according to our carrier height. For 7-levels inverter number of carrier is 6. So multiply and add with 3000. Then get the center value of sine is 3000, peak is 6000 and peak to peak is 0 to 6000 for modulation index of one.
- Generate the carrier as a triangular wave form by the use of up-down counter. From that carrier may generate phase shifted carrier by the help of delay, and offset carrier by the help of adder. First generate the carrier height of 0 to 1000. Then add 1000 for each offset level. So carriers having height of 0 to 1000, 1000 to 2000, 2000 to 3000, 3000 to 4000, 4000 to 5000, 5000 to 6000 respectively.
- Now compare each carrier with the fundamental sine and generate two PWM pulses which having 180

Table 4. Specification of Hardware

Description	Specification
MOSFET	IRF840,500V,8A
Driver Circuit	IR2110
Voltage Regulator	KA7815,15V,0.5A
Octal Buffer	74LS22P
FPGA Processor	SPARTAN3E
Voltage Regulator	L7805CV,5V,0.5A
1 ϕ Induction Motor	100V,1.3A,1440RPM

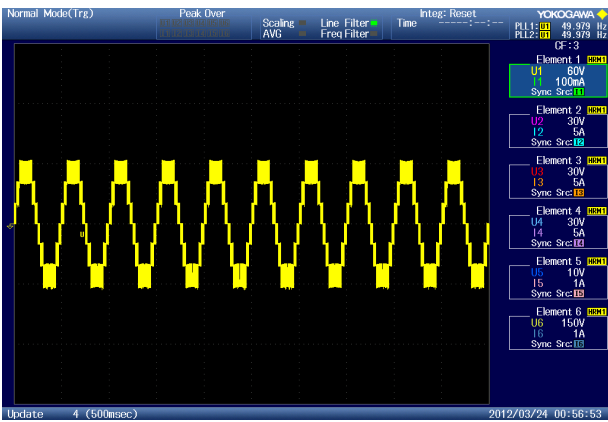


Figure 24. Output voltage of 7 level CMLI for motor load.

degree out of phase. Finally 6 carriers compare with sine signal and generated 12 pulses for single phase inverter.

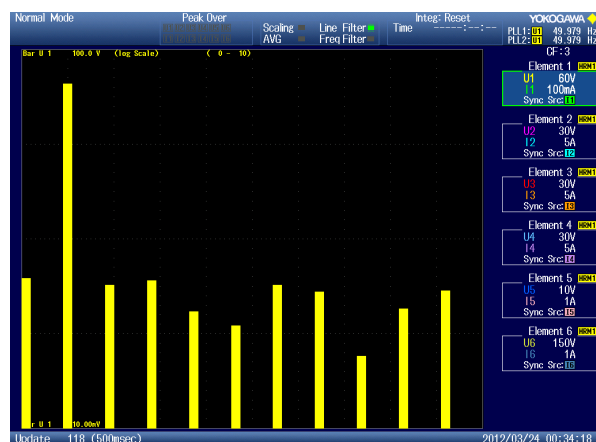


Figure 25. Output voltage harmonic spectrum.

Figure 24 shows the output voltage of 7 level CMLI connected to single phase induction motor. Figure 25 indicate output voltage harmonic spectrum waveform. From the result we conclude that THD value of 7 level CMLI voltage is 6.844%.

5. Conclusion

This paper proposes the simulation of 7 level Cascaded Multilevel (CMLI) with different PWM techniques such as phase disposition-bipolar, phase disposition-unipolar, phase shift-bipolar and phase shift-unipolar. The performance parameter such as THD, Voltage stress, load voltage, power factor, main winding current, auxiliary winding current, rotor speed, and electromagnetic torque compared for different modulation. From the comparison table phase shift bipolar modulation provides low THD value i.e. 5.45% in RL load. Phase shift unipolar modulation technique provides THD value of 1.57% when it is connected single phase induction motor load. Hence the prototype of 7 level CMLI was implemented using phase shift carrier bipolar modulation which gives output voltage THD is 6.844%. Therefore, Phase shift carrier modulation best suited for RL and motor load.

The work is limited due to there is no control over parameter such as speed and torque of the induction motor when it is loaded. This limitation can be overcome by implementing feedback control method using fuzzy pi hybrid controller.

This proposed concept is extended by use of renewable source like PV cell, Fuel cell with Maximum Power Point Tracking (MPPT) algorithm such as Perturb Observe P&O and Incremental Conductance (ICT).

6. References

1. Yamamoto T, Furuhashi T, Arai N, Mori K. Design and testing of the Organic Rankine Cycle. *Energy J.* 2001; 26:239–251.
1. Komolafe OA, Olayiwola OI. Gapped alternate phased opposite disposition pulse width modulation control for multilevel inverters. *ARN journal of engineering and applied sciences.* 2014 Apr; 9(4):560–7.
2. Rodriguez J, Lai J-S, Peng FZ. Multilevel inverters: a survey of topologies, controls and applications. *IEEE Trans Ind Appl.* 2002 Aug; 49(4):724–38.
3. Mosazadeh SY, Fathi SH, Radmanesh H. An overview of high frequency switching patterns of cascaded multilevel inverters suitable for PV applications and proposing a modified method. *Indian Journal of Science and Technology.* 2014 Sep; 7(9):1342–9.
4. Porselvi T, Muthu R. Seven-level three phase cascaded H-bridge inverter with a single DC source. *ARN journal of engineering and applied sciences.* 2012 Dec; 7(12).
5. Pate J, Kapadia R, Patel D. Simulation and analysis of Cascaded H-bridge multilevel inverter using single DC source. *International Journal of Emerging Technology and Advanced Engineering.* 2013 Apr; 3(4). ISSN 2250-2459.
6. Filho F, Tolbert LM, Cao Y, Ozpineci B. Real-time selective harmonic minimization for multilevel inverters connected to solar panels using artificial neural network angle generation. *IEEE Trans Ind Appl.* 2011; 47(5):2117–24.
7. Urmila B, Subbarayudu D. Multi level inverter: a comparative study of pulse width modulation techniques. *Int J Sci Eng Res.* 2010; 1(3):25.
8. Colak I, Kabalcı E, Bayindir R. Review of multilevel voltage source inverter topologies and control schemes. *International Journal on Energy Conversion and Management.* 2011; 52(2):1114–28.
9. Wanjekeche T, Nicolae DV, Jimoh AA. Realization of a nine - level cascaded NPC/H-bridge PWM Inverter using phase-shifted carrier PWM technique. *The International Conference on Electrical Engineering;* 18-20 March; Hong Kong; 2009. p. 1–6.
10. Bashi SA, Mailah NF, Kadir MZ, Leong KH. Generation of triggering signals for multilevel converter. *Eur J Sci Res.* 2008; 24(4):548–55.
11. Vijaya MK, Deekshit KKC. Comparison of hybrid PWM technique for cascaded multi-level inverter. *Int J Adv Sci Res.* 2012; 3(2):265–74.

12. Murugesan M, Sakthivel R, Muthukumaran E, Sivakumar R. Sinusoidal PWM based modified cascaded multilevel inverter. IJCER. 2012 Mar-Apr; 2(2):529–39.
13. Pandian G, Reddy SR. Simulation and analysis of multilevel inverter fed induction motor drive. Indian Journal of Science and Technology. 2009 Feb; 2(2).