Efficient VCO using FinFET

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Abstract

In this paper the two different architectures of voltage controlled oscillator using MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and FinFET are compared and analyzed. The comparison is on the basis of different parameters of VCO (Voltage Controlled Oscillator). The parameters which are analyzed are Voltage swing, Tuning Range, Power Consumption, number of stages and phase noise. Two architectures of VCO namely Current Starved Ring Oscillator and Source coupled VCO are implemented on Cadence Virtuoso simulator. The results of simulation indicated that implementation using FinFET, gives very high tuning range of VCO as compared to MOSFET. The Tuning range in Current starved VCO using FinFET is found out to be 23 GHz to 32 GHz compared to MOSFET which is only 3 GHz to 6 GHz. The phase noise in Source coupled VCO FinFET is better than MOSFET for low frequency domain. According to power consumption analysis, Source coupled VCO FinFET is much better than Source coupled MOSFET.

Keywords: FinFET, Mosfet, Oscillator, Phase Noise

1. Introduction

VCO is the most important and an indispensable part of any electronic systems ex. PLL (Phase Locked Loop). The application of PLL is generating clocks of variable frequencies which are essential for any system. So VCO is the most important part of PLL. Voltage Controlled Oscillator (VCO)¹ as the name suggests controlling oscillations using voltage. Oscillation is mainly characterized by amplification of unwanted or noise signals without any external input. By intuition it can also be interpreted that oscillations mainly produced due to charging and discharging of Load capacitance. Every oscillatory motion mainly depends on the frequency. If the frequency of oscillation is controlled by external input i.e. voltage then the oscillator block or circuit is called Voltage Controlled Oscillator. Oscillations can be produced using ring based topology or LC based tank circuit. There are two major topologies of VCO viz Ring Oscillator and LC Tank Circuit. The principle behind oscillation is positive feedback. If a signal has a positive feedback to the input it will create a regenerative effect on input side for sustaining oscillation. There is a tradeoff between Ring Based topology and LC tank Circuit in terms of parameters. If high frequency is a main constraint then phase noise is poor and if phase noise is a constraint then Frequency range is poor. Ring oscillator provides high frequency range but poor phase noise while LC Tank circuit gives better phase noise but poor frequency range. LC based VCO has inductors and capacitors as its primary circuit elements so it works on one resonant frequency which is the frequency of inductor and capacitor so the frequency range is reduced. The power consumption which is prime important in today's electronic systems is more in LC Tank as compared to ring oscillator circuit. In ring oscillator the power varies strongly due to current variation. To have a better phase noise power consumption is more in ring oscillator. On other hand in case of LC Tank the power consumption is higher for getting the same frequency range but for better phase noise power consumption is lower. The gain of ring oscillator is high and independently affected by supply source noise injection

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but LC has lesser gain and strongly depends upon supply noise rejection. As the size of the inductor is more the layout area is more as compared to ring based oscillator. This creates complexity in integration in case of LC tank circuit. On the basis of merits and demerits discussed above Ring oscillator is mainly used for digital chip as wide frequency range is one of its advantages while LC tank circuit is mainly used for RF IC Design because of its stability due to better phase noise. As system size is reducing day by day so there is a need of smaller devices which forms the least size systems. As transistors are the basic building block of any circuit so reducing its size is mandatory. MOSFETs are continuously scaling down in recent years but as the size reduces the SCE (Short channel effect) becomes more dominant. FinFET which is nonplanar transistor gives better performance as compared to MOSFET. The SCE (Short channel effect) is greatly reduced due to FinFET. FinFET basically having multiple gates over the channel reduces the off current provides a reduced sub-threshold leakage as compared to MOSFET. Due to the continuously reduction in the channel length the control over the channel is reduced. MOSFET² suffers with this limitation. FinFET4 has multiple gates so control over the channel is more hence it is best suited for high speed applications. The current driving capability of FinFET5 is more as compared to MOSFET. High current driving results in fast charging and discharging of the load capacitor which results in high frequency reduced time period. Ring oscillator frequency is characterized by number of stages and time delay of each inverter in a inverter chain. Mathematically it can be written as: $f = 1/(2 \times n \times t_d)$ where, N = number of stages and t_d is time delay of each inverter. Following sections illustrates more detailed explanation on VCO and the two different architectures. Section 2 gives a detailed explanation of two different architectures of VCO:

Current Starved Ring Based VCO and Source Coupled VCO. Section 3 deals with analyses and discussion of the architectures for different parameters of VCO. Finally conclusion is drawn in Section 4.

2. Architectures

2.1 Ring Oscillator

Ring oscillator⁶ as the name suggests oscillations due to a ring circuit. It consists of ring of inverters with odd number of stages without any external input voltage. The successive stages are connected as the output of one stage is fed to the next stage input. This cyclic fashion continues and the output of the last stage is fed back to the input of first stage⁷. At the connection of each preceding inverter and following inverter comprises of three major capacitances as Cox-oxide capacitance, output capacitance at the drain of preceding inverter and input capacitance of following inverter. The oscillations are produced due to charging and dis-charging of these capacitances. The oscillation frequency of Ring oscillator8 is related with number of stages and the time required to charge and discharge the capacitance called as delay of each cell. These parameters have an inverse relationship with frequency and can be expressed as in equation 1.

$$f = 1/(2 \times n \times t_d) \tag{1}$$

So to have wide frequency range the number of stages should be less. This oscillating behavior can be controlled by a voltage which results in Voltage Controlled Oscillator. The VCO can be built using various architectures. Two of them are discussed in the next sections.

2.2 Current Starved Voltage Controlled Oscillator

The Figure 1 shows the topology, which consists of ring based³ connection of odd number of inverters along with the current mirror circuit and additional transistors which can act as a current source to the inverter chain. The figure 2 shows the FinFET current starved circuit. As shown in the topology the middle transistors forms the chain of inverters, the topmost and bottommost transistors forms the current source to the inverters. The leftmost transistors form the current mirror circuit which is controlled by the input voltage. This current produced by the input voltage is mirrored to the upper-most and bottommost transistors as shown. These transistors act as current sources to the inverter chain. Hence the current to inverter is limited so inverter starves for the current. This current is produced by the input voltage hence the oscillations are controlled by the voltage forming the Voltage Controlled Oscillator. The design equations can be analyzed as follows:

Let us take one stage of current starved VCO. The capacitance at the output of the drain of T2 and T3 which are called input and output capacitance of inverter in equation 2.

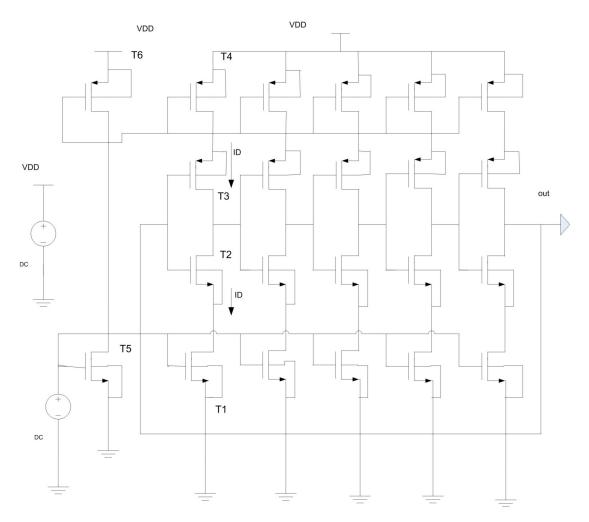


Figure 1. Current starved ring VCO using MOSFET.

$$C_{tot} = C_{out} + C_{in} = C'_{ox}(W_{pLp} + W_{nLn}) + 2C'_{ox}(W_{pLp} + W_{nLn})$$
(2)

• As constant current flowing through the transistors the capacitor which is at the output of inverter is charged to the voltage developed across the source of T3. The time required to charge and discharge it is in equations 3 and 4.

$$T_{charge} = C_{tot} \times \begin{pmatrix} V_s \\ I_{d4} \end{pmatrix}$$
 (3)

$$T_{discharge} = C_{tot} \times \left(V_{dd} - V_{s} / I_{d1} \right)$$
 (4)

• If the currents $I_{d4} = I_{d1}$, then the total time to charge and discharge the capacitor (C_{tot}) in equation 5.

$$T_{charge} + T_{discharge} = C_{tot} \times \begin{pmatrix} V_{dd} / I_{d} \end{pmatrix}$$
 (5)

where, $I_{d} = I_{d1} = I_{d4}$

Therefore frequency of oscillation for N stages (N> =
 5) can be given in equation 6.

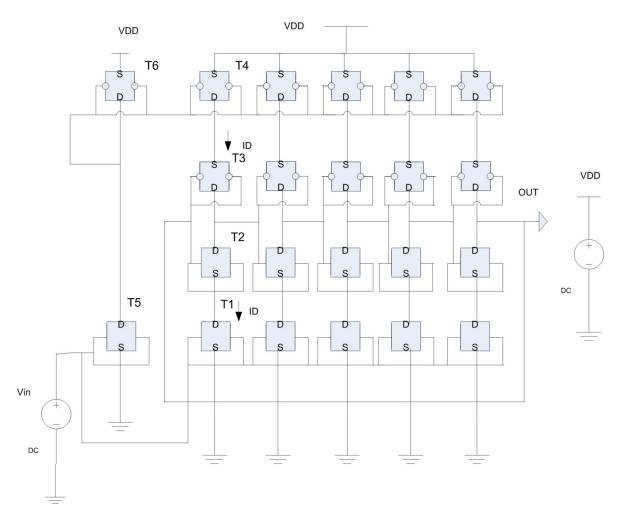
$$fosc = \frac{1}{N \left(T_{charge} + T_{discharge} \right)} = \frac{I_d}{\left[(N \times C)_{tot} \times V_{dd} \right]}$$
(6)

- The F_{max} and F_{min} are called as the maximum and minimum frequency of VCO. F_{max} is the frequency of oscillation when $V_{in} = V_{dd}$. Where V_{in} is input voltage to VCO. F_{min} is the frequency of oscillation when $V_{in} = V_{thn}$, where V_{thn} is the threshold voltage of transistor.
- To calculate the power dissipation by the VCO the average current should be found out which is given in equation 7.

$$I_{avg} = N[(f_{osc} \times C]_{tot} \times V_{dd}$$
(7)

Therefore power in equation 8 is given as,

$$p = I_{avg} \times V_{dd} \tag{8}$$

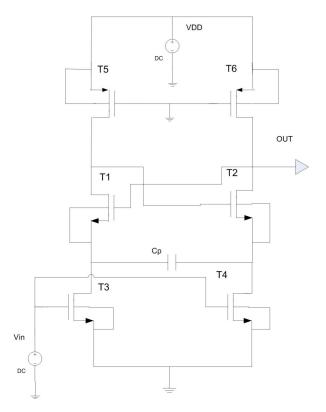


Current starved ring VCO using FinFET.

This power excludes the power in the mirror circuit. If the power in mirrored transistors are also considered then power doubles.

2.3 Source Coupled Voltage Controlled **Oscillator**

Another architecture of VCO(9) is shown in figure 3 and figure 4 If low power is a constraint this circuit is better suited as compare to the current starved VCO discussed above at the frequency of interest. The disadvantage of this circuit is the use of capacitor because of its parasitic nature and also the reduced output swing. There can two forms of this circuit viz. NMOS Source Coupled VCO and CMOS Source Coupled VCO. The difference between the two is that in case of NMOS based the output which is shown in the fig is pulled to $\rm V_{\rm dd}$ - $\rm V_{\rm thn}$ while in case of CMOS based the output is maintained at V_{dd} by the transistors T3 and T2 respectively. The transistors T5 and T6 act as current sources while the transistors T1 and T4 act as switches. If transistor T1 is off then T2 is on and the drain of T1 is raised to $V_{_{\mbox{\footnotesize dd}}}$ - $V_{_{\mbox{\footnotesize thn}}}$ by T3. The threshold voltage is affected by the body effect which is called as body bias effect. Hence if the threshold voltage is high then the output swing is reduced because the source and drain of T2 will be reduced to $V_{\mbox{\tiny dd}}$ -2V $_{\mbox{\tiny thn}}\!\!,$ a much reduced voltage swing. So to avoid reduction in swing an inverter is placed at the output of the circuit. The output voltage as shown is V_{dd} - $2V_{thn}$ as discussed above and is remained at this voltage until T1 turns on and T2 turns off. The point A is at V_{dd} - V_{thn} initially when the T1 is off and T2 is on. Therefore the current through the capacitor tends to degrade the voltage at point A towards ground. As the voltage degrades to $V_{\rm dd}$ - $3V_{\rm thn}$ then T1 is on and T2 is off.



Sourced coupled VCO using MOSFET.

So there is total change of 2V_{thn} at point A. Oscillations are basically produced due to change of voltage at point A and B. Therefore the time takes to change voltage at A by $2V_{thn}$ is given in equation 9 as,

$$T = C \times 2 \times \frac{V_{thn}}{I_d} \tag{9}$$

Due to symmetry of the circuit the frequency of oscillation in equation 10 is calculated by

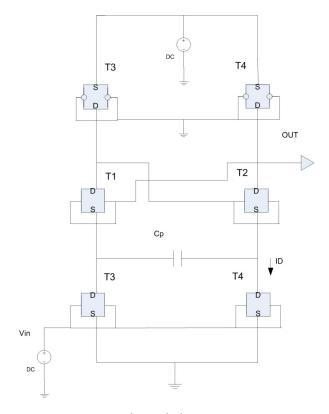
$$f_{osc} = \frac{1}{(2 \times T)} = \frac{I_d}{(4 \times C \times V_{thn})}$$

$$\tag{10}$$

In this way oscillations are produced in Source Coupled Voltage Controlled Oscillators. An important point is that the transistors T3 and T2 are long Transistors. Following section discusses the comparison of FinFET and MOSFET in case of various parameters of VCO.

3. Results and Discussion

The two topologies are compared on the basis of following parameters with FinFET and MOSFET as the implementing Transistors.



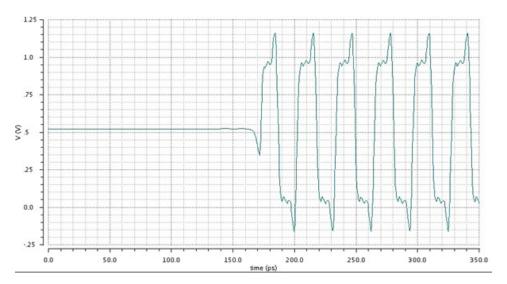
Sourced coupled VCO using FinFET.

3.1 Output Voltage Swing

The difference between the maximum output and minimum output is called output swing. The output swing is a crucial factor in analog circuits as this is the voltage which is used to drive the subsequent stages. The output swing in case of MOSFET Based Current Starved VCO is 1.15V while in case of FinFET the output swing is 1.323V which is definitely an improvement. Considering the MOSFET Based source coupled VCO. The output swing is 200mV while in case of FinFET the output swing is 551mV which is again an improvement. The reduced voltage swing in source coupled VCO is due to the threshold voltage which is the main component in output. The values indicate that the FinFET is better than MOSFET in case of output voltage swing in a respective circuit. Figure 5 shows the oscillation of current starved circuit using FinFET and figure 6 shows the oscillation of source coupled circuit using FinFET.

3.2 The Tuning Range

The Tuning range means the range of frequencies lies between the minimum and maximum frequency. Wide



Oscillations of current starved using FinFET.

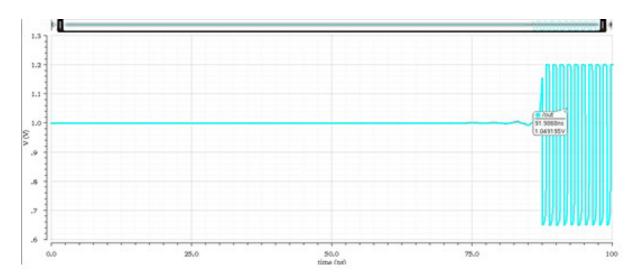
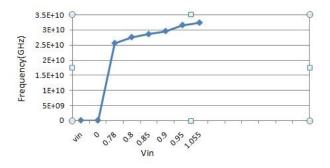


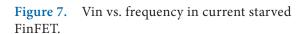
Figure 6. Oscillations of source coupled VCO using FinFET.

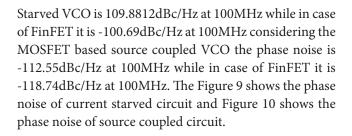
frequency range(10) is very important in high speed applications. To get a wider range of frequency ring oscillator topology is best suited as discussed above. The maximum and minimum frequency in case of MOSFET based Current Starved VCO is 6.535GHz and 4.087GHz respectively while in case of FinFET it is 32.42GHz and 22.95GHz respectively which is definitely an improvement. Considering the MOSFET Based source coupled VCO The maximum and minimum frequency are 0.603GHz and 0.12GHz respectively while in case of FinFET maximum and minimum frequency are 1.34GHz and 0.191 GHz respectively which is again an improvement compared to MOSFET. The reason behind it is the current driving capability of FinFET which is far superior thanthe MOSFET. The following figure 7 and figure 8 shows the variation of input voltage with respect to frequency of current starved circuit using FinFET.

3.3 Phase Noise

Phase noise means the generation of same frequency at a specified period of time. Phase Noise results from the changing phase of the noise sources modulating the oscillation frequency center around the frequency stability. The phase noise in case of MOSFET Based Current

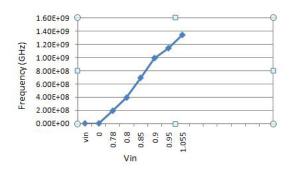






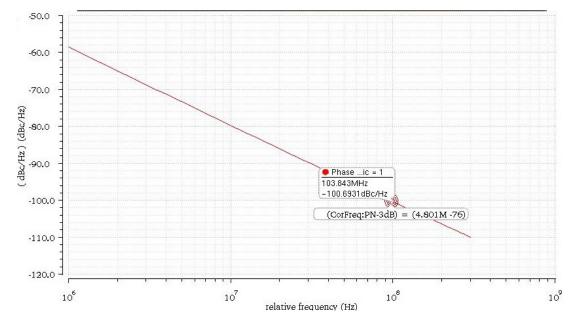
4. Conclusion

The various parameters of Voltage controlled oscillator are been analysed using two different architectures. The



Vin vs. frequency in source coupled Figure 8. FinFET.

architectures are compared on the basis of two types of transistors, planar and non-planar. The planar transistor is MOSFET and non-planar Tri-Gate FinFET. The wide frequency range is emphasized more than the phase noise. So we implemented ring oscillator based current starved VCO and source coupled VCO because they are better for wide frequency and better phase noise respectively. The high tuning range is achieved for FinFET as compared to MOSFET, phase noise is also better compared to MOSFET. Previous works are analyzed using double gate FinFET, we have implemented VCO in Tri-Gate as high frequency is achieved so it is better for high speed applications.



Phase noise of current starved using FinFET.

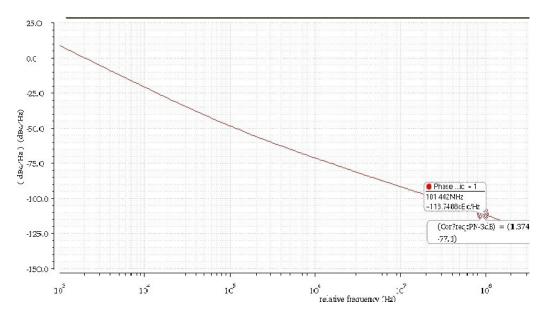


Figure 10. Phase noise of source coupled VCO using FinFET.

Table of comparison Table 1.

Parameters	MOSFET Current Starved VCO	FINFET Current Starved VCO	MOSFET Source Coupled VCO	FINFET Source Coupled VCO
Technology node	45nm	45nm	45nm	45nm
Output Swing	1.15V	1.323V	0.2V	0.551V
Tuning Range	4.087GHz-6.535GHz	22.95GHz- 32.42GHz	0.12GHz-	0.191GHz-
			0.603GHz	1.34GHz
Phase Noise	-109.88	-100.69	-112.55	-118.78
	dBc/Hz at 100MHz	dBc/Hz at 100MHz	dBc/Hz at 100MHz	dBc/Hz at 100MHz
Gain (Kvco)	1.06	4.27	0.21	0.51
Power Dissipation (uw)	-	50.51	38	29

5. References

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