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A High Performance Asynchronous Counter using Area and Power Efficient GDI T-Flip Flop

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Abstract

As the technology is increasing day by day in electronic industry, it needs a field which involves packing more and more devices into smaller area. Along with Very Large Scale Integration (VLSI) is a process of integrating much number of devices into a single chip. According to Moore's law the competence of an IC has increased in terms of power, speed and area. Hence the GDI technique is used here, in which many complex logic functions can be designed by using only two transistors. Along side, the memory device plays an important role in digital systems, where the flip flops are the basic building blocks of digital electronic systems. Asynchronous logic in digital system does not use common clock pulse, in place the precious state output will be considered as clock pulse to the next state. Based on the concept of T-flip flop, a new GDI T-Flip flop is designed, which has less number of transistors than other GDI T-flip flops and also, it consumes low power and lesser delay. With this energy efficient GDI T-Flip flop, a high performance Asynchronous down counter is developed in this paper. The comparison is done on the basis of four performance parameters i.e. total Area, delay, Power consumption and power-delay product.

Keywords: CMOS, Counters, FinFET, GDI, MOSFET, T-flip flops

1. Introduction

Area and energy efficient circuits are always needed for VLSI. By using CMOS technology the area and energy efficient circuits can be made. Generally in VLSI, there are three important parameters to measure the quality of all the circuits, which are area, power and delay. Also due to the advancements in CMOS technology the VLSI circuits are concentrating only on improving the area, power and delay. But there will be always trade off exists between area, power and delay in a circuit[1]. The CMOS logic has two different families, which are: 1. Static and 2. Dynamic logic[2,3]. The most widely used logic is static, which has two networks pullup and pulldown. In other words this pullup and pulldown networks are the extension of CMOS inverter with multiple number of inputs. The pullup and pulldown networks restore the logic 1 and 0, so that this logic can be static. This static logic has high reliability and easy to design. But the main disadvantage of this static logic is, more number of transistors are needed to build the circuits[4]. So that the area and delay will be increased. Hence pseudo nMOS logic is introduced. This is also called as ratio logic. It requires only less number of transistors and the gate of pulldown network will be grounded, thus the power consumption will also be reduced. But the main drawback of this logic is non zero static power dissipation. Thus to obtain the better performance in CMOS circuits many logic designs were found. Among those logics the PTL is one of the logic which is used to overcome the drawback of CMOS technology. The advantage of PTL is 1) high speed due to less area, 2) low power consumption due to less number of transistors, 3) Since the logic has low area the interconnection effect will also be very less[5]. There are many sorts of PTL techniques that aims to solve the problems mentioned below[6].

Transmission gate CMOS (TG) consists of transmission gate, in which one pMOS and one nMOS transistors will be connected parallel and the complement inputs will

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be given to the gate of both the transistors. By using this TG low logic level swing can be reduced.

Complementary Pass-transistor Logic (CPL) gives the complementary inputs and outputs to the nMOS pass transistor with CMOS output inverters. But this logic suffers from static power consumption. To avoid this problem LCPL and SRPL logic styles are used. It reduces the static power consumption, since these styles contains pMOS transistor. Here the pMOS transistor will be acting as restoration circuit.

Double Pass-transistor Logic (DPL) is introduced to remove the necessity of restoration circuit, since it operates at full swing and also reduces the dc power consumption. Hence the Gate Diffusion Input (GDI) technique is used here. The GDI approach allows implementing wide range of complex logic functions using only two transistors. So that the GDI logic is suitable for designing fast and low-power circuits, with reduced number of transistors as compared to CMOS and existing PTL techniques.

The recent trend in electronic industry is to provide the portable devices with less power consumption. Even for the non portable devices also the power consumption should be very less, because of increased area and cooling cost as well as reliability. Thus the main aim of VLSI engineers is to make the products within the assumed power budget. Therefore the efficiency in power can be assumed as major concern. FinFET is an emerging transistor technology which is likely to replace the bulk CMOS at 22nm and beyond, also it offers interesting delay and power tradeoff. The pMOS and nMOS transistor are developed for CMOS and pass transistor logic. In FinFET, NFinFET and PFinFET will be used instead of nMOS and pMOS in CMOS logic. Here ther gate of both transistors will be tied together. By using this approach, we can design a FinFET version of a CMOS logic circuit or a pass transistor logic circuit that retains the same functionalities as the MOSFET version. In the mean time, FinFET provides better circuit performances and reduces leakage current through effective suppression of short-channel effect and near-ideal subthreshold swing[7].

2. Gate Diffusion Input Logic

2.1 GDI Basic Cell

The basic GDI logic cell is shown in Figure 1. In this the basic cell looks like a standard CMOS inverter, but the operation completely differs from CMOS inverter[8].

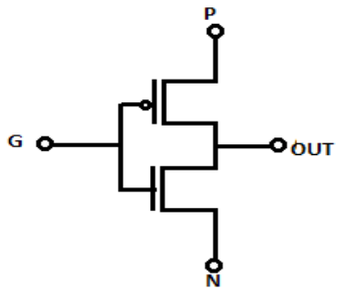

Figure 1. GDI Basic cell, which has three inputs: G, P, N and one output.

1) The GDI basic cell consists of three inputs: G (common gate input of both nMOS and pMOS), P (input to the source or drain of the pMOS), and N (input to the source or drain of the nMOS).
2) Since the bulks of both pMOS and nMOS are connected to N and P respectively, this GDI cell will be biased in difference with standard CMOS inverter.

2.2 GDI AND

From the Figure 2 the operation of GDI AND can be evaluated as follows: The P of the transistor will be given as 0, so that it goes to off state. Hence either logic 0 or logic 1 appears at the input, and the same will be reflected at the output. Therefore the output will be z=a*b.

2.3 GDI OR

From the Figure 3, the GDI OR function can be evaluated as follows: When N of the GDI cell is 1, then the input of the OR gate A also will be 1, and output will be equal to N.

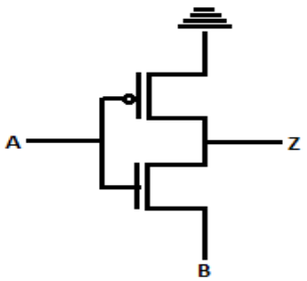

Figure 2. GDI AND cell has two inputs A and B and one output Z. Here input to the source or drain of pMOS is grounded.

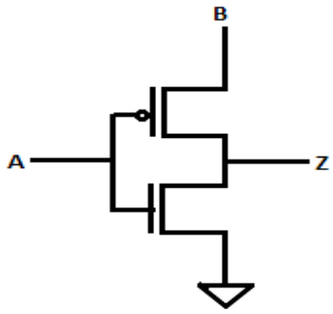

Figure 3. GDI OR cell has two inputs A and B and one output Z. Here the Vdd supply is given to input to the source or drain of nMOS.

Therefore a∗1=a, in the same way for a=0. Hence b will be given at the output as a∗b, Therefore a+a∗b = a+b.

2.4 GDI EX-OR

In Figure 4, the GDI Ex-OR function has been evaluated. When the inputs a=1, b=0, then the output will be 0 and it will be connected to N of second transistor, when the pMOS (first transistor is turned on) then the output will be a*b. In the same way for the inputs a=0 and b=0. Hence the final output will be a∗b+ab∗.

3. Flip Flop

Flip flop's can be considered as basic building block of communication and digital systems. It has two stable states and the main purpose of the flip flop is to store one bit information. The states will be changed when an external triggering pulse is applied to the circuit. So that it can also be called as storage device. Flip flops can be clocked or not clocked. The clocked ones are called as flip flops, not clocked ones are called as latches. Different types of flip flops are available, where T flip flops are mainly used to design the counters, which counts the number of states or clock pulses. It produces the output which is alternate to the input when clock pulse is applied[9]. The characteristic table for toggle or T flip flop is described in Table 1.

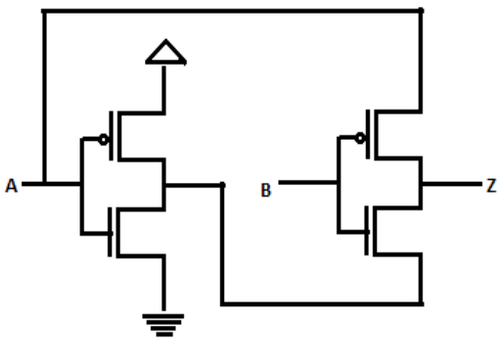

Figure 4. GDI EX-OR cell has two inputs and one output, Here the first input A is given to the inverter cell and the second input B is given to next cell.

4. Comparisons of T-flip flop

4.1 Conventional T-flip flop

This is equivalent with, if T is "0", the state will not change and if T is "1" then flip flop will change state or toggle. This conventional CMOS based T-flip flop in Figure 5 has 48 transistors and it consumes more power.

4.2 T-flip flop using GDI Gates

The (Figure 6) has connection of two latches (master-slave). In this each and every gates are based on GDI technique and here two three input GDI and gates, four two input GDI nor gates and two, two input and gates are used. This circuit contains 30 transistors.

4.3 T-flip flop using GDI multiplexer(Existing T-FF)

The components in the latch circuit can be divided into two main categories; GDI gate and inverter. GDI gate uses two transistors and controlled by the clock signal. Clock signals is fed to the gate of transistors and create two alternative states: one state is when the Clock is low then the signals will be passing through pMOS transistor and creates temporary state and other one is when the clock is high the nMOS transistor will be turned on and the prior values will be maintained in the same state, due to conduction of the outputs. Here the Figure 7 has five GDI gates. This GDI gates based T flip flop has 24 transistors[10].

Table 1. The characteristic table for a toggle or T-flip flop

	T	Q(t+1)
No change	0	Q(t)
Toggle	1	$\overline{Q}$(t)

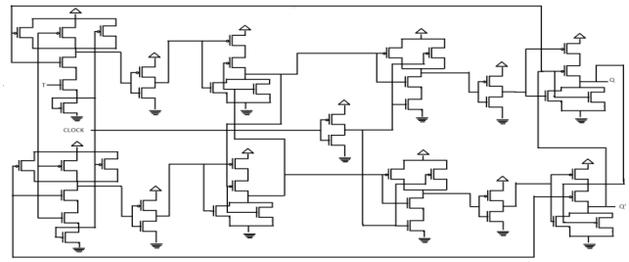

Figure 5. T-Flip flop based on cross-coupled NOR gates.

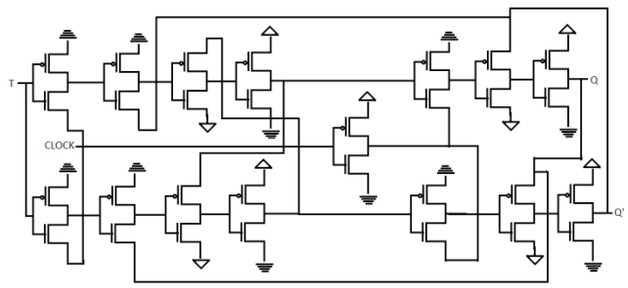

Figure 6. Conventional T flip flop using GDI logic gates.

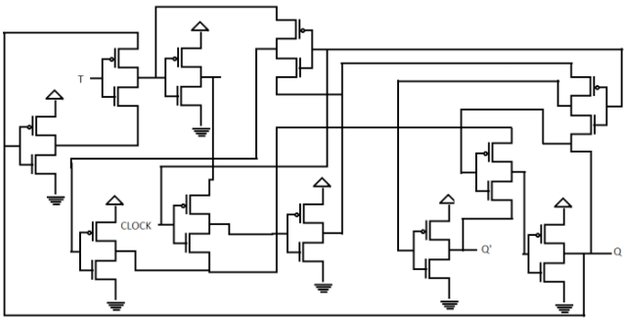

Figure 7. GDI T-flip flop using multiplexer.

4.4 Proposed T flip flop using GDI

The Proposed GDI T-FF is shown in Figure 8, which consists of two latch circuits. Each latch consists of two categories; GDI gate and inverter. GDI gate uses two transistors and controlled by the clock signal. Clock signals fed to the gate of transistors and create two alternative states in which one state is when the clock is low and the signals will be passing through pMOS transistor and creates temporary state and other one is when the clock is high, nMOS transistor will be turned on and the prior values will be maintained in the same state due to conduction of the outputs. In this state, GDI gates holding state of the latch. The existing Flip flop is made by using five GDI gates, but the proposed flip flop has only three

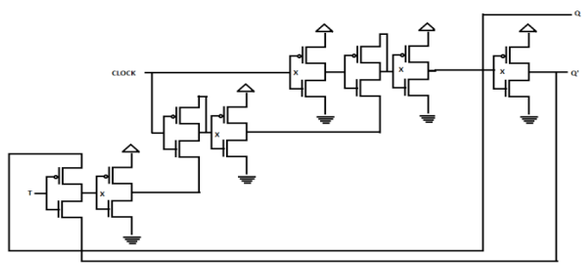

Figure 8. Proposed GDI T-flip flop with less number of transistors.

GDI gates and it is more efficient than proposed method in terms of power and area. This GDI gates based T flip flop has only 16 transistors.

5. Counters

Counters are designed using flip flops. Counters counts the number of clock pulses or inputs, in which the number of bits in counter is based on number of flip flops which is used to design the counter. For example to design a 3 bit counter 3 flip flops are needed. The digital system can be divided into two types: 1. Combinational, 2. Sequential. A combinational circuit does not use clock pulses where as sequential circuits use clock pulses. Sequential circuits can be divided into two types, 1. Synchronous logic, 2. Asynchronous logic. The Synchronous logic uses common clock pulse for all the circuits, where as the asynchronous logic uses only one clock pulse for a circuit, the output of the first circuit can be taken as clock pulse to the next circuit. Asynchronous counter can be up, down and up/down. The 3 bit asynchronous down counter is designed by using 3 T flip flops[11] as shown in figure 9.

6. 3-bit Counter Design using Various Flip Flops

These are the counter designs using various flip flops. In this, the Figure 10 shows the counter designed using conventional T flip flop and totally it has 144 transistors. Figure 11 shows the counter using T flip flop using multiplexers and it has 68 transistors. Figure 12 shows the counter using GDI T flip flop and it has 90 transistors. Finally the Figure 13 shows the counter using proposed GDI T flip flop and it has only 48 transistors. So the counter using proposed GDI T flip flop is the efficient one when compared to the other designs.

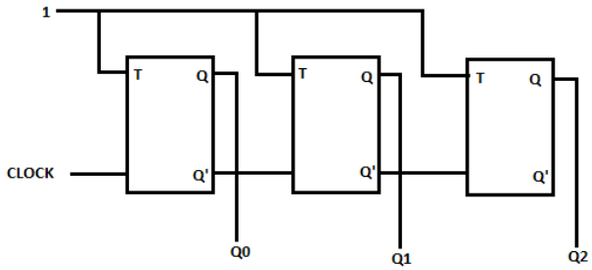

Figure 9. 3 bit Asynchronous counter using T-Flip flop.

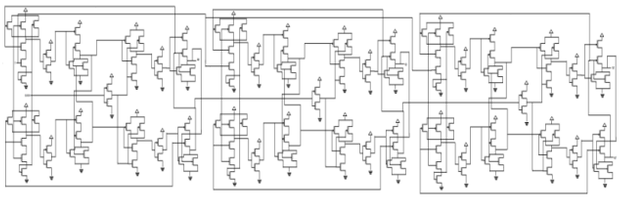

Figure 10. Counter design using conventional T-flip flop.

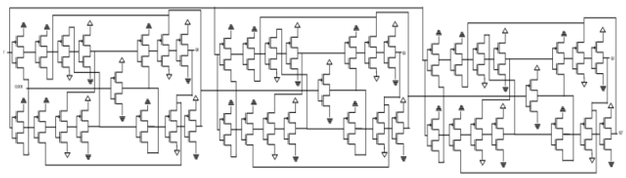

Figure 11. Counter design using T-flip flop using multiplexers.

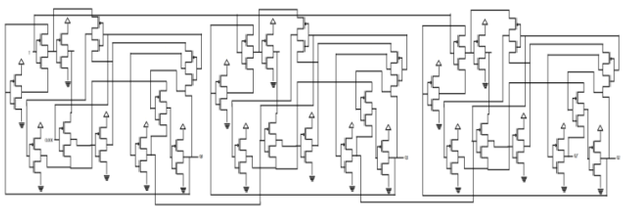

Figure 12. Counter design using GDI T-flip flop.

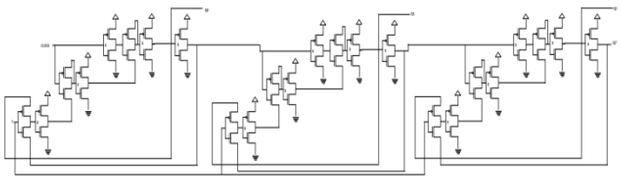

Figure 13. Counter design using proposed GDI T-flip flop.

7. Simulation Results

The Figure 14 shows the simulation results, in which the first signal is the input signal of the flip flop, second signal is the clock, third signal is the output Q, and fourth signal is the output Q bar.

The Figure 15 and 16 shows the simulation results for existing and proposed GDI counters. In which the first signal is the clock signal and second signal is the input to the all flip flops which is tied to be always high, and third signal is the output Q and fourth signal is the output Q bar.

8. Comparison Table and Charts for Various T-Flip Flops and Counters

Table 2 shows the area and power comparison for proposed T-FF and other methods.

The Figure 16 and 17 shows the area and power comparison charts for various flip flops. Table 3 shows the area and power comparison table for both existing and proposed GDI asynchronous counters. Figure 18 and 19 shows the area and power comparison chart for existing and proposed GDI asynchronous counters. The Table 4 shows the area, power and power delay product for existing and proposed T-FF using both MOSFET and FinFET technologies. The Figure 20 and 21 shows the area, power and Power Delay Product (PDP) comparison charts for flip flops and counters using both MOSFET and FinFET technologies. Table 5 shows the area, power and PDP comparison for counters GDI counters using both MOSFET and FinFET technologies.

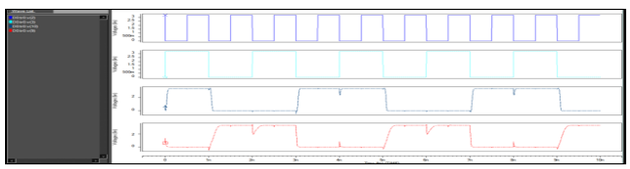

Figure 14. Simulation result for proposed GDI T FF.

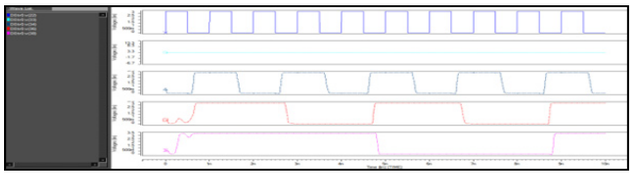

Figure 15. Simulation result for proposed GDI counter.

Table 2. Comparison table for Proposed T-FF and other methods

Circuit	Number of transistors	Power[mW]
Proposed GDI T FF	16	0.02331
T FF usibg GDI MUX	24	0.08212
T FF using GDI gates	30	0.3949
T FF using CMOS technique	48	0.4564

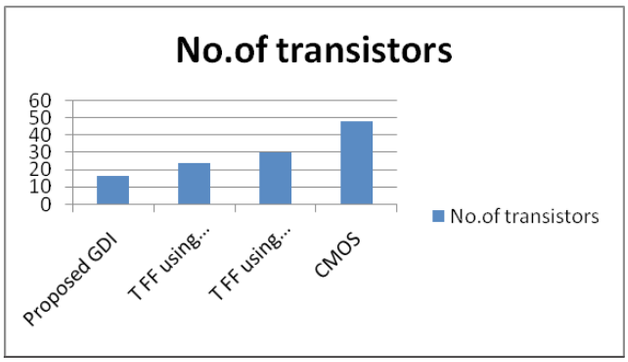

Figure 16. Area comparison chart for various flip flops.

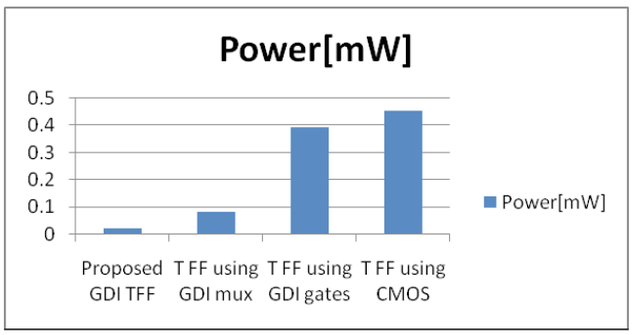

Figure 17. Power comparison chart for various flip flops.

Table 3. Comparison table for existing and Proposed GDI asynchronous counters

Circuit	Number of Transistors	Power[mW]
Proposed GDI counter	48	0.1193
Existing counter	72	0.1322

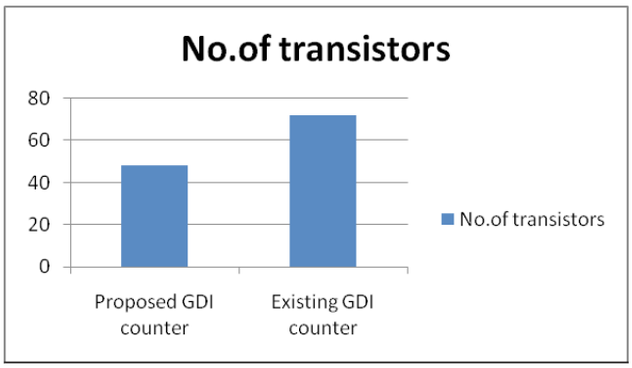

Figure 18. Area comparison chart for Existing and Proposed GDI counters.

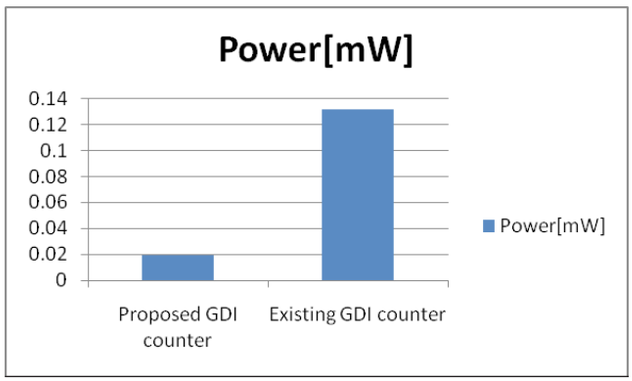

Figure 19. Power comparison chart for Existing and Proposed GDI counters.

Table 4. Power, Delay and PDP comparison for T FF using MOSFET and FinFET

	Power(w)	Delay(ps)	PDP(J)
Mosfet	2.331e-05	14.36	$3.3473x10^{-16}$
Finfet	8.290e-08	2.897	$2.4016x10^{-19}$

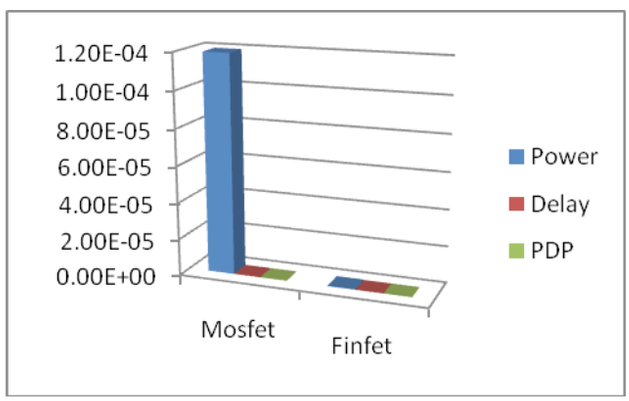

Figure 20. Power, Delay and PDP comparison chart for T FF using MOSFET and FinFET.

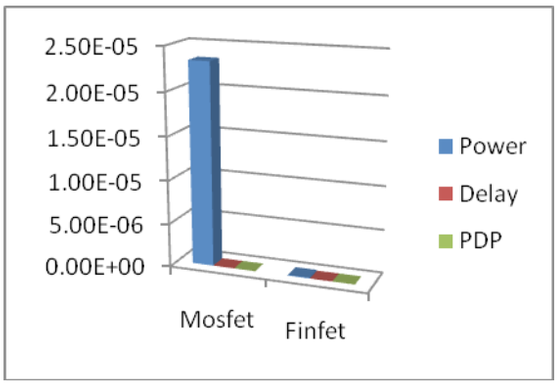

Figure 21. Power, Delay and PDP comparison chart for GDI counters using MOSFET and FinFET.

Table 5. Power, Delay and PDP comparison for GDI counters using MOSFET and FinFET

	Power(w)	Delay(ps)	PDP(J)
Mosfet	$1.193x10^{-4}$	295.92	$3.53032x10^{-14}$
Finfet	$2.262x10^{-7}$	87.25	$1.9735x10^{-17}$

9. Conclusion and Future Research

A new high performance asynchronous counter is implemented by using area and power efficient GDI T-FF. The proposed counter structure has very less number of transistors, since the efficient GDI T-FF has only 16 transistors. The circuit is implemented in both 130 nm MOSFET and 20nm FinFET technology and the simulation results are showed using HSPICE software. The performance comparisons has been made for both existing and proposed counters interms of area, delay, power and Power Delay Product (PDP). The future research activities may include integration of the proposed GDI counter in complex digital systems such as combining sequential and combinational logic.

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