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Low Loss 2-bit Distributed MEMS Phase Shifter using Chamfered Transmission Line

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Abstract

Objectives: The objective of this paper is to design a 2-bit DMTL phase shifter with low insertion loss, improved phase shift per dB loss with minimum number of switches. **Methods/Analysis:** In order to reduce the insertion loss tapered impedance section proposed previous researchers introduces impedance discontinuity at the end of the taper that introduces a fringing capacitance at the transition region which cannot be neglected while calculating the loaded line capacitance. The proposed chamfered transmission line design for phase shifter overcomes this shortcoming with a uniform high impedance line that does not have any discontinuities and causes variations of propagation constant along the length of the transmission line. The proposed design also reduces the discontinuity effects associated with step width junction and reflection is much reduced. **Findings**: Chamfering the corners at the contact area of switch with the transmission line reduces the discontinuity effects associated with step width junction. The achieved phase shift is 178.87o at 17GHz with an insertion loss of -0.87dB and return loss in both up, down states less than -15dB. Design and simulation results of the phase shifter with respect to pull-in voltage of the switch, RF characterization is done using Coventorware and HFSS.

Keywords: Chamfered, Co-Planar Waveguide (CPW), Distributed MEMS Transmission Line (DMTL), Pull-In, Lift-Off, Radio Frequency Micro Electro Mechanical Systems (RF MEMS)

1. Introduction

Recent advancement in Radio Frequency (RF) Micro Electro Mechanical Systems (MEMS) has great impact on improved performance of RF switches, variable capacitors and phase shifters. Phase shifters are essential for the completeness of communication and radar systems. MEMS sensors and actuators demonstrated every possible sensing modality in biomedical field due to their compactness1,2. Low insertion loss, low power consumption, high isolation and high linearity makes MEMS concepts adaptive for the development of RF passive components as compared to FET or P-i-n diode at millimeter wave frequencies[3]. The Distributed MEMS Transmission Line (DMTL) is a low loss, low cost, high impedance transmission line that is loaded periodically using MEMS bridges that act as a shunt capacitors. electrostatic force created by the application of DC voltage between the beam (movable electrode) and center conductor (fixed electrode) brings down the bridge there by raising the net capacitance resulting in a phase shift with respect to zero dc bias[4,5]. This paper analyses digital DMTL phase shifter based on chamfered CPW transmission line with maximum phase shift per dB loss. The Digital MEMS distributed phase shifter of this work is designed on a high impedance CPW line (Zo = 65Ω, G/W/G = 150/100/150μm) by periodically placing a series connected MEMS bridges and MAM capacitors that influences the capacitive loading of the line. Variations in capacitive loading of the

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transmission line affect the line loss which in turn alters the impedance. Change in impedance of the line brings in phase shift which modifies the reflection co-efficient of the phase shifter. The phase shift is given by

$$\Delta\phi = \frac{s\omega Z_o\sqrt{\varepsilon_{r,eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \quad \ldots (1)$$

where, Zld and Zlu are upstate and downstate impedances of loaded line.

2. Design of CPW Transmission Line

The goal of this paper is to design a DMTL phase shifter with low insertion loss operating up to 20GHz. The design requires an accurate modeling of transmission line and distributed loading capacitance of MEMS bridges. The unit length capacitance Ct and inductance Lt of unloaded transmission line are given by

$$C_t = \frac{\sqrt{\varepsilon_{eff}}}{cZ_o} \quad \ldots (2)$$

$$L_t = C_t Z_o^{\,2} \quad \ldots (3)$$

where, ἐff and Zo are the effective dielectric constant and characteristic impedance respectively. The impedance Z_l and phase velocity v_l of the loaded line are

$$Z_l = \sqrt{\frac{L_t}{C_t + C_b/s}} \quad \ldots\ldots\ldots\ldots (4)$$

$$v_l = \frac{1}{\sqrt{L_t(C_t + C_b/s)}} \quad \ldots\ldots\ldots\ldots (5)$$

Where, s is the periodic spacing of the MEMS Bridge and Cb is the distributed MEMS capacitance of loaded line. In this paper, CPW transmission line is designed on silicon substrate with impedance of 65Ω where (W+2G) is 400μm. Equally spaced 8 and 16 shunt capacitance switches for 90° and 180° sections are placed above a 2μm transmission line with 680μm spacing between the switches.

A transmission line chamfered only at the contact area of switch with line is proposed in this work. Figure 1 shows the unit cell representation of proposed structure along with the equivalent circuit.

Figure 1(a). Unit cell of the proposed chamfered transmission line.

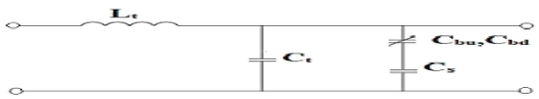

Figure 1(b). Equivalent circuit model.

Tapered impedance section proposed by6 has different impedance section cascaded together to improve the return loss. Though the bandwidth of multi-section impedance matching increases with the number of switches, impedance discontinuity occurs at the end of the taper. Step width discontinuity causes the fringing capacitance at the transition region which cannot be neglected while calculating the loaded line capacitance. The proposed design for phase shifter overcomes this shortcoming with a uniform high impedance line that does not have any discontinuities and causes variations of propagation constant along the length of the transmission line. The proposed design with chamfered corners reduces the discontinuity effects associated with step width junction. The field is concentrated in mitered section and reflection is much reduced. The wider transmission line accounts for reduced ohmic loss. Generally, the capacitance ratio is dependent on the up and down state capacitance of the bridge. In digital phase shifter, the down state capacitance is dominated by a fixed capacitance of MAM

which is independent of shape of the transmission line. The total load capacitance to the transmission line is series combination of bridge capacitance (C_{bu}) and the static capacitance (C_s).

$$C_L = \frac{C_{bu}C_s}{C_{bu}+C_s} \quad \ldots (6)$$

In the upstate, as bridge capacitance is much smaller than static capacitance, the net capacitance seen by the line is approximately C_{bu}. In the downstate position, bridge capacitance increases and C_L is approximately C_s. Independent choice of C_{bu} and Cs endues discrete control of the distributed capacitance till C_{bu}<<C_s in upstate and C_{bd}>>C_s in down state. This condition empowers the performance of phase shifter relatively not controlled by MEMS bridge capacitance ratio7,8. In conventional transmission line, the phase deviation due to the upstate and downstate capacitance is low and more number of switches is required to get the desired phase shift. The proposed chamfered structure reduces the contact area of switch and the transmission line in the upstate producing a low phase shift due to small capacitance. However, the phase deviation between up and down state is large resulting in a higher phase shift per section. This implementation is effective only for digital phase shifter. In case of analog phase shifter, both up and down state capacitances are dependent on area of contact between the switch and transmission line. The gap between the chamfered section of the transmission line and the ground plane on either side is sized to match the wave impedance for smaller line width. The gap varies from 150μm to 125μm where the switch contacts the line.

2.1 Design of Phase Shifter

Design of phase shifter takes the lead from analysis of capacitive MEMS shunt switch. MEMS bridge parameters and their periodic spacing determines the impedance and the propagation velocity of transmission line. The switch is placed on a 65Ω CPW line. The metal bridge of length 300μm, width 60μm, and thickness 2μm is suspended over CPW line at 1.5μm in series with static capacitance Cs provided by 160 x 170μm2 MAM.

Figure 2 shows the schematic model of the complete design. The transmission line distributed capacitance is in parallel with the series combination of MEMS bridge capacitance (Cb) and static capacitance (Cs).

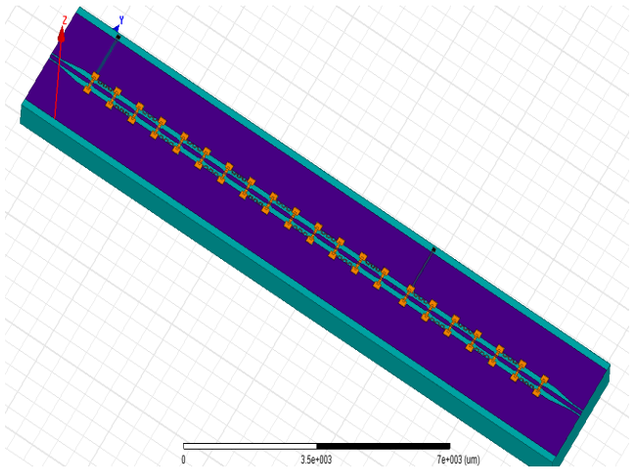

Figure 2. Schematic model of the design with 21 switches.

The 2-bit phase shifter has 21 shunt capacitive switches with an area of 16.18 x 3.2mm^2. On applying analog voltage, the bridge snaps down affecting the distributed capacitive loading on transmission line and variation in the propagation characteristics there by producing a phase shift. The simulated results of switch in their up (0V) and down state (39V) using HFSS are shown in Figure 3 and Figure 4.

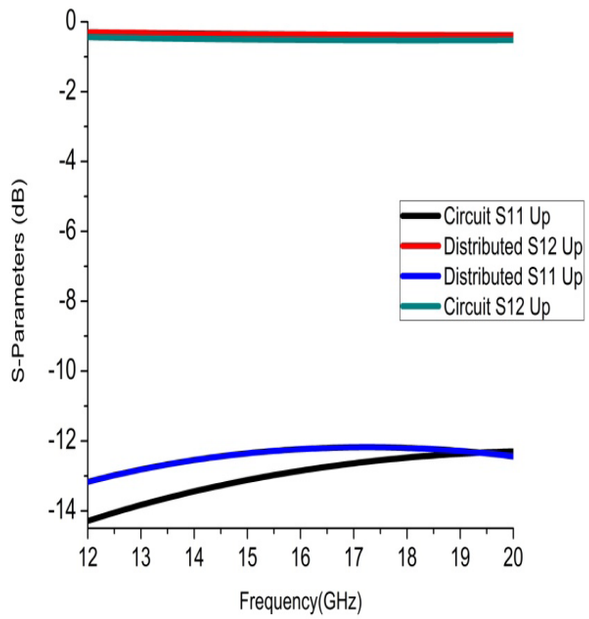

Figure 3. Modeled (circuit) and simulated (distributed) s-parameters of unit cell in up state.

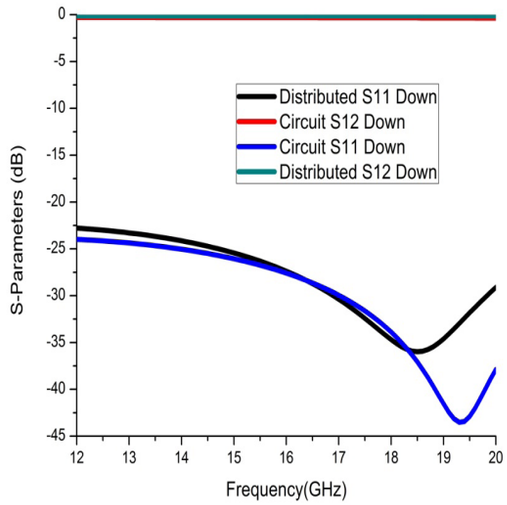

Figure 4. Modeled (circuit) and simulated (distributed) s-parameters of unit cell in down state.

The switch brings about a return loss of -29.64dB and -19.20dB in the upstate and down state respectively while the insertion loss is maintained at -0.01dB and -0.07dB for the respective states mentioned earlier. The phase achieved by a single switch is 11.82° when the edges are beveled to reduce loss. The resulting S-parameters are fitted in the equivalent circuit consisting of series inductor and shunt capacitor with in 50Ω transmission line as in Figure 5 using Advanced Design System (ADS).

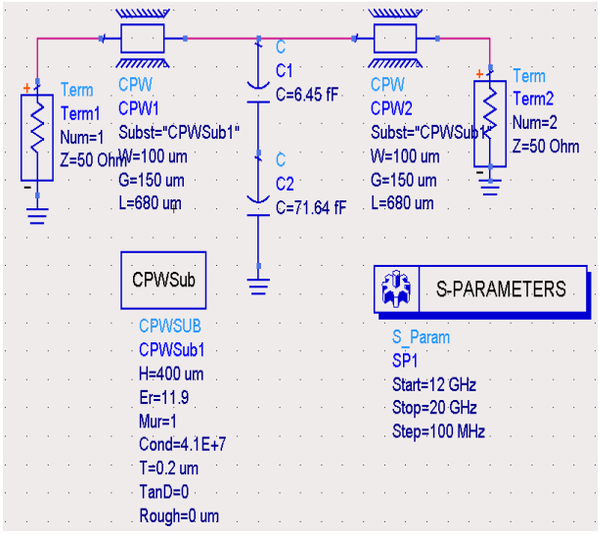

Figure 5. CLR extraction of unit cell using ADS.

The modeled capacitor values of 15.39fFand 123.37fF for up and down states are in good agreement with the simulated values obtained. Table 1 lists the losses for both states of unit section.

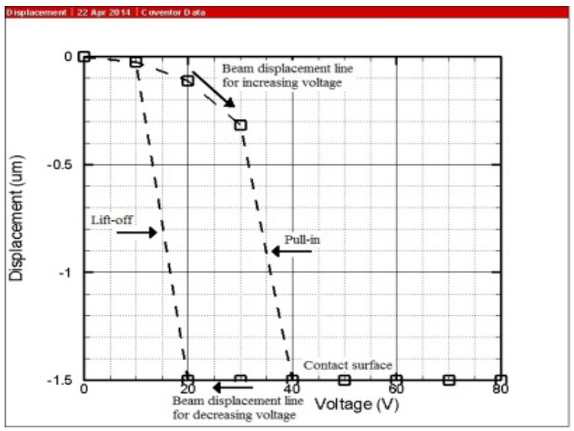

Figure 6. Hysteresis of the bridge on application on DC bias.

Table 1. Comparison of losses using CLR and Simulated model

Model	S-Parameter (dB)				Phase shift (degrees)
	Up state		Down state		
	S_{11}	S_{12}	S_{11}	S_{12}	
Schematic (HFSS)	-12.18	-0.48	-30.37	-0.33	12.8
CLR Extracted (ADS)	-12.63	-0.37	-29.94	-0.24	12.05

The pull down voltage of the bridge on application of electrostatic voltage is given by

$$V_p = \sqrt{\frac{8k}{27\varepsilon_o W w}\, g_o^{\,3}} \qquad \text{.....(7)}$$

The mechanical analysis of the switch involving electrostatic force is performed using coventorware and the result is depicted in Figure 6. The figure shows the effect on the switch by applying a linearly inclined voltage causing downward motion and a release effect due to linearly declined voltage. The snap down of the bridge occurs between 36 and 40V.

The mechanical load is modified due to the redistribution of charges under structural deformation. The pull down voltage is found to be 36.5V.

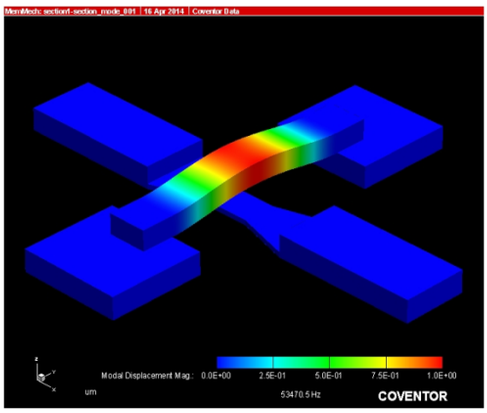

Figure 7(a). Mode 1 (53.4 KHz).

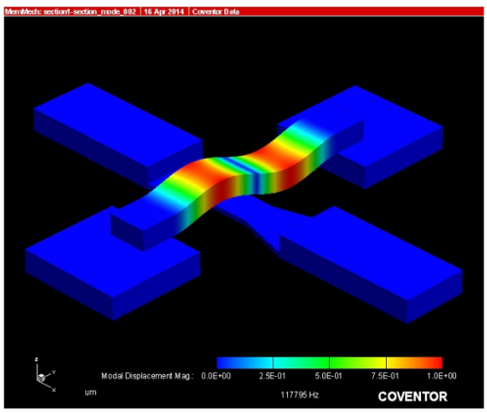

Figure 7(b). Mode 2 (117.79 KHz).

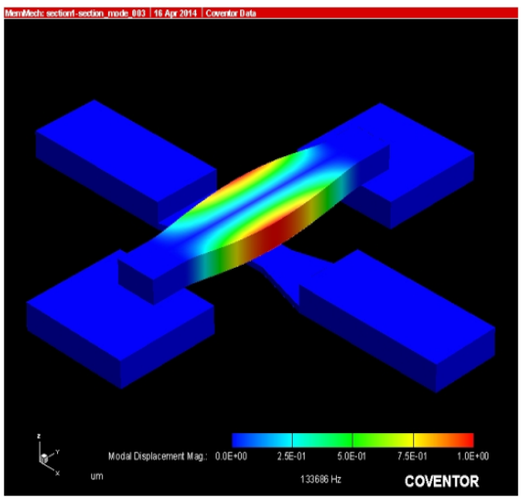

Figure 7(c). Mode 3 (133.68 KHz).

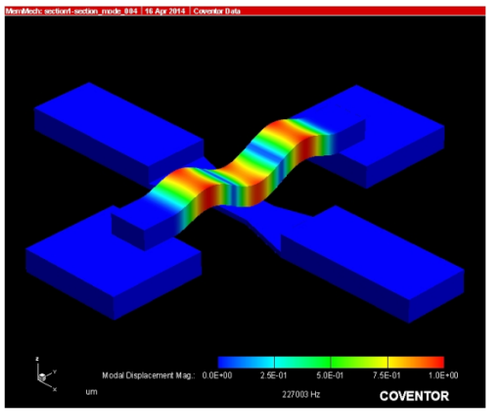

Figure 7(d). Mode 4 (227 KHz).

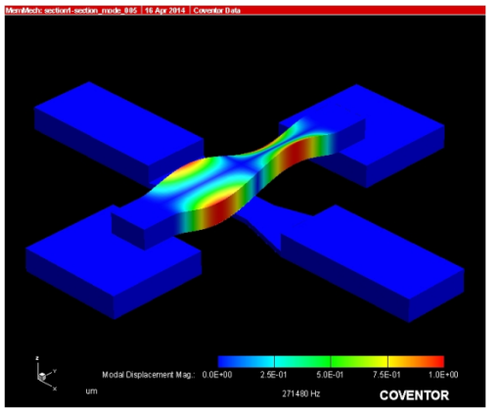

Figure 7(e). Mode 5 (271.48 KHz).

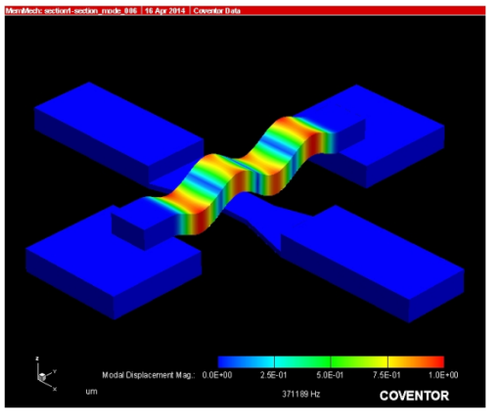

Figure 7(f). Mode 6 (371.18 KHz).

Figure 7. Mode shapes of MEMS switch.

The dynamic property of a mechanical structure under vibrational excitation is determined by the modal analysis of the beam. The Eigen modes of the beam subjected to fundamental and higher order vibrational modes are given in Figure 7.

At the pull in voltage of 35V, the capacitance of the bridge is 37fF. The displacement of 0.86μm at 35V is in close agreement with the theoretically calculated value of 0.6μm. The failure condition of the membrane material is analyzed using the Von Mises stress. The Figure 8 depicts the 'Mises' stress of the membrane to be 39MPa which is well within the yield strength of gold.

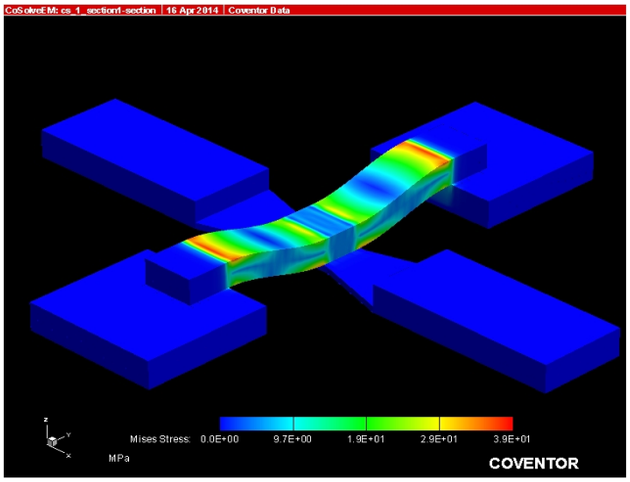

Figure 8. Von Mises stress of MEMS switch.

The simulated capacitance-voltage (C-V) characteristic under the influence of dc voltages is shown in Figure 9. It is observed that around 40V there is a rapid increase of capacitance, a distinctive attribute of the pull-in process while a less sharp decrease in capacitance is noted when the applied voltage is reduced from 40V to 20V, an attribute of the gradual release process.

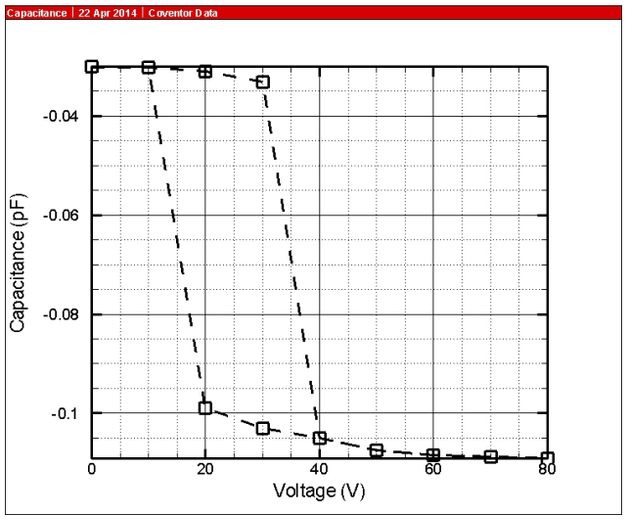

Figure 9. C-V characteristics of MEMS switch.

3. Results and Discussion

A DMTL phase shifter is simulated for 90° using 7, 60μm bridges spaced at 680μm with the total length of 5.4mm. The simulated phase shift and losses are shown in Figure 10 to Figure 15 respectively for up and down states. It is observed that a maximum phase shift of 89.02° is achieved with -0.62dB loss at 17GHz. The Bragg frequency is chosen 2.1times the fo. For a 150/100/150μm line with return loss of -15dB, Zu and Zd are 62 and 42Ω respectively. The theoretical value calculated using equations given by[7,8] of C_{lu} and C_{ld} are 15.39fF and 123.37fF. These values agree well with the simulated values of 14fF and 109.71fF obtained for a single MEMS bridge using HFSS. The disparity in the bridge capacitance between theoretical and simulated values arises out of non-accuracies in the peak reflection coefficient. The phase shift of a single switch is 12.8^0 from the simulation. Juxtaposing the results of the phase shifter simulated for 180^0 using 14 switches with 90^0 section, it is found that the loss increases to -0.87dB with the phase shift of 173.87^0. The loss increases further when the design is simulated along with a bias line. Increase in insertion loss at 32GHz is due to the high upstate capacitance. Smaller upstate capacitance accounts for better return loss as against the higher upstate capacitance. The return loss is maintained between -10dB and -15dB by higher dielectric thickness and as a worst case approaches 0dB at frequencies beyond Bragg frequency.

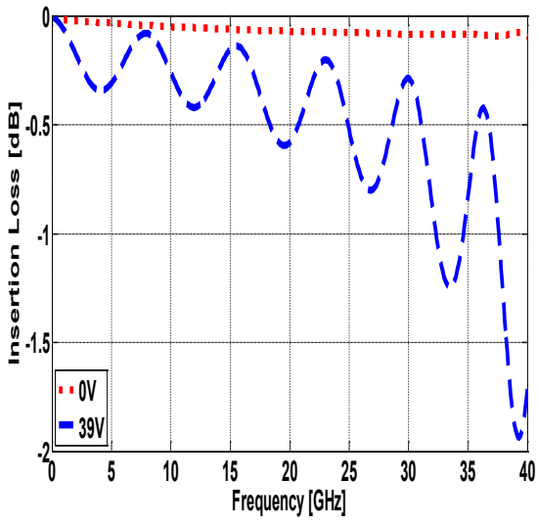

Figure 10. Insertion loss of 7-bridges in up and down state.

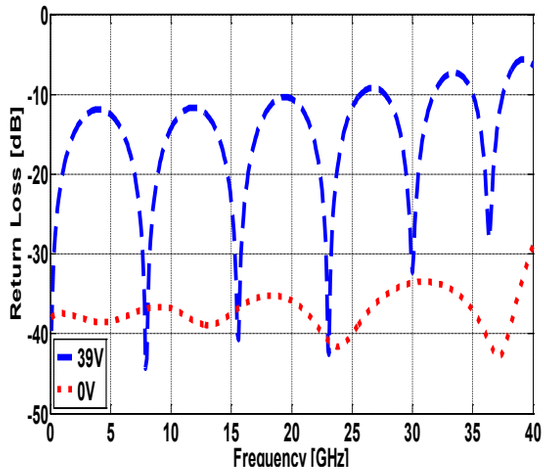

Figure 11. Return loss of 7-bridges in up and down state.

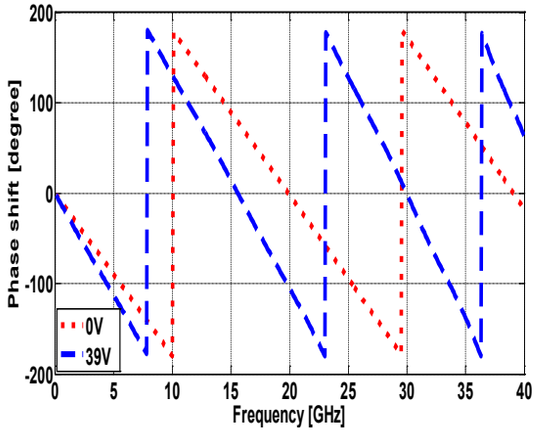

Figure 12. Phase shift of 7-bridges in up and down state.

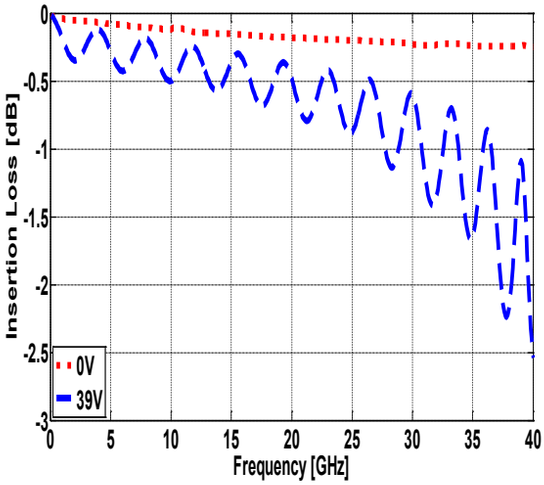

Figure 13. Insertion loss of 14-bridges in up and down state.

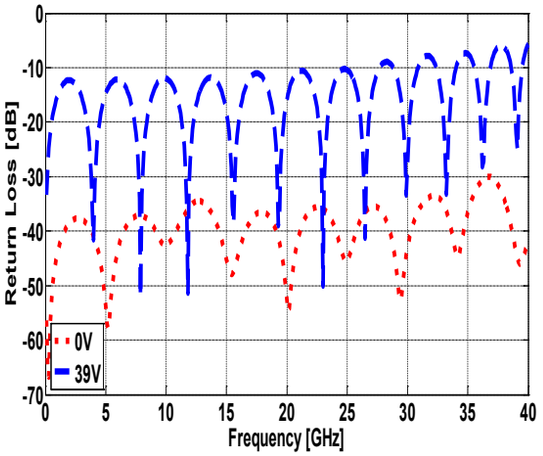

Figure 14. Return loss of 14-bridges in up and down state.

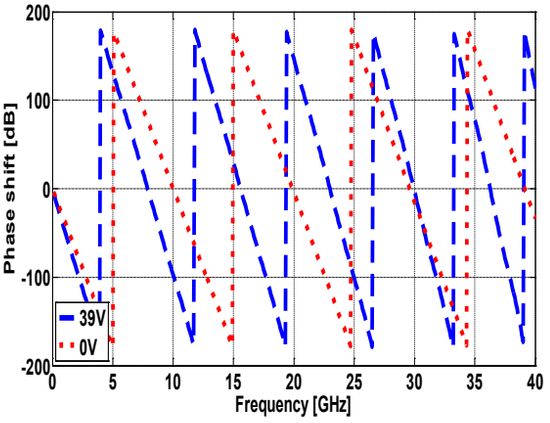

Figure 15. Phase shift of 14-bridges in up and down state.

The switch brings about a return loss of -12.18dB and -30.37dB in the up and down state respectively while the insertion loss is maintained at -0.48 dB and -0.33 dB for the respective states mentioned earlier. The phase achieved by a single switch is 12.8° when the edges are beveled to reduce loss.

4. Conclusion

This paper presents a CPW DMTL phase shifter based on chamfering only in the contact area of the switch with transmission line. The design avoids the step change in tapered section that accounts for lot of fringing field increasing the loss of the signal. The phase shifter obtains a maximum phase shift of 178.87° at 17GHz with -0.87dB loss using 14 shunt capacitive switches with a better phase deviation of 1.13°. Fabrication of the design presented herein is in progress.

Author	Frequency (GHz)	Substrate	Insertion Loss (dB)	Bit	Phase Deviation
Du et al[9].	10	HR Si	1.54	5	3.82°
Afrang and Majis[10]	26.3	Glass	1.6	1	NA
Topalli et al[4].	15	Glass	1.5±0.5	3	2.6°
Lakshminarayanan and Weller[11]	50	Quartz	1.9	4	5.5°
Hung et al[12].	78	Glass	2.7±0.5	3	3°
Hayden et al[8].	14	Quartz	1.2±0.4	2	4°
Hayden et al[8].	37	Quartz	1.5±0.6	2	1.5
Kim et al[13].	65	Quartz	2.8±0.8	4	8.3
Proposed Work	17	Silicon	-0.48 (Unit cell) -0.62 (90° section) -0.87 (180° section)	2	1.13°

5. Acknowledgement

The authors would like to gratefully acknowledge the Center for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore, India for providing the tools required for simulation and evaluation.

6. References

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