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Design and Optimization of Ultra Low Power Low Noise Amplifier using Particle Swarm Optimization

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Abstract

In this paper, an Inductively Degenerated Cascode Low Noise Amplifier (IDCLNA) is designed using TSMC 0.13 μm RF CMOS technology. For improving the performances of LNA, modifications are done in conventional IDCLNA. They are 1. Forward Body Bias (FBB) technique is applied to reduce the supply voltage. 2. The inductor is added between main and cascode transistors for increasing the gain. 3. To reduce the noise factor of cascode stage, an inductor is inserted at the gate of cascode stage. 4. For improving the stability factor, the modified resistive and capacitive shunt feedback is used. The proposed LNA produces 10.7 dB voltage gain, 3.27 dB noise figure, -9.1 dBm IIP3 and 957 μW power consumption. For optimizing the design parameters of proposed LNA, the popular optimization technique like Particle Swarm Optimization (PSO) algorithm is used to improve the performance measures. The optimized LNA achieves 12.6 dB voltage gain, 3.19 dB noise figure and consumes 869 μW power. The optimized results produce the good Figure of Merit (FOM) of 6.6.

Keywords: Figure of Merit, LNA, Power Consumption and PSO

1. Introduction

The rapid development of wireless communication and semiconductor technologies increases the CMOS RF transceiver for Wireless Sensor Network (WSN) applications. WSN consists of group of sensors or nodes which are used to gather information from an environment or control an event[1]. If the nodes are battery operated in a WSN, so their power consumption has to be reduced to ensure that they can provide a longer battery lifetime[2]. The requirement of low power consumption is a major concern for short range communication devices. The IEEE 802.15.4 standard called zigbee supports 2.4GHz ISM band frequency for WSN.

Low Noise Amplifier (LNA) is the first crucial component in RF transceiver. The design of LNA has a tradeoff between the performance measures such as gain, linearity, noise figure and dc power consumption. The Inductively Degenerated Cascode LNA (IDCLNA) is a popular approach for narrowband applications[3,4]. The IDCLNA structure does not support for low voltage and low power applications. Usually, the supply voltage of cascode LNA should be larger than twice of the threshold voltage. Various techniques are incorporated for reducing power consumption[5–7]. An inductively degenerated common source topology was proposed. It operated at 0.5 V supply voltage[8]. This LNA produced the 13 dB gain, 5 dB noise figure, -9 dBm of IIP3 and 2.8 mW power consumption. The common source LNA affects the isolation. Another LNA was proposed using modified current reuse architecture which used the two stage common source topology with modified input matching. It achieved the 14.4 dB gain, 1.6 dB noise figure, IIP3 of –9 dBm and consumed 960 mW power at 0.9 V supply voltage[9]. An ultra low voltage low power LNA was proposed for UWB applications[10]. To attain low power, Forward Body Bias (FBB) technique was applied for reducing the supply voltage. It achieved the noise figure of 2.83-4.7 dB and consumes 4.2 mW power. In this paper, the cascode LNA is proposed with FBB technique and also it is biased in moderate inversion region for supporting low power dissipation and low supply voltage.

For analog/RF design, finding optimized values of LNA is a very difficult task. Optimization algorithms

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are playing a major role in analog design automation methodologies. For optimization, various algorithms are available for LNA optimization. A PSO algorithm was applied to a single discrete transistor for optimizing the performance limitations of the transistor such as minimum noise figure and maximum gain. Using that transistor, an ultra wideband LNA was designed to produce good performances[12]. Theoretical based least square algorithm was incorporated to optimize the output matching network of the 3–5GHz wideband CMOS LNA for minimizing the Noise Figure (NF) and maximizing the gain[12]. The UWB LNA in CMOS 0.25 mm technology was designed and its area, power and performances were optimized using genetic algorithm[13]. In this, Particle Swarm Optimization (PSO) algorithm is applied to optimize the LNA using equation based approach. The remainder of the paper is structured as follows: The design of proposed LNA is discussed in section 2. Section 3 discusses PSO algorithm and also states that specifications, objective function and constraints of the problem. Simulation results are discussed in Section 4. Section 5 dealt with conclusion.

2. CMOS LNA Design

A schematic diagram of proposed LNA and its equivalent two stage circuit is shown in Figure 1(a) and (b). It has IDCLNA structure which consists of cascode structure with input and output matching networks. The cascode structure is treated as CS-CG (Common Source-Common Gate) stages. Usually, the supply voltage of cascode LNA is selected as greater than the twice of the threshold voltage in saturation region. For reducing the supply voltage, Forward Body Bias (FBB) technique is applied to reduce the threshold voltage. The threshold voltage (V_{th}) expression is given as,

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}\right) \quad (1)$$

where V_{th0} is the threshold voltage at zero bulk source voltage, g V_{bs}= 0 γ is the bulk threshold parameter, and φ_f is the bulk Fermi potential. Based on Equation (1), the threshold voltage is reduced by applying positive bulk source potential (i.e.,) $V_{bs} > 0$. The simulated threshold voltage of CS stage MOSFET with L= 0.13 mm and W = 62 mm reduces from 0.43 V to 0.347 V when applying body source voltage of 0.5 V. The supply voltage of proposed LNA is chosen as 0.8 V. The bias or gate source voltage has chosen in transition region between weak and strong inversion regions which is called as moderate inversion region[14]. Both drain and diffusion currents are significant in moderate inversion region and also support for low current consumption.

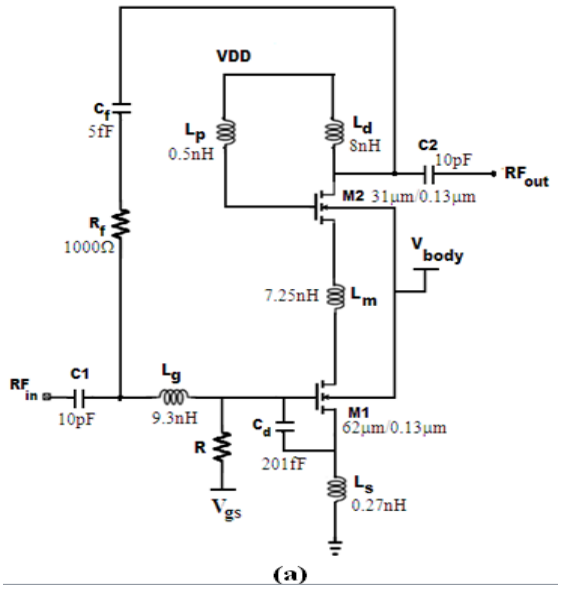

Figure 1. (**a**) Proposed LNA.(**b**) CS-CG Stages of LNA.

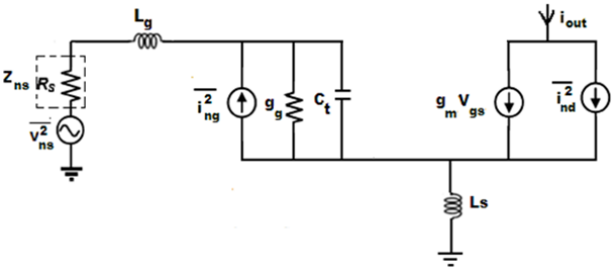

Figure 2. Small signal circuit of input stage.

The small signal equivalent circuit is shown in Figure 2. The input impedance of IDCLNA is written as[4],

$$Z_{in} = \frac{1}{j\omega C_t} + j\omega L_t + \left(\frac{g_{m1}}{C_t}\right) L_s \quad (2)$$

where

$$L_t = L_g + L_s \quad (3)$$

$$C_t = C_{gs} + C_d \quad (4)$$

L_s is the source inductance and L_g is the gate inductance. C_d is the additional capacitance. It is connected in parallel with the gate source capacitance. C_{gs} is the gate source capacitance and is calculated by

$$C_{gs} = \frac{2}{3} W_{opt1} L C_{ox} \quad (5)$$

To find the values of inductors L_s, L_g and the capacitance C_d, the real and imaginary terms in Equation (2) are equated to the input impedance value of 50 Ω. For obtaining the perfect input impedance matching, the values of parameters L_s, L_g and C_d are adjusted. g_{m1} is the transconductance of the main device.

If the output impedance of the CS stage and the input impedance of the CG stage are both capacitive, a series inductor L_m is inserted between CS and CG stages to build a series resonator so as to improve the matching between CS and CG stages. Also, the power transfer between CS and CG stages is increased at resonant frequency of the resonator.

An inductor L_d is inserted at the drain of CG stage for output impedance matching. L_d is placed for two purposes: 1. The inductor L_d is resonated with the total drain capacitance so as to obtain the desired frequency range. 2. It is used to provide high impedance for good voltage gain. The values of L_d and C2 are chosen by trade-off between gain and bandwidth of the circuit.

In accordance with the noise figure, the noise of CG (cascode) stage is smaller than the CS stage. It mostly depends on parasitic capacitances of CG stage. The parasitic capacitance C_{gs2} (gate to source capacitance) which depends on width of the CG stage is more important to produce the noise figure of CG stage. The equivalent circuit of proposed LNA is shown in Figure 1 (b) where C_{gd2} and g_{mb2} (gate to drain capacitance and bulk transconductance of the CG stage) are ignored for simplicity. The total parasitic capacitances are represented by C_p which estimates as,

$$C_p = C_{gs2} + C_{gb2} \quad (6)$$

where C_{gs2} and C_{gb2} are the gate to source capacitance and gate to bulk capacitance of CG stage. C_p affects the gain of CS stage and the noise figure of CG stage. The noise figure of two stage LNA becomes as in Equation (7) when noise contribution of CG stage is considered[15,16],

$$F = F_1 + F_2 = F_1 + 4R_s\gamma_2 g_{d02}\left(\frac{\omega_0^2 C_p}{\omega_T g_{m2}}\right) \quad (7)$$

where F_1 and F_2 are the noise figures of CS stage and CG stage. The equation of F_1 is described as

$$F = \frac{R}{R_s}\left(1 + R\frac{\gamma\omega_0^2 C_t^2}{\alpha^2 g_{d0}}\chi\right) \quad (8)$$

where

$$\chi = \frac{\delta\alpha^2}{5\gamma}\left[1 + Q_s^2\right]\frac{C_{gs}^2}{C_t^2} + 1 - 2|c|\frac{C_{gs}}{C_t}\sqrt{\delta\alpha^2/5\gamma} \quad (9)$$

R_s, γ_2 and g_{d02} are the source resistance, bias dependent factor and zero bias drain conductance of the CG stage.

In Equation (7), C_p increases the noise figure of CG stage. For reducing F_2, an additional inductor L_p is inserted at the gate of CG stage and is in parallel with the capacitance C_p. L_p and C_p are formed as a parallel network. The inductance L_p is used to cancel out the capacitive effect of C_p at the resonant frequency. The resonant frequency of the parallel network is given by

$$\omega_0 = 1/\sqrt{L_p C_p} \quad (10)$$

The inductor L_p effectively reduces the noise figure of CG stage. The modified resistive and capacitive shunt feedback (R_f and C_f) is employed to improve the input impedance matching and stability factor. The value of resistor (R_f) is 1kΩ.

3. Optimization of LNA

Optimization is required for finding an optimum bias point because various bias points are available in moderate inversion region. Also, the optimum width is also very

important for gain, noise figure and power consumption. For optimization of analog/RF circuits, optimization algorithm plays a vital role. PSO algorithm is applied to LNA which are discussed below.

3.1 PSO Algorithm

PSO is a population based optimization technique invented by Eberhart and Kennedy. This algorithm is inspired by social behavior of bird flocking or fish schooling (Kennedy 2001). PSO has better computational efficiency, less memory space, lesser CPU speed and lesser number of parameters. It starts with the number of particles which form a swarm to move around in the search space. Each particle keeps track of its coordinates in the search space to achieve the best solution associated with the two solutions which are personal best (pbest) and global best (gbest). Every particle move toward its pbest and the gbest locations, with a random weighted acceleration at each time step. The flowchart of PSO algorithm is shown in Figure 3.

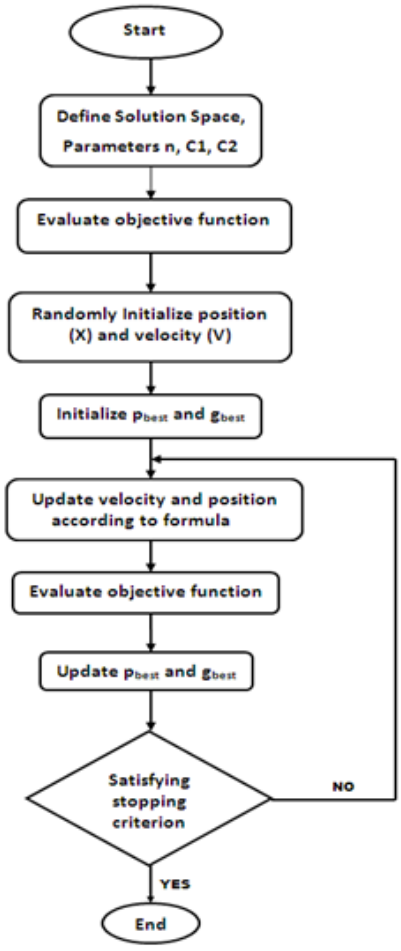

Figure 3. Flowchart of PSO.

PSO initializes with a swarm of particles to move around in the search space. The swarm size (N) and dimensions (D) of the problem are used to represent the search space i.e., N ´D matrix vector. The i^{th} particle of the swarm is represented by a vector, $x_i = [x_{i1}, x_{i2}, ... x_{iD}]$. $x_i = [x_{i1}, x_{i2}, ... x_{iD}]$ A vector $V_i = [v_{i1}, v_{i2}, ... v_{iD}]$ is used to represent the velocity of the i^{th} particle $V_i = [[v]_{i1}, v_{i2}, ... v_{iD}]$ pbest and gbest are the two important parameters which are represented by the vectors $pbest_i = [pbest_{i1}, pbest_{i2}, pbest_D]$ $p_i = [p_{i1}, p_{i2}, ... p_{iD}$ and $gbest = [gbest_1, gbest_2, ... gbest_D]$. Randomly, initializes the particle's position and velocity. The fitness or objective function is calculated for each particle. If the calculated fitness value is better than pbest (best fitness value), the current fitness value is used as the new pbest value. Particle with best fitness value of their neighboring particles is chosen as the gbest value. According to Equations (11) and (12), position and velocity of particle are updated. This procedure continues until the maximum iterations reached.

$$v_{id}^{k+1} = w.v_{id}^{k} + c_1.r_1^{k}.(pbest_{id}^{k} - x_{id}^{k}) + c_2.r_2^{k}.(gbest_{d}^{k} - x_{id}^{k}) \quad (11)$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (12)$$

where d = 1,2,……D and I = 1,2,…..N. $pbest_k^{id}$ pb is the personal best position of given particle. $gbest_k^{id}$ is the global best position of all the particles and w,c_1,c_2 are constants. r_1 and r_2 are random numbers which are uniformly distributed the values between 0 and 1. PSO algorithm is used for optimization of low noise amplifier. LNA is optimized using equation based optimization approach.

3.2 Design Specifications and Objective of PSO Algorithm

The objective function of LNA design is the maximization of FOM (Figure of Merit). It involves three important performance metrics which are gain, noise figure and power consumption. The cost function is defined as

$$CF = \text{maximize FOM} \quad (13)$$

where FOM can be expressed as follows[7,17],

$$FOM = \frac{G}{(NF-1).P_{DC}} \quad (14)$$

where G is the voltage gain in dB, NF is the noise

figure in dB and P_{DC} is the power dissipation in mW. To maximize the objective function, gain should be increased and noise figure and power dissipation should be reduced. The LNA is to be optimized using equation based approach. The equations of the design specifications should be expressed in device parameters as discussed in following subsections.

3.2.1 Voltage Gain

It is the important performance metric of LNA. It is defined as the ratio of LNA output to the input and is expressed in dB. The gain depends on the main transconductance of LNA. The formula for voltage gain is as follows[18],

$$A_V \,?\, Q_{in}\, g_{m1}\, Z_L \tag{15}$$

where Q_{in} is the input matching network quality factor, g_{m1} is the transconductance of main transistor, Z_L is the load impedance. Q_{in} is expressed as,

$$Q_{in} = \frac{1}{2\omega_0 R_s C_t} \tag{16}$$

ω_0 is the resonant frequency, R_s is the source resistance and C_t is the total capacitance which is expressed as,

$$C_t = C_{gs} + C_d \tag{17}$$

where

$$C_{gs} = \frac{2}{3} C_{ox} W_1 L \tag{18}$$

C_{ox} is the oxide capacitance, W_1 and L are the width and length of main transistor. The transconductance of main transistor is explained as,

$$g_{m1} = \frac{\left(e_{ff} C_{ox} W V_{od} \alpha\right)}{L} \tag{19}$$

and the effective mobility is expressed as,

$$e_{ff} = \frac{2V_{sat}}{E_{sat}} \tag{20}$$

V_{sat} is the saturation velocity, E_{sat} is the velocity saturation field strength, W and L are the width and length of the main transistor and the parameter α is expressed in terms of overdrive voltage as in Equations (19) and (20),

$$\alpha = \frac{1 + 1/2\rho}{(1+\rho)^2} \tag{21}$$

$$\text{and } \rho = \frac{V_{od}}{LE_{sat}} \tag{22}$$

3.2.2 Noise Figure

Noise figure is another important measure. It is defined as the ratio of the Signal to Noise Ratio (SNR) at the input to the signal to noise ratio at the output. The noise factor is calculated using transistor's small signal parameters as follows[9],

$$F = \frac{R}{R_s}\left(1 + R\frac{\gamma\omega_0^2 C_t^2}{\alpha^2 g_{d0}}\chi\right) \tag{23}$$

$$\chi = \frac{\delta\alpha^2}{5\gamma}\left[1 + Q_{in}^2\right]\frac{C_{gs}^2}{C_t^2} + 1 - 2|c|\frac{C_{gs}}{C_t}\sqrt{\delta\alpha^2/5\gamma} \tag{24}$$

Where g_{d0} is the zero bias drain conductance of the transistor and is expressed as,

$$g_{d0} = eff\ C_{ox}\frac{W}{L}V_{od} \tag{25}$$

where $R = R_s + R_g$. R_s and R_g are the source resistance and gate resistance respectively. γ, δ and α are the bias dependent parameters. c is the correlation coefficient between gate and drain noise currents. It is defined as,

$$c = \frac{\overline{i_{ng} * i_{nd}}}{\sqrt{i_{ng}^2 i_{nd}^2}} \tag{26}$$

where i_{ng} and i_{nd} represent the gate noise current and drain noise current.

3.2.3 Power Consumption

It is very important factor of LNA. It is simply a DC current multiplied by a supply voltage. In saturation region, the current expression of the short channel transistor is given as[9,19],

$$I_d = WC_{ox}V_{sat}\frac{V_{od}^2}{V_{od}^2 + LE_{sat}} \tag{27}$$

V_{od} is the effective or overdrive voltage and can be written as,

$$V_{od} = V_{gs} - V_{th} \quad (28)$$

The overdrive voltage ranges depend on moderate inversion region. The power consumption is calculated as,

$$P_{DC} = I_d \times V_{DD} \quad (29)$$

where W and L are the width and length of the transistor, E_{sat} is the velocity saturation field strength, and v_{sat} is the saturation velocity and V_{od} is the overdrive voltage.

3.2.4 Input Parameters and Constraints for PSO

PSO algorithm is implemented using Matlab. Initial population matrix size of PSO is 70 × 3 where row number of 70 represents the number of particles in the population and column number 3 indicates the dimension of particle vector which is represented as {A_v, NF, P_{DC}} where A_v is the voltage gain, NF is the noise figure and P_{DC} is the DC power consumption. Iterations are given as 200. The value of constants c1 and c2 are chosen as 2 and inertia weight w is selected as 0.9.

The constraints for design parameters are

$$L_{min} \le L_i \le L_{max} \quad (30)$$

$$W_{min} \le W_i \le W_{max} \quad (31)$$

$$V_{odmin} \le V_{odi} \le V_{odmax} \quad (32)$$

The range of L is set to be relatively small, which is close to the minimum feature size of the targeted CMOS technology. The range of W is set to be from 10 µm to 100 µm, which is adequate for channel width requirement. V_{gs} is set to be in moderate inversion region so that the range of overdrive voltage V_{od} from 10 mV to 400 mV. The effective gate length of 0.13 mm is selected. The LNA Small signal parameters involved in the objective problem are as follows: γ = 1.2; c = 0.2; R_s = 50 W; δ = 2; ω_o = $1.5'10^{10}$; C_{ox} = $13.2'10^{-3}$F/m^2; T_{oxn} = 2.81nm; E_{sat} = $4.5'10^6$ V/m; v_{sat} = $11.7'10^4$ m/s. The target value of the objective function is aimed to be greater than 5. The fitness or cost function can be written as,

$$CF = -abs\ (FOM - F_{desired}) \quad (33)$$

where abs denotes the absolute value. $F_{desired}$ is the desired value which is 7. When the condition is satisfied, the fitness function has zero value. In other cases, negative fitness value is obtained. To maximize the fitness function, the optimal solution is achieved. According to the PSO algorithm, the optimized values of design parameters are obtained which are given in Table 1.

Table 1. Optimized design parameters of LNA

Design Parameters	LNA without Optimization	PSO
W1 (mm)	62	86
W2 (mm)	31	89
V_{od} (mV)	53	23
V_{gs} (mV)	400	370

The other design parameters of LNA for input and output matching networks are L_g=10 nH; L_s=0.25 nH; C_d=318 fF; L_m=6.7 nH; L_d=9 nH; L_p=0.5 nH; R_f=1 KΩ ; C_f=5 fF.

4. Simulation Results

The designed LNA is simulated using Advanced Design System (ADS). The low noise amplifier is redesigned with resulting PSO design parameters in ADS simulator to validate that PSO based LNA design is satisfying desired specifications. The overall performance merit FOM is maximized from 4.92 to 6.6. The LNA with and without PSO is shown in Figure 4 which produces 10.7 dB voltage gain for the proposed LNA and 12.6 dB gain for the proposed LNA with PSO.

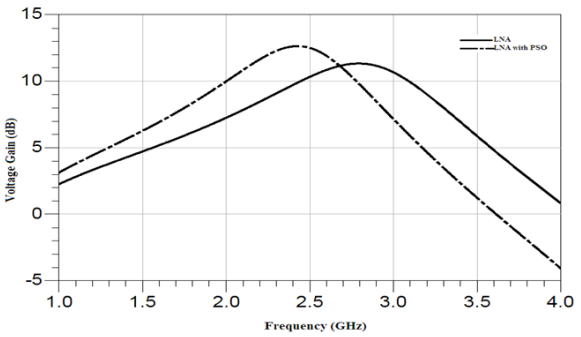

Figure 4. Voltage gain.

The noise figure of LNA with and without PSO is shown in Figure 5. The proposed LNA with and without PSO achieve 3.27 dB noise figure and 3.20 dB.

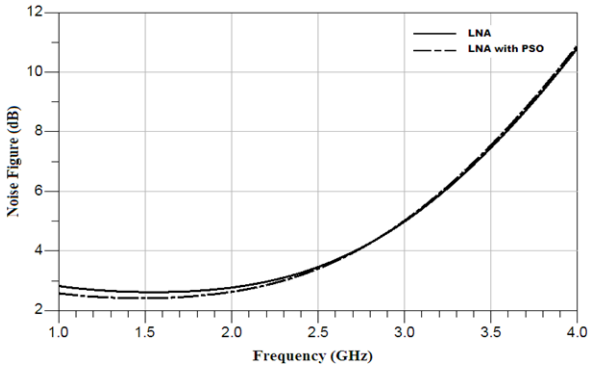

Figure 5. Noise figure.

For two tone test, two frequency signals of 10 MHz spacing with equal power levels are applied to the proposed LNA with and without PSO. The input third order intercept point (IIP3) of -9.1 dBm and -11.1 dBm are achieved for proposed LNA with and without PSO as shown in Figure 6.

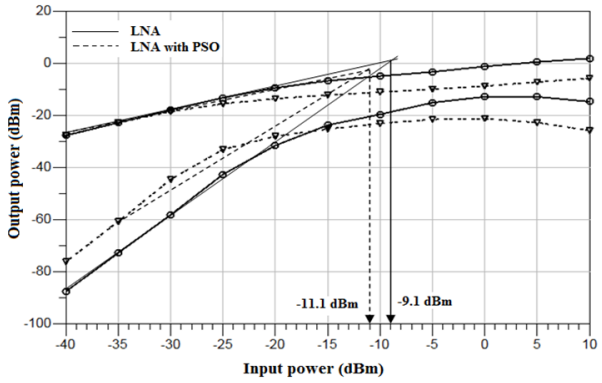

Figure 6. Third order intercept point.

The modified resistive capacitive shunt feedback effectively improves the stability factor of proposed LNA. For unconditional stability, the necessary and sufficient conditions are[20],

$$|\Delta| < 1 \tag{34}$$

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/2|S_{12}S_{21}| > 1 \tag{35}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ (36)

Figure 7 shows that Rollet's stability factor K and Δ which are satisfied their conditions for proposed LNA with and without PSO. The values of K and Δ are 6.84 and 0.286 for proposed LNA. The optimized LNA produces 6.632 and 0.477 for K and Δ.

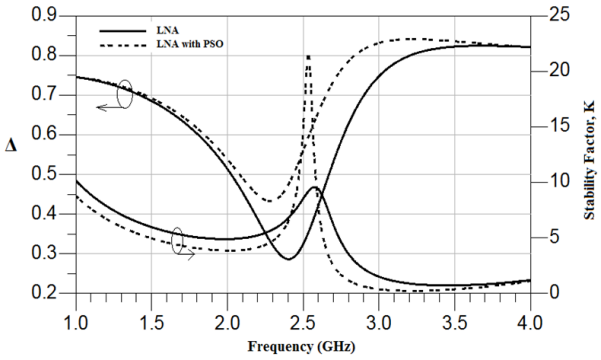

Figure 7. Stability factor and Δ.

The proposed LNA and the optimized LNA satisfy the stability conditions. The voltage gain and the noise figure values have improved for the proposed LNA with PSO. The IIP3 value has decreased for LNA with PSO than LNA without PSO. The proposed LNA consumes 957 μW power. The optimized LNA consumes 1.087 mA current at 0.8 V supply voltage. The performance comparison of LNA with and without optimization is shown in Table 2.

Table 2. Performance comparison of LNA

Specifications	LNA without Optimization	LNA with PSO (ADS Simulator)
Power Consumption (mW)	957	869
Voltage Gain (dB)	10.7	12.6
Noise Figure (dB)	3.27	3.20
FOM	4.92	6.6

LNA with equation-based PSO optimization has achieved the low power consumption of 869 mW, voltage gain of 12.6 dB, noise figure of 3.20 dB. PSO algorithm is an efficient algorithm for optimization of LNA circuit.

5. Conclusion

A 2.4 GHz ultra low power CMOS LNA has been designed in TSMC 130 nm CMOS process at 0.8 V supply voltage.

Some modifications have been successfully applied for improving the performances in the proposed LNA. The proposed LNA has achieved the 10.7 dB voltage gain, 3.27 dB noise figure, -9.1 dBm IIP3 and 957 μW power consumption. PSO algorithm has been successfully applied for increasing the FOM by optimizing the design parameters of proposed LNA. The optimized LNA has produced 12.6 dB gain, 3.20 dB noise figure, -11.1 dBm IIP3 and consumes 869 mW power from the supply voltage of 0.8V. The designed LNA is more suitable for low power applications.

6. References

1. Hafez AA, Dessouky MA, Ragai HF. Design of a low-power ZigBee receiver front-end for wireless sensors. Microelectronics Journal. 2009; 40:1561–8.
2. Kim YJ, Hwang IC, Baek D. A switchless Zigbee frontend transceiver with matching component sharing of LNA and PA. IEEE Microwave and Wireless Components Letters. 2010; 20:516–8.
3. Shaeffer DK, Lee TH. A 1.5-V, 1.5-GHz CMOS low noise amplifier. IEEE Journal of Solid-State Circuits. 1997; 32:745–59.
4. Andreani P, Sjoland H. Noise optimization of an inductively degenerated CMOS low noise amplifier. IEEE Transactions on Circuits And Systems-II: Analog and Digital Signal Processing. 2001; 48:835–41.
5. Wang YS, Lu LH. 5.7 GHz low-power variable-gain LNA in 0.18 um CMOS. Electronics Letters. 2005; 41:66–8.
6. Toofan S, Rahmati AR, Abrishamifar A, Lahiji GR. Low power and high gain current reuse LNA with modified input matching and inter-stage inductors. Microelectronics Journal. 2008; 39:1534–7.
7. Chang C-P, Chen J-H, Wang Y-H. A fully integrated 5 GHz low-voltage LNA using forward body bias technology. IEEE Microwave and Wireless Components Letters. 2009; 19:176–8.
8. Ho D, Mirabbasi S. Low-voltage low-power low-noise amplifier for wireless sensor networks. Electrical and Computer Engineering Conference; Ottawa, Ont. 2006. p. 1494–7.
9. Liu B, Wang C, Ma M, Guo S. An ultra-low-voltage and ultra-low-power 2.4 GHz LNA design. Radioengineering. 2009; 18:527–31.
10. Chang C-S, Guo J-C. Ultra-low voltage and low power UWB CMOS LNA using forward body biases. IEEE Radio Frequency Integrated Circuits Symposium; Seattle, WA. 2013 Jun 2-4. p. 173-6.
11. Demirel S, Gunes F, Ozkaya U. Design of an ultra-wideband low-noise amplifier using a single transistor: A typical application example. Progress in Electromagnetics Research B. 2009; 16:371–87.
12. Dorafshan A, Soleimani M. High-gain CMOS low noise amplifier for ultra wide-band wireless receiver. Progress in Electromagnetics Research C. 2009; 7:183–91.
13. Khalaf LD. Area and power optimization of 802.15.4a UWB pulse low noise amplifiers by genetic algorithms. Progress in Electromagnetics Research C. 2012; 28:155–64.
14. Binkley D. Tradeoffs and optimization in analog CMOS design. USA: John Wiley and Sons Ltd; 2008.
15. Samavati H, Rategh HR, Lee TH. A 5-GHz CMOS wireless LAN receiver front end. IEEE Journal of Solid-State Circuits. 2009; 35:765–72.
16. Fan X, Zhang H, Sanchez-Sinencio E. A noise reduction and linearity improvement technique for a differential cascode LNA. IEEE Journal of Solid-State Circuits. 2008; 43:588–99.
17. Song I, Jeon J, Jhon HS, Kim J, Park BG, Lee JD, Shin H. A simple figure of merit of RF MOSFET for low-noise amplifier design. IEEE Electron Device Letters. 2008; 29:1380–2.
18. Toofan S, Rahmati AR, Abrishamifar A, Lahiji GR. A low-power and high-gain fully integrated CMOS LNA. Microelectronics Journal. 2007; 38:1150–5.
19. Lee TH. The design of CMOS radio-frequency integrated circuits. UK: Cambridge University Press; 1998.
20. Gonzalez G. Microwave transistor amplifiers: Analysis and design. Upper Saddle River, NJ: Prentice-Hall; 1997.