

Design of Novel Low Power Dual Edge Triggered Flipflop

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Abstract

Low power designs are gaining more importance in the recent VLSI Era. Electronics Design Automation (EDA) tools play a vital role in low power system implementation. High speed Computing and processing applications also requires low power designs to enhance their performance. Flip-flops are the basic memory and timing elements in digital circuits. To improve the performance of digital circuits new methods have to be devised for the implementation of low power and energy efficient flipflops. This in turn will help to improve the speed and performance of the system. This paper aims in the design of novel low power flip-flop which is an important element to determine the performance of the synchronous circuit in the area of low power VLSI.

Keywords:

1. Introduction

This paper mainly focuses in the reduction of power dissipation, reducing sensing delay and to increase the circuit robustness of dual edge triggered flip-flops and latches and also to analyze the technique of dual edge triggered circuits¹.

1.1. Low Power Design

The design of portable devices requires consideration for peak power consumption to ensure reliability and proper operation. The time averaged power is often more critical as it is linearly related to the battery life. Power due to switching activity, Power due to leakage and short circuit power constitutes the major cause for Power dissipation².

Pswitching is the switching power⁴. Generally in the CMOS circuit design this power component usually dominant and may account for more than 90% of the total power. α denotes the transition activity factor, which takes into account the average number of power consuming, transition that is made at a node in one clock period. V_s are the voltage swing, where in most cases it's the same as the supply voltage, V_{dd} . C_L is the node capacitance. It can be broken into three components, the gate capacitance, the diffusion capacitance and the interconnect capacitance.

The interconnect capacitance is in general function of the placement and routing.

2. Dual Edge Designs

2.1. Static Output Controlled Discharged Flipflops

Static output Controlled Discharged Flip-Flops (SCDFF) involve an explicit pulse generated and a latch that captures the pulse signal show the schematic of pulse generation³.

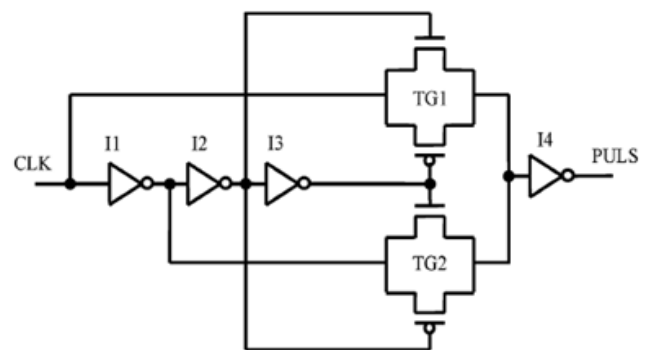


Figure 1. Dual Pulse Generation for Static output controlled discharged flip-flops..

The latch structure of SCDFF consist of two static

stages. In the first stage, input D is used to drive the precharged transistors so the node X follows D during the sampling period. In addition, the conditional discharging technique is implemented by inserting a QB-controlled nMOS the discharge path, which prevents unnecessary discharging at node X as long as the input⁵

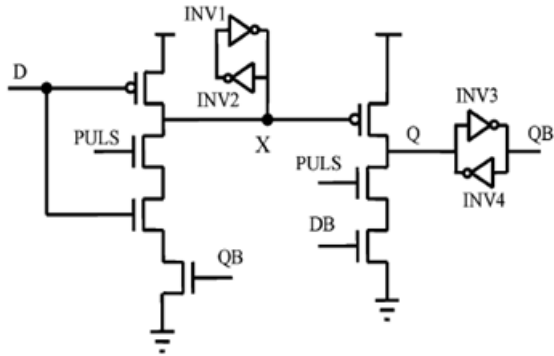


Figure 2. Latch for Static output controlled discharged flip-flop.

The major advantage of SCDF is low power consumption and soft edge property. However the delay is always presented between Q and QB due to the single-ended nature of SCDF⁶

2.2 Simulation Results for SCDF

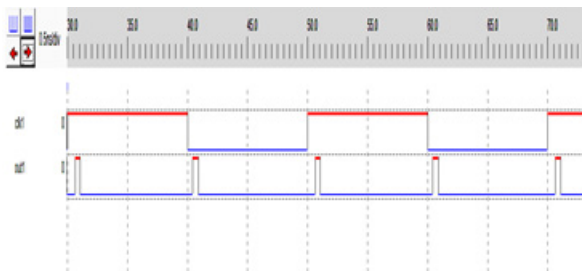


Figure 2(a). Waveform for Dual Pulse Generator.

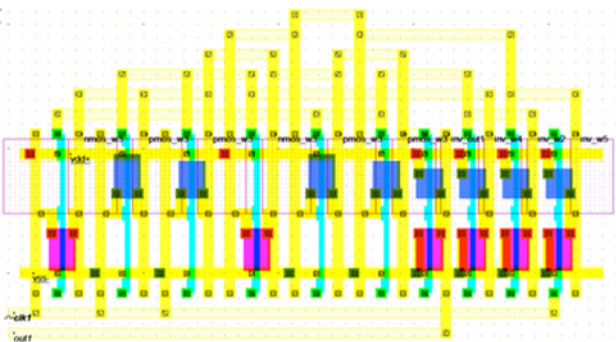


Figure 2(b). Layout of Dual Pulse Generation using microwind..

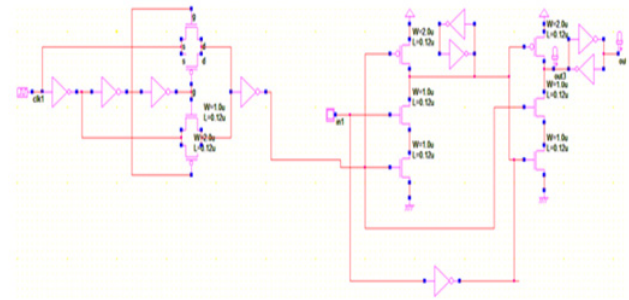


Figure 2(c). Static output controlled discharged flip-flops using DSCH

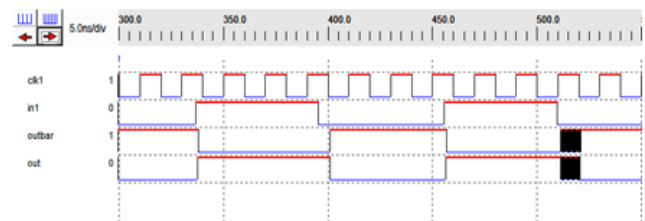


Figure 2(d). waveform for Static output controlled discharged flip-flops

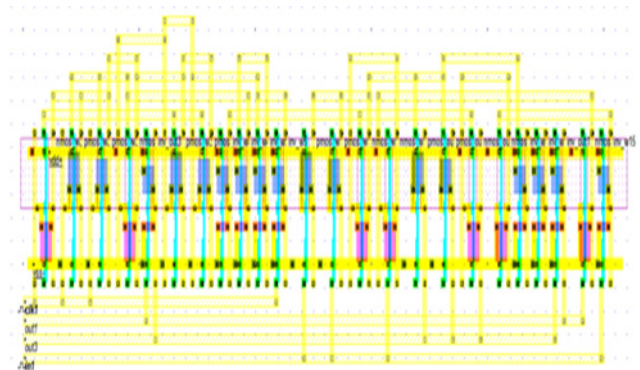


Figure 2(e). Layout of Static output controlled discharged flip-flops.

3. Dual Edge Triggered Static-Pulsed Flip-Flop

The schematic diagram of dual-edge triggered static pulsed flip-flop (DSPFF) is shown⁷.

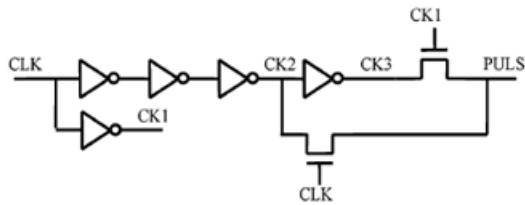


Figure 3(a). Pulse generator for Dual Edge triggered static pulsed flip-flop.

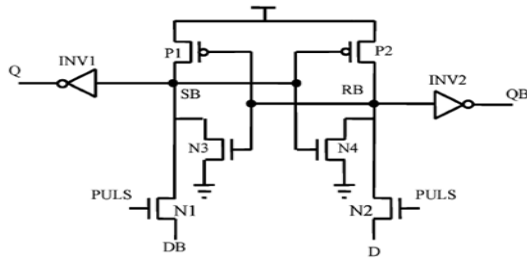


Figure 3(b). Static Latch for Dual Edge triggered static pulsed flip-flop.

3.1 Simulation Results for DSPFF

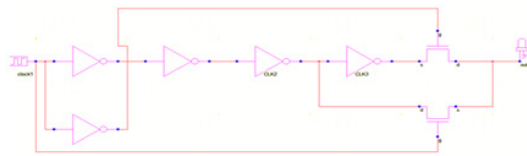


Figure 3(c). Dual Edge Triggered Static Pulse Generator using Dsch.

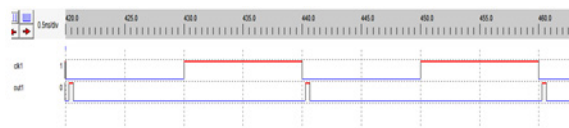


Figure 3(d). Wave Form of Dual Edge Triggered Static Pulse Generator.

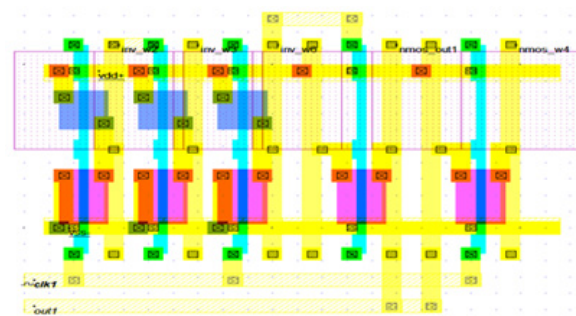


Figure 3(e). Layout of Dual Edge Triggered Static Pulse Generator using Microwind.

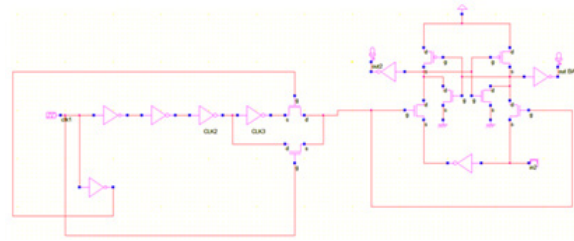


Figure 3(f). Dual-Edge Triggered Static Pulsed Flip-Flop Using DSCH.

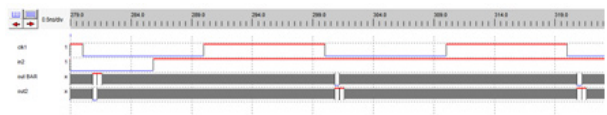


Figure 3(g). Waveform for dual-edge triggered static pulsed flip-flop.

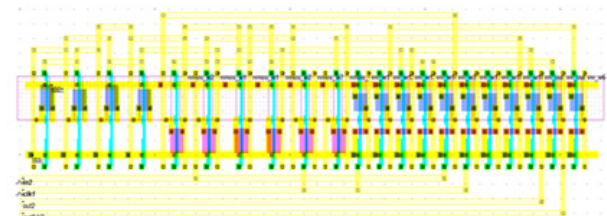


Figure 3(h). Waveform for dual-edge triggered static pulsed flip-flop.

4. Adaptive Clocking Edge Sense Amplifier Flip-Flops

Adaptive clocking dual edge sense amplifier flip-flops consist of three stages:⁸ the adaptive clock inverting stage, the front-end sensing stage and the Nikolic's latch stage.

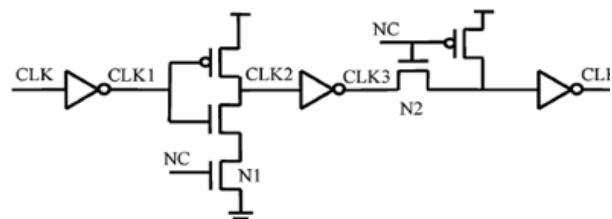


Figure 4(a). Adaptive Clocking Inverter Chain.

The adaptive clocking inverter chain is designed to disable some transistors in the chain when the data switching activity is low. The node NC in the sensing stage

is design to generate adaptive clocking. When the output input same, NC will become to be low voltage and turn off the NMOS transistors N1 and N2, the adaptive clocking inverter chain will generate a pulse.

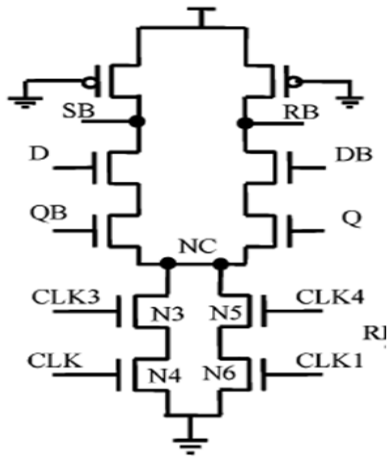


Figure 4(b). TSensing Stage

When the output of the flip-flop and input data are different, it will become to be high voltage and turn on the NMOS transistor N1 and N2, and then a pulse will be generated. Therefore, the adaptive clocking inverter chain will generate the pulse or will not generate the pulse according to the input and output of the flip-flop. During the transparent period of the adapting clock edge sense-amplifier flip-flop, either SB or RB will be discharged due to the input data. Then the output of the flip-flop will be changed in the latching stage.

This disadvantage of the adaptive clocking dual-edge sense-amplifier flip-flop⁹⁻¹³. As seen in the schematic, the adaptive clocking dual edge sense-amplifier flip-flop requires more transistor to realize the adaptive clocking, and the circuit is very complex, so the speed of the flip-flop will be slower; moreover, if the switching activity of the circuit is very high, the adaptive clocking dual-edge sense-amplifier flip-flop will consume a lot of power due to the more used transistors in the circuit.

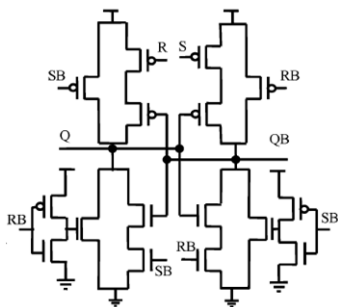


Figure 4(c). Nikolic Latch.

4.1.1 Simulation Results

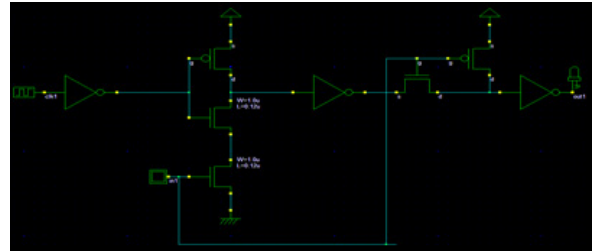


Figure 4(d). Adaptive Clocking Inverter Chain using DSCH.

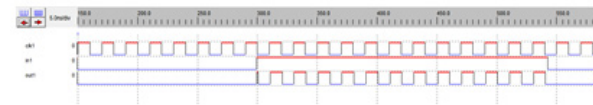


Figure 4(e). Waveform for Adaptive Clocking Inverter Chain.

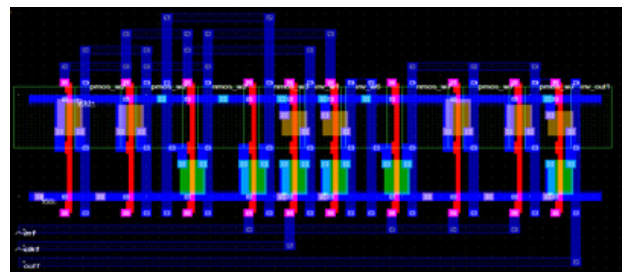


Figure 4(f). Layout of Adaptive Clocking Inverter Chain using microwind.

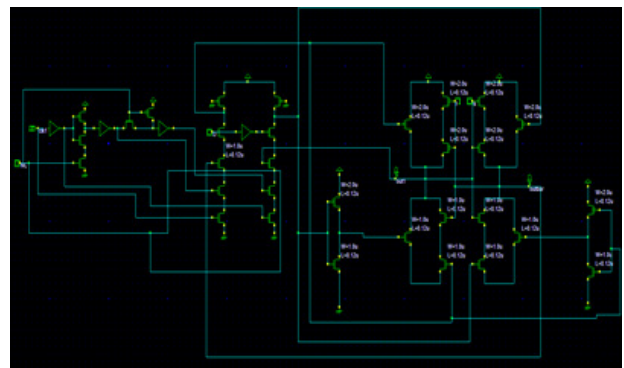


Figure 4(g). Adaptive clocking edge sense amplifier flip-flops using DSCH.

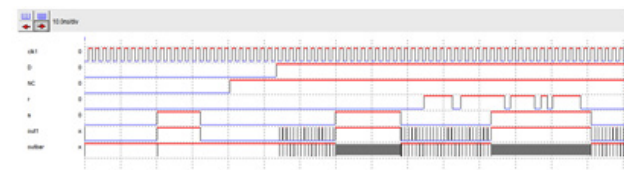


Figure 4(h). Wave form for adaptive clocking edge sense amplifier flip-flop

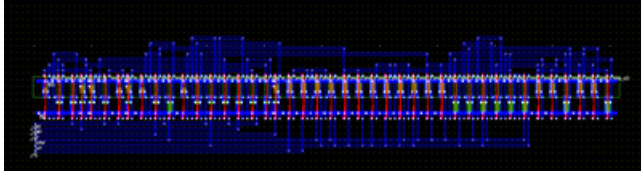


Figure 4(i). adaptive clocking edge sense amplifier flip-flop.

5. Power Dissipation Parameter Analysis of Dual Edge Designs

5.1 Power Dissipation Comparison for Dual Edge Pulse Generators

Table 1. Power dissipation for various capacitances

Capacitance In ff	Dual Edge Pulse Generator Design Power Dissipation in mw		
	SCDFF	DESFF	ACSAFF
0	0.020	0.007	0.014
10	0.031	0.007	0.020
20	0.033	0.007	0.025
20	0.033	0.007	0.031
40	0.033	0.007	0.037
50	0.033	0.007	0.043
60	0.033	0.007	0.048
70	0.033	0.007	0.054
80	0.033	0.007	0.060
90	0.033	0.007	0.066
100	0.033	0.007	0.071

5.2 Delay Comparison for Various Dual Edge Pulse Generators

Table 2. Path output delay comparison

Dual Edge Designs	Delay in ns
SCDFF	0.410
DESFF	0.640
ACSAFF	0.710

5.3 Power Dissipation Comparison for Dual Edge Triggered Flipflops

Table 3. Power dissipation comparison for dual edge triggered flipflops

Capacitance In ff	Dual Edge Designs Power Dissipation in mw		
	SCDFF	DESFF	ACSAFF
0	0.390	0.020	0.167
10	0.384	0.023	0.178
20	0.384	0.026	0.174
20	0.384	0.029	0.165
40	0.384	0.034	0.133
50	0.384	0.037	0.118
60	0.384	0.040	0.115
70	0.384	0.043	0.114
80	0.384	0.049	0.114
90	0.384	0.049	0.114
100	0.384	0.049	0.114

5.4 Power Dissipation for Various VDD (Pulse Generators)

Table 4. power dissipation for various supply voltage

Supply Voltage (VDD) in Volts	Dual Edge Pulse Generators		
	SCDFF	DECFF	ACSAFF
0	0	0	0
0.2	0	0	0
0.4	0.001	0.001	0.002
0.6	0.010	0.003	0.006
0.8	0.013	0.004	0.008
1.0	0.017	0.005	0.011
1.2	0.020	0.007	0.014

5.5 Power Dissipation for Various VDD (Dual Edge Designs)

Table 5. Power dissipation for various VDD (dual edge designs)

Supply Voltage (VDD) in Volts	Dual Edge Designs		
	SCDFF	DECFF	ACSAFF
0	0	0	0
0.2	0	0	0
0.4	0.003	0.003	0.005
0.6	0.038	0.009	0.014
0.8	0.155	0.012	0.061
1.0	0.255	0.016	0.116
1.2	0.390	0.020	0.161

6. Conclusion

Various dual edge designs for flip-flops have been analysed¹⁴. In this Dual Edge Triggered Static Flip Flop (DSPFF) consumes less power when compare to Static Output Controlled Discharge Flip-Flop (SCDFF), Adaptive Clocking Edge Sense Amplifier Flip-Flop (ACSAFF). And it is simple and suitable for dual edge triggering and also used to eliminate unnecessary transition¹⁸.

In Static Output Controlled Discharge Flip-Flop (SCDFF) a delay is always present at Q and QB due to the single ended nature. And also there is a short circuit current. In ACSAFF exponentially power dissipated when the increase in capacitance due to the more number of transistors used in circuit¹⁵.

Future work lies in reducing the clock frequency half of the single edge flip-flop while maintaining the same data throughput and also better performance in terms of both power dissipation and speed. And also able to achieve low power consumption that has small delay^{16,17}.

7. References

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