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# Design of Power Aware on Chip Embedded Memory based FSMEncoding in FPGA

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## Abstract

A new design methodology to reduce power consumption and minimization of area in FSM based system is fore fronted into FPGA using Finite State Machines (FSMs) mapping in this proposed work. This FSM is mapped into the On Chip Embedded Memory (OCEM) through clock gating technique. FSM encoding is stored using OCEM as it reduces the Flip-Flop (FF) and combinational function usage. Clock gating technique will reduce the power consumption additionally through blocking the clock while OCEMP is inidle state. The proposed design is tested and analyzed using ALTERA cyclone II FPGA for Arithmetic Logic Units(ALU), Advanced Encryption Standard core (AES), SRAM controller and Synchronous FIFO. OCEM based implementation of One- Hot encoding is performed and compared with conventional Flip-Flop based One-hot encoding and analyzed.The FSM implemented using proposed method consumes less power and fewer areas when compared with FF based FSM implementation or using binary encoding technique. The OCEM based implementation can be clocked to maximum clock frequency. Experimental results and analyses shows that OCEMbased FSM consumes 4 to 26 % less power than FF based techniques.

**Keywords:** Gated Clock, Low Power Design, Synchronous Counter

## 1. Introduction

Power reduction and area optimization of Field Programmable Gate Arrays (FPGAs) is a significant area of research in this era. Any digital circuits can be implemented using FPGA as it is a semiconductor Integrated Circuit (IC). FPGA has several advantages when compared with Application Specific Integrated Circuits (ASICs) or full custom devices though they are power consuming1. FPGAs take less time design, Non-recurring expenses reprogramability, reusability and synthesis is easier compared to ASIC. FPGAs are extremely desirable for implementing digital designs because of its properties such as flexibility, programmability and due to these properties they are more suitable for prototyping, debugging, etc1. Power consumption of FPGA is 60% more than ASIC as 60% consumed by interconnects between logical blocks, 16% by logic blocks and 14% by clock distributing network2. Clock distribution is different from ASIC based design3, as major power consumption is due to clocking circuits. Logic block interconnect are power dominating as the transmitted signal should be routed through many switches before reaching its destination block. Power consumption takes place due to the implemented logics and clocking circuit. FPGAs are power dominated design architecture, but power reduction techniques to lower power consumption in FPGAs are new area of research1,2. This power reduction technique are used to utilize the advantages of FPGA as they are used as co processor for implementing and executing complex and parallel task including high end servers, defense applications, video processing with high resolution, network control, portable device etc.

Any FPGA based design is controlled using combinational logic design and these techniques are commonly designed by Finite State Machine (FSM) design[4]. Traditionally existing method of FPGA based on FSM is usually composed of a control unit with FFs

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and Look Up Tables (LUTs) which are programmable and combinational logics[5]. These elements are more power consuming, hence if the power consumption of FSM is reduced then entire design power consumption is decreased significantly. In the past there are many techniques have been already proposed to optimize the power consumption of FPGA based design using FES decomposition[6,7], gating techniques for power as well as clock[8,9], routing techniques, partial and dynamic reconfiguration. In this work a FSM based power optimization is proposed using one-Hot encoding and binary encoding based system. In this method unutilized memory bits are used to store FSM encoded state bit and this will reduce the burden due to routing resources[6]. Here a clock gating technique[10] is used to reduce the switching function additively on circuit signals, by temporarily disabling of clock signal in specific registers, whenever their outputs are not relevant.

## 2. Finite State Machine

Finite state machine consist of number states which gives a output to the given input. It act as the backbone of FPGA based system development can be represented using six tuple (I, O, S, r 0, δ, Y). Where I is set of inputs represent set of output, S is set of states and r0 is reset sate at initial stage. , δ: I X S = S is the state transition function and Y: I X S = O is the output function. This can be showed as state Transition Graph (STG) nodes are represented by stages and edges are given as output and input to state transition. Many methods are there to encode various state of finite machine. Optimal solution can be obtained by choosing right encoding method. Three methods are commonly used they are: Binary encoding, one-hot encoding and gray encoding. Every state of the state machine is represented using a unique pattern (i.e.) high (1) or Low (1) output signal from registers[7,11].

### 2.1 Binary Encoding

This type of encoding requires very less logics to be implemented so that only few Flip- flops are used. Flip flop used for this encoding is equal to the number of state variables. Only state machine with fewer gates can use this encoding technique and is mostly efficiently used in PLA'S and CPLD's. Major drawback of this system is it requires tedious decoding process and consumes more power[11].

### 2.2 Gray Encoding

Gray encoding is preferred asynchronous state bits are obtained as output. Intermediate logics are avoided in this method of encoding. For all the logic which reads state bit asynchronously then output is not predictable. Gray code uses registers same as binary encoding but encoding logic involved is complex .this type of encoding is high preferred in case of PLA and CPLD applications. Switching time is less in this type of encoding. In gray coding one bit is changed for every consecutive state[7].

### 2.3 One-Hot Encoding

As the name indicates it uses only one bit state variable for high (1) or HOT for any number of states. Hence it uses one bit, number is number of state is equal to number of flip flops. Decoding is simple as it can be derived from the previous state. This is faster method as it uses one bit to check any state. This type of encoding is suited in case of FPGA implementation for more number of flip flops and power will be less consumed as it is area optimized[7].

## 3. Clock Gating

Dynamic power management can be called as Clock-gating, which is a technique to control clock to reduce power consumption. A gate- control signals added to disable the clock when it is not in use. Power consumption can be reduced by avoiding unnecessary charging and discharging of unused circuits. Gate clock is formed to control the clock signal by AND the clock signal with control signal and then it is given to control various components in the circuit[8]. Control signal decides the module where gate clock should be applied[12].

Figure 1 represents the OCEM implementation using one hot encoding using FSM. The OCEM array contents are configured with state bit encoding and output from state machine. The sequence detector in the above figure points towards address decoding latch, it starts from the initial state with address 0000 and at the next stage the counter moves to next address and consecutively if it reaches the final state 0001 then the sequence detector detects end of the task. Then the command is passed to start next task by setting and clearing location address accordingly from first address of memory location. The embedded memory block in the FPGA can be reconfigured to high or low in case of any reset signal. Initial position can be set or cleared as the signal is routed to the address of input in the memory array.

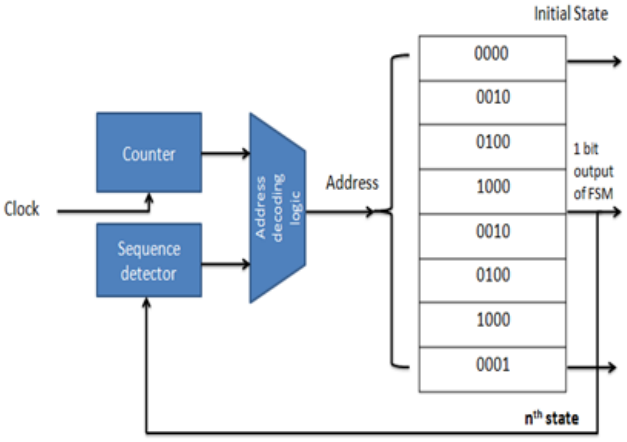


**Figure 1.** Implementation of one hot state encoding in OCEM.

## 4. FPGA Implementation

Functional block diagram of proposed OCEM FSM implementation is shown in Figure 2, which composed of M4k memory array, memory controller, task execution unit, sequence detector and UART controller[10].

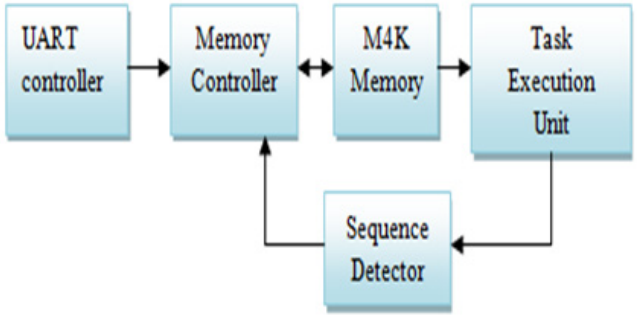


**Figure 2.** Block diagram of proposed OCEM FSM implementation.

### 4.1 Memory Controller

Memory controller is used to read the next state from M4k on chip embedded memory and also to modify the content in run time without affecting the architecture. Process of changing OCEM content is much faster than going through the entire process of synthesis, placement and routing process[9]. RTL view of o chip embedded memory and memory controller is shown in Figure 3 and Figure 4.

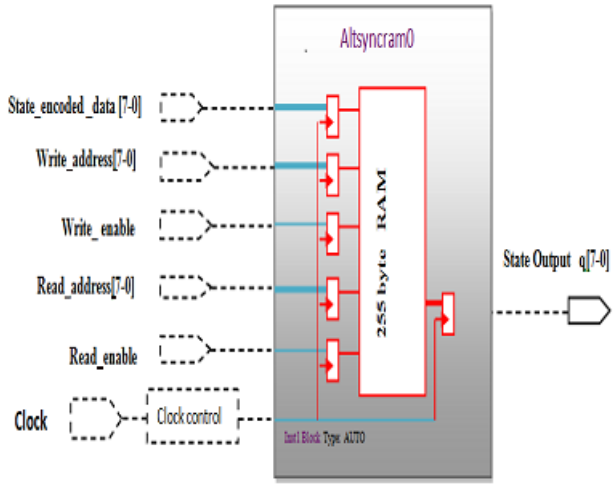


**Figure 3.** M4k on Chip Embedded Memory.

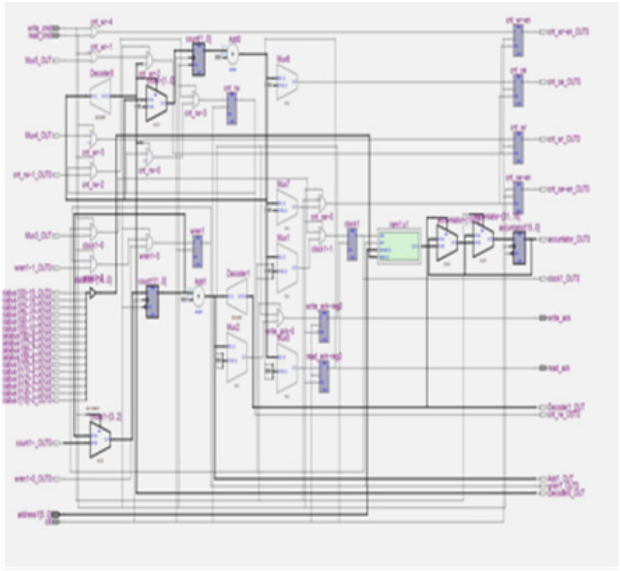

**Figure 4.** RTL view of memory controller.

### 4.2 Sequence Detector

Sequence detector is a sequential circuit which works with interconnection of sequence of logical blocks. The data obtained between one operation to another is stored as chain of bits which can be given as input[11]. The bits are either 1 or 0. When the output of the detector reaches i then the assigned output is reached and the system is reset for next operation to 0000. Figure 5 shows the RTL view, Figure 6 shows the state diagram and Figure 7 shows the map view of sequence detector.

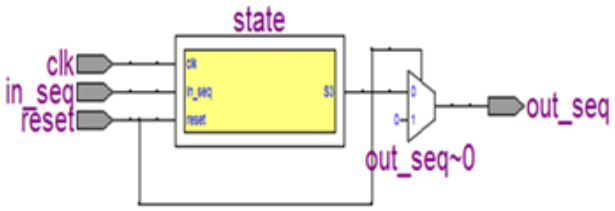


**Figure 5.** RTL View of State sequence detector.

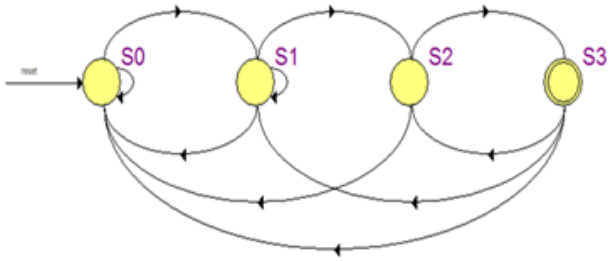


**Figure 6.** State diagram representation.

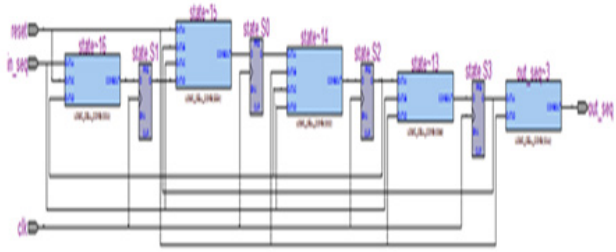

**Figure 7.**

## 4.4 UART Controller

UART is a serial communication device which is used to send data UART is a serial communication device which is used to send data efficiently over long way with reduced channel cost. Serial communication reduces the error in transmission and error correction is easy in case of serial data transfer. UART controller is used here to transmit the downloaded encoded state bit from PC to on chip embedded memory. This data will be transmitted at a baud rate of 9600 and the standard baud rates are 19200, 38400 and 128000. Standard baud rates are supported by this UART controller for various data transmission. RTL view of UART controller is presented in Figure 8.

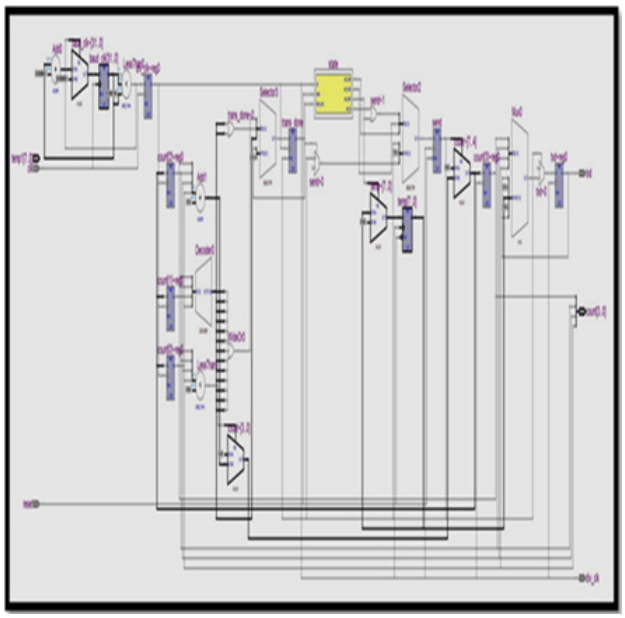

**Figure 8.** RTL view of UART Controller.

# 5. Result and Discussion

One hot state encoding has chosen to evaluate the proposed technique with traditional technique for which standard power consumption applications are chosen, such as FSM based 32bit ALU, 16 bit LFSR FSM based AES encryption core and UART controller. The comparison is performed with ALTRA cyclone II EP2C35F672C6 FPGA and logic utilization. Power dissipation for proposed technique and traditional technique are tabulated in Table 1. The traditional method use Look up table and flip-flop based FSM design is compared with the proposed OCEM method[12].

Chip planner view of 32bit ALU, 16 bit LFSR FSM based AES encryption core and UART controller are shown in Figure 9. Table 2 was given the comparison

**Table 1.**

| | Look up table and flip-flop based FSM | | | | OCEMP | | | |
|---|---|---|---|---|---|---|---|---|
| | AES | LFSR | ALU | UART | AES | LFSR | ALU | UART |
| Power(mW) | 239.45 | 197.05 | 78.36 | 68.86 | 124.24 | 72.68 | 78.10 | 68.53 |
| Logic elements | 9,765 | 76 | 229 | 300 | 4,544 | 32 | 158 | 59 |
| Registers | 9189 | 16 | 132 | 48 | 3968 | 8 | 24 | 20 |
| Total pins | 385 | 21 | 99 | 19 | 385 | 21 | 94 | 16 |
| Memory bits | 409,60 | 0 | 0 | 0 | 704,512 | 320 | 120 | 128 |

**Table 2.**

| Various clock frequency | AES core | | LFSR | | ALU | | UART | |
|---|---|---|---|---|---|---|---|---|
| | With clock gating | Without clock gating | With clock gating | Without clock gating | With clock gating | Without clock gating | With clock gating | Without clock gating |
| 10 MHZ | 40.33 | 33.29 | 32.12 | 31.11 | 30.55 | 30.10 | 28.25 | 27.32 |
| 25 MHZ | 63.44 | 60.43 | 43.32 | 39.11 | 46.14 | 45.19 | 37.64 | 36.00 |
| 27 MHZ | 68.24 | 65.97 | 45.21 | 42.66 | 49.16 | 47.24 | 40.22 | 37.23 |
| 50 MHZ | 124.24 | 122.11 | 72.68 | 68.49 | 78.10 | 74.22 | 68.53 | 65.44 |

analysis of with and without power gating technique for various clock frequencies.

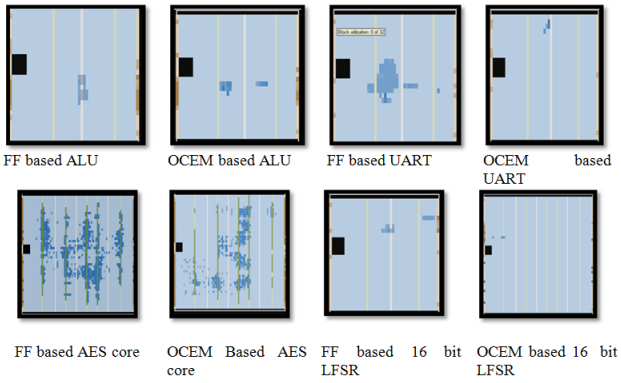


**Figure 9.** Chip planner view of ALU, UART, AES and LFSR.

## 6. Conclusion

FPGA based FSM implementation is presented in this work, where the M4K is implemented on the FPGA embedded memory blocks. From the analyses on result obtained from experiments shows that power consumption is reduced from 4% to 26% .when compared with FF based method. In this method clock is stopped in case of FSM idle state. OCEM based design has reduce the area utilization as well it is flexible for FSM to change functionality without any modification or compilation and only thee memory block is modified. The power analyses of the proposed model id performed and parameters are also analyzed.

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