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Performance Investigation of Gate-All-Around Nanowire FETs for Logic Applications

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Abstract

In this paper, SiC and Si Nanowire Field Effect Transistors (NW-FETs) with SiO_2 and HfO_2 gate oxide materials are simulated in various gate oxide thicknesses and channel diameters. In order to study the performance of these transistors in logic applications, the effect of channel material and diameter and also oxide material and thickness changes on the important switching parameters like delay time (τ_d), Power Delay Product (*PDP*) and Sub-threshold Swing (*SS*) are investigated. Results show that calculated parameters are sensitive to these changes. But the dependence of the parameters to the type of oxide material is higher in which by changing the oxide material to HfO_2 τ_d decreases considerably. In addition, the optimum feature for the best switching speed is obtained. This study shows that SiC-NWFETs are comparable with Si-NWFETs in logic applications.

Keywords: Delay Time, Nanowire Field Effect Transistor, Power Delay Product, Sub-threshold Swing, Switching Speed

1. Introduction

SiC has been extensively studied because of its physical properties such as wide band gap, high breakdown field, high thermal conductivity, high saturated drift velocity of the carriers and high temperature stability. Many researchers have been worked on SiC and its applications in various device fabrications. One of the SiC important applications is the Nanowires devices[1–6]. Some studies have investigated the Si and SiC effect on NWFETs performance[1–10]. Simulation and experimental results have shown that SiC NWFETs and Si NWFETs have identical performance. A comparison between their electrical characteristics have shown that their Sub-threshold Swing (SS) and also their on current (I_{on}) are approximately in the same level. In addition, SiC NW has higher thermal conductivity, higher band gap, higher electron drift velocity, higher breakdown electric field, and better physical and chemical stability. Also, appear to be competitive in electrical transport properties and could be an excellent candidate for future high power and high frequency nanoelectronic applications[1–10].

On the other hand, the gate insulator material of NWFETs has a great significance. One of the most widely used materials is SiO_2. But, one of the disadvantages of SiO_2 in comparison with SiC is its small dielectric constant (2.5 times smaller). Also the week interface of SiC/SiO_2 results in an inconvenient increase in the gate oxide electric field in comparison with semiconductor. So need for novel oxide with higher or at least comparable dielectric constant with SiC in device applications. HfO_2 is the promise candidate for replacement of SiO_2[11–13].

In this paper, performances of NWFETs in logic applications will be investigated. In this regard, a ballistic model based simulation is applied on NWFETs with two different channel materials including Si and SiC, with different diameters. Then the impact of substituting HfO_2 for SiO_2, and variation of oxide thickness on some important parameters like SS, PDP, and τ_d will be investigated and compared. It should be mentioned that tight binding

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method is used to calculate effective mass and energy bad gap because the energy bad diagram of Nano wire is dependent to its diameter.

The rest of paper includes 4 sections. The device structure and simulation method are presented in Section 2. Results and analysis are presented in section 3 and finally, conclusions are drawn in section 4.

2. Device Structure and Simulation Method

Figure 1 illustrates a schematic representation of cylindrical Gate-All-Around (GAA) semiconductor Nanowire FET. The channel semiconductor material supposed to be Si or SiC and the gate oxide material is supposed to be SiO_2 or HfO_2. The channel length (L_{ch}) and drain-source voltage (V_{DS}) are supposed to be 10 nm and 0.4 V, respectively. In this study, the channel diameter (d_{ch}) supposed to be 0.61, 0.92, 1.23 nm, and the gate oxide thickness (t_{ox}) is supposed to be 0.7 and 1.5 nm for each device.

At the first step of simulation, energy band structures of cylindrical Si and SiC Nanowire are calculated using tight binding method, for various diameters d_{ch} = 0.61, 0.92, 1.23 nm. Due to energy band structure, the electron effective mass can be calculated using following equation

$$\frac{1}{m^*}\left(\frac{1}{h^2}\right)\left(\frac{\partial^2 E}{\partial k^2}\right)$$

In which $m^* = m_0 m_t$, and m_0 is electron rest mass in free space, m_t is the electron effective mass in the transport direction[8]. The electron effective mass is calculated at various diameters d_{ch} = 0.61, 0.92, 1.23 nm, for materials Si and SiC[8,15]. The simulation results are shown in Table 1. At the next step, based on the energy band structure (the electron effective mass and energy band gap) for each diameter and material of NW, the I_{DS}–V_{GS} characteristics of the device of Figure 1 are calculated using the ballistic model[14,16]. The

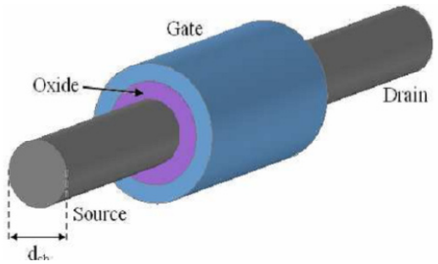

Figure 1. Schematic representation of cylindrical gate-all-around semiconductor NWFET[14].

some important parameters in logic application will be calculated and investigated in the following section.

3. Results and Analysis

In this section, we investigate some important parameters for logic applications such as SS, PDP, and τ_d. The various materials of channel, diameters of channel and oxide thicknesses are strategies for improving the performance of parameters.

3.1 Delay Time

One of the important criteria for evaluating transistor switching speed is delay time (τ_d) that is defined by

$$\tau_d = \frac{(Q_{on} - Q_{off})}{I_{on}} \quad (2)$$

In which Q_{on}, Q_{off}, and I_{on} are channel charge in on state, channel charge in off states and channel current in on state, respectively[14,17]. Figure 2 shows τ_d versus I_{on}/I_{off} for

Table 1. The electron effective mass for Si and SiC NW at three different diameters d_{ch} = 0.61, 0.92 and 1.23 nm.

Channel diameter (nm)	Electron effective mass	
	SiC	Si
0.61	0.66	0.55
0.92	0.57	0.46
1.23	0.49	0.41

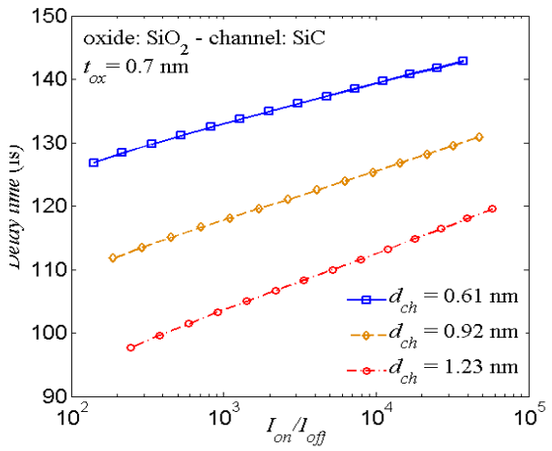

Figure 2. τ_d versus I_{on}/I_{off} ratio for SiC as the NW of the channel and SiO_2 as gate oxide with t = 0.7 nm in different channel diameters d_{ch}= 0.61, 0.92 and 1.23.

the transistor of Figure 1 with the SiC and SiO_2 as material of channel and gate oxide, respectively. The diameters of channel d_{ch} = 0.61, 0.92, 1.23 nm and oxide thickness t_{ox} = 0.7 nm. As it can be seen increase in channel diameter increases switching speed. As higher switching speed is desired in logic applications, to reach improved performance, the best state of this simulation is selected (d_{ch} = 1.23 nm) for the next stage of simulating (will be shown in Figure 3).

Figure 3 illustrates the device with SiC-NW channel is simulated in the best channel diameter of 1.23 nm, and it aims to investigate the dependence delay time to the oxide material in different thicknesses. Changing from SiO_2 to HfO_2 it can be seen that the slope of delay time increases which shows higher sensitivity of τ_d to HfO_2. Based on the curves of this Figure shown it can be inferred that HfO_2 has better performance on the device speed. In addition, by decreasing oxide thickness τ_d decreases for both oxide materials. Consequently, HfO_2 with thickness of 0.7 nm and the channel with diameter of 1.23 nm are the best alternative for the device of Figure 1. The effect of channel material on the switching speed is shown in Figure 4. It is shown delay time in SiC channel material is more than Si so that SiC decreases switching speed. Consequently, it is obvious that the best oxide is HfO_2 with thickness of 0.7 nm and the best channel material is Si with diameter of 1.23 nm.

Simulation results can be justified and analyzed based on analytical ballistic model of FETs. Based on equation (2) it is seen that time delay is in inverse proportion with on current (I_{on}). I_{on} relation is[7,18].

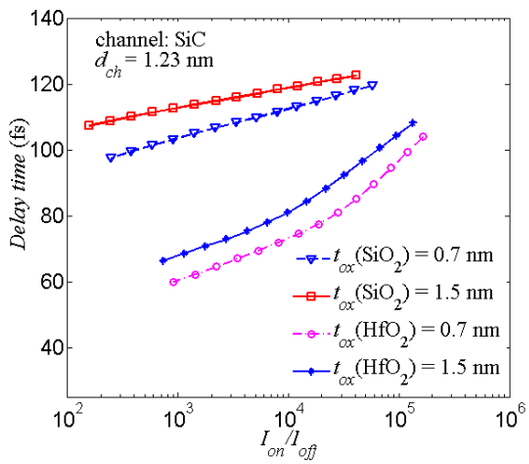

Figure 3. τ_d versus I_{on}/I_{off} forSiC as the NW of the channel with the best inferred diameter of 1.23 nm and SiO_2 and HfO_2 as gate oxide with t = 0.7 and 1.5 nm. It can be inferred that HfO_2 with thickness of 07 nm is the best oxide.

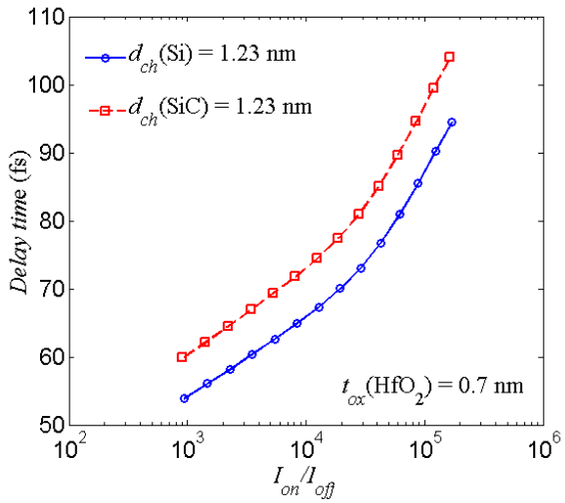

Figure 4. The τ_d versus I_{on}/I_{off} ratio for SiC and Si as two NW of the channel with diameter of 1.23 nm and HfO_2 as better gate oxide with t_{ox} = 0.7 nm.

$$I_{DS} = wc_{ox} v_T (V_{GS} - V_T) \quad (3)$$

$$v_T = \sqrt{\frac{2K_B T}{\pi m^*}} \quad (4)$$

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_r}{Ln\left(\frac{2t_{ox} + d_{ch}}{d_{ch}}\right)} \quad (5)$$

In which v_T is electron velocity, m* is the electron effective mass in the transport direction, $k_B T$ and C_{ox} are Boltzmann constant, the ambient temperature, the gate oxide capacitance, respectively. As it is shown in Table 1, effective mass decreases as channel diameter increases. Consequently, considering equation (4) velocity increases. On the other hand, according to equation (5) by increasing the channel diameter and the decreasing oxide thickness gate capacitance increases which in turn leads to an increase in on current (I_{on}) and a decrease in time delay, as shown in equation (2). In addition, if gate oxide changes to HfO_2, dielectric constant and as a result gate capacitance and on current (I_{on}) increase. This leads to an improvement in switching speed. Moreover, if channel material changes in to SiC the energy band structure changes, so that effective mass increases and consequently, based on equation (4) and (3) velocity and on current (I_{on}) decrease. Finally, according to equation (2) delay time increases.

3.2 Power Delay Product

Power Delay Product (PDP) is another important criterion of device performance in logic applications. These parameters show the needed amount of energy for a logic gate to switch output voltage from one logic state to another state[17]. The PDP is defined as[17]

$$PDP = \tau V_{DD} I_{on} = (Q_{on} - Q_{off}) \cdot V_{DD} \quad (6)$$

In this work V_{DD} is supposed to be 0.4 V. Figure 5(a) illustrates PDP variations versus I_{on}/I_{off} in different channel diameters for SiC-NWFET in which SiO_2 gate oxide has 0.7 nm thickness. It is obvious that PDP has downward trend when I_{on}/I_{off} increases. Also, PDP has lower amounts for higher channel diameters. Moreover, the effect of oxide material changes on PDP of SiC-NWFET is shown in Figure 5(b) in which the channel diameter is 1.23 nm

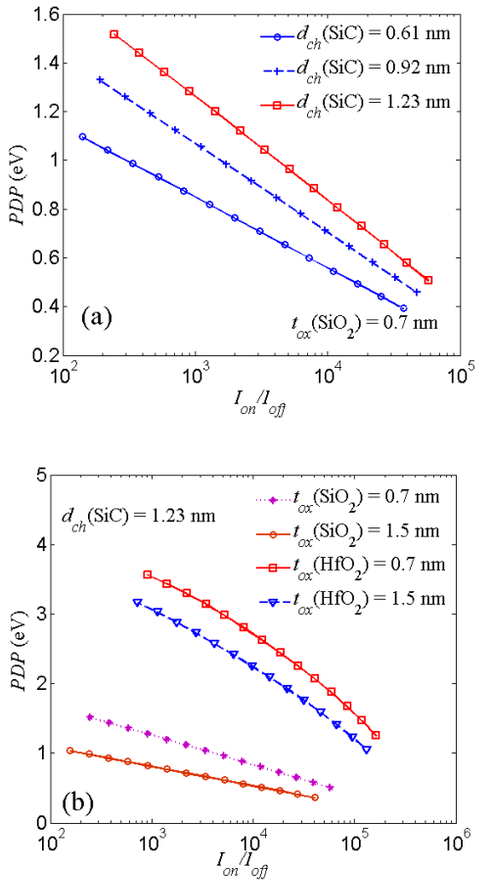

Figure 5. (a) The PDP versus I_{on}/I_{off} in channel diameters of 0.61, 0.92 and 1.23 nm for SiC-NWFET in SiO_2 gate oxide thickness t_{ox} = 0.7 nm. (b) SiC-NWFET in which the channel diameter is 1.23 nm and both SiO_2 and HfO_2 are used with thicknesses of 0.7 and 1.5 nm.

and both SiO_2 and HfO_2 are used with two different thicknesses. As it can be seen, HfO_2 oxide material represents higher PDP and more curve slopes. The latter shows that PDP is more sensitive toward HfO_2 changes.

This effect can be justified by equation (3) and (5). A decrease in channel diameter causes a decrease in gate oxide capacitance that in turn causes a decrease in I_{on}. Thus, according to equation (6), PDP decreases. In addition, as it can be inferred from Figure 5(b) PDP increases if oxide thickness decreases. Based on analytical models corresponds to equation (5), a decrease in oxide thickness and an increase of ε_r due to HfO_2, causes an increase in C_{ox} so that based on equation (3) I_{on} increases and consequently, PDP increases according to equation (6).

PDP changes versus the change of channel material from SiC to Si are depicted in Figure 6. The optimum features for delay Time, which is the channel diameter of 1.23 nm and HfO_2 with thickness of 0.7 nm, are selected for this simulation. It is obvious that the PDP for channel of SiC is slightly more than Si.

However, simulation results show that the lowest PDP is 0.28 eV and 0.29 eV for Si and SiC, respectively, which are obtained for SiO_2 gate oxide material with thickness of 1.5 nm and channel diameter of 0.61 nm.

3.3 Subthreshold Swing

Sub-threshold Swing (SS) is another important parameter to evaluate switching performance of a semiconductor NWFET. SS value can be obtained by[15]

$$SS = \left(\partial(\log I_{DS})/\partial V_{GS}\right)^{-1} \quad (7)$$

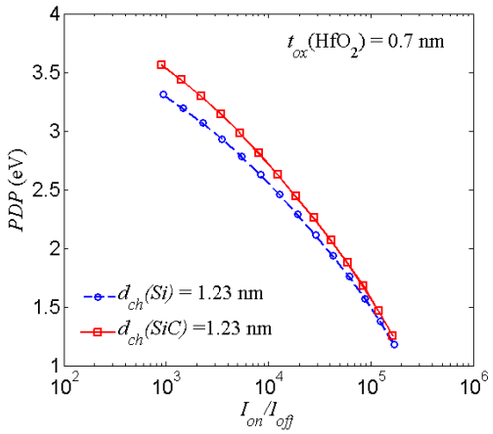

Figure 6. *PDP* variations versus I_{on}/I_{off} for Si and SiCNWFEt with 0.7 nm thick HfO_2 gate oxide and 1.23 nm channel diameter.

Figure 7(a), (b) and (C) show SS variation versus various channel diameters in different features. As it can be seen, sub-threshold swings of all three Figures have downward trends and semi-linear behaviors versus channel diameter increase. Figure 7(a) shows the effect of changing oxide material from SiO_2 to HfO_2 on SS of the SiC-NWFET with t_{ox} of 0.7nm. Results imply that SS is reduced by diameter increase and the slope of changes for HfO_2 is less than SiO_2. Figure 7(b). shows SS dependence to the oxide thickness. In this simulation, the channel material is SiC and the oxide is HfO_2. As it can be inferred by reducing oxide thickness SS reduces and switching speed improves. Also, if SiO_2 is replaced by HfO_2 the switching speed is better due to lower SS represented by HfO_2.

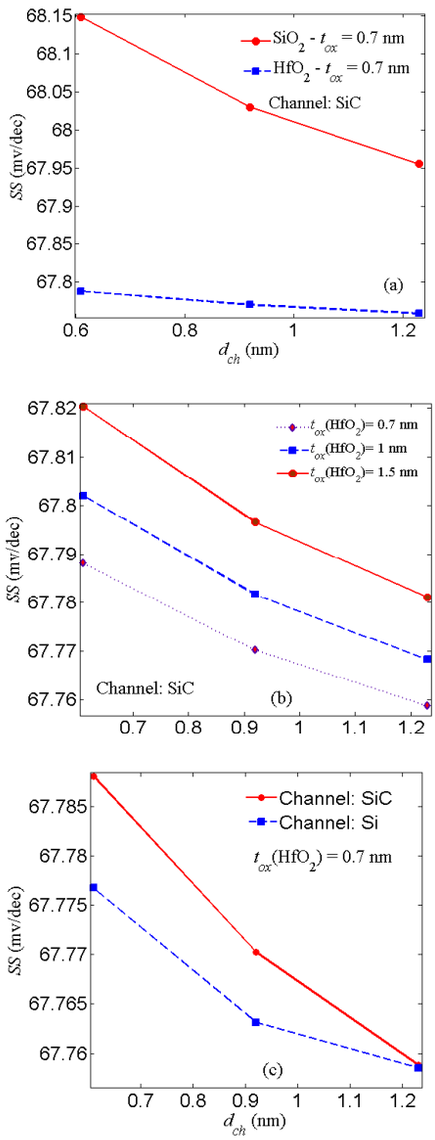

Figure 7. Subthreshold swing variation versus channel diameter with (a) oxide materials of SiO_2 and HfO_2 for thickness of 0.7 nm, (b) Oxide material HfO_2 with thicknesses of 0.7, 1 and 1.5 nm and (c) channel materials of SiC and Si for HfO_2 thickness of 0.7 nm.

The influence of channel material including SiC and Si on SS is investigated in another simulation represented in Figure 7(c). According to pervious simulation results, HfO_2 is opted as oxide material with t_{ox} of 0.7 nm. By changing SiC to Si, SS decreases that shows Si has better performance.

As a conclusion, it can be said that simulation results show that estimated parameters are highly sensitive to channel diameter, oxide thickness, and oxide material changes. However, these parameter dependencies upon oxide material changes are more significant. It was shown that an increase in the channel diameter caused an increase in switching speed, thus according to the simulation values, d_{ch} =1.23 nm was chosen as the best value for further simulations. Then, another simulation depicted that HfO_2 oxide has better switching speed performance in comparison with SiO_2. In addition, it was shown that oxide thickness reduction can help to have better switching speed. Consequently, based on performed simulations, the best oxide with optimum thickness and the best channel diameter was selected that are HfO_2 with 0.7 nm thickness and 1.23 nm channel diameter. Conversely, PDP simulations depicted that PDP for the optimum selection is high, so that for the best switching speed higher energy consumption is needed. Table 2 illustrates numerical results of delay time, PDP and SS of SiC-NWFET and Si-NWFET for SiO_2 and HfO_2 oxide materials, d_{ch} =1.23 nm and t_{ox}= 0.7 nm.

In order to show, the effect of channel material on NWFET logic performance a numerical comparison is shown in Table 2 for Si and SiC. Table 2.A is for SiO_2

Table 2. Comparison between the logic performance of SiC and Si NWFETs based on logic important parameters. Simulations were performed in d_{ch} = 1.23 nm and t_{ox} = 0.7 nm.

Table 2.A. A. For SiO_2

Prameters	SiC-NWFET	Si-NWFET
I_{on}/I_{off}	0.57×10^5	0.61×10^5
τ	119.55 fs	108.79 fs
SS	67/95 mV/dec	67.93 mV/dec
PDP	0.5 eV	0.49 eV

Table 2.B. For HfO_2

Prameters	SiC-NWFET	Si-NWFET
I_{on}/I_{off}	0.16×10^6	0.16×10^6
τ	104 fs	94.52 fs
SS	67.759 mV/dec	67.758 mV/dec
PDP	1.25 eV	1.17 eV

and Table 2.B is HfO_2 oxide material. It is obvious from Table 2 that HfO_2 oxide represents better switching speeds.

As the aim of this study was investigation of NWFETs' logic performance, the I_{on}/I_{off} ratio was estimated between 0 up to 0.4 V for V_{GS}. It should be noted that the value of V_{DD} in our simulations was 0.4 V. This study proves that SiC NWFETs can have an acceptable performance in logic applications.

4. Conclusion

In order to investigate NWFET performance, a numerical simulation based on ballistic model has been utilized. The channel and the gate oxide have been considered to be SiC or Si and SiO_2 or HfO_2, respectively. The channel diameters have been considered to be 0.61, 0.92, and 1.23 nm and the gate oxide thicknesses have been considered to be 0.7 and 1.5 nm based on the done researches. Accordingly, some important parameters like delay time, power delay product, and sub-threshold swing have been compared in various states. In our simulation the tight binding method used to calculate the electron effective mass. It has been shown that switching speed increases by an increase in the channel diameter and switching speed can be modified by substituting HfO_2 for SiO_2 and also decreasing the oxide thickness. The results have shown that mentioned parameters are highly sensitive to the channel diameter, oxide material and thickness, but, they have greater dependency to the type of oxide material such that by changing oxide from SiO_2 to HfO_2 switching speed increases sharply. In addition, the optimum oxide thickness and channel diameter to have the best switching speed have been obtained. Numerical comparisons of the mentioned parameters have shown that best switching speed can be achieved by HfO_2 gate oxide with 0.7 nm thickness and 1.23 nm channel diameter in which its value for Si and SiC NWFET is 94.52fs and 104fs, respectively. In this state, the *PDP* value for Si and SiC-NWFET is 1.1 eV and 1.25 eV, respectively. Finally, this study has shown that SiC-NWFET performance in logic applications is comparable with Si-NWFET.

5. References

1. Rogdakis K, Lee SY, Bescond M, KwonLee S, Bano E, Zekentes K. 3C-Silicon Carbide Nanowire FET: An Experimental and Theoretical Approach. IEEE Trans Electron Dev. 2008; 55(8):1970–6.
2. Rogdakis K, Bescond M, Bano E, Zekentes K. Theoretical comparison of 3C-SiC and Si nanowire FETs in ballistic and diffusive regimes. Nanotechnology. 2007; 18(47):1–5.
3. Janis A, Yao Y, Klement U. Dielectric Properties of SiC Nanowires with Different Chemical Compositions. IEEE Transactions on Nanotechnology. 2011; 10(4):751–6.
4. Zekentes K, Rogdakis K. SiC nanowires: material and devices. J Phys Appl Phys. 2011; 44(13):133001.
5. Trejo A, Calvino M, Ramos AE, Carvajal E, Cruz-Irisson M. Theoretical study of the electronic band gap inβ-SiC nanowires. Revista Mexicana De Fisica. 2011; 57(2):22–5.
6. Miranda A, Ramos AE, Cruz-Irisson M. Electronic Band Structure of Cubic Silicon Carbide Nanowires. Mater Sci Forum. 2009; 600–603:575–8.
7. Wang J. Device physics and simulation of silicon Nanowire Transistors [Ph.D Thesis]. Purdue University; 2005.
8. Zheng Y, Rivas C, Lake R, Alam K, Boykin TB. Electronic Properties of Silicon Nanowires. IEEE Trans Electron Dev. 2005; 52(6):1097–103.
9. Zhou WM, Fang F, Hou ZY, Yan LJ, Zhang YF. Field-Effect Transistor Based on β-SiC Nanowire. IEEE Electron Device Lett. 2006; 27(6):463–5.
10. Han R. A Study on Lightly-Doped Cylindrical surrounding-gate 6H-SiC Nanowire FET. IEEE-ICSE2012 Proc; Kuala Lumpur, Malaysia; 2012. p. 137–40.
11. Tang WM, Leung CH, Lai PT. A Study on Hydrogen Reaction Kinetic of pt/HfO2/SiC Schottky-Diode Hydrogen Sensors. In: Innocenti A (editor). Stoichiometry and Materials Science-When Numbers Matter. 2012. p. 263–82.
12. Erlangung Z. Structural analysis of HfO_2 and HfSi2ultra-thin films on Si(100).A photoelectron diffraction study [PhD thesis]. Dortmond University; 2008.
13. Gupta SK, Singh J, Akhtar J. Materials and Processing for Gate Dielectrics on Silicon Carbide (SiC) Surface. Physics and Technology of Silicon Carbide Devices. 2013. p. 207–34.
14. Sedigh-Zyiabary SA, Saghafi K, Faez R, Moravvej-Farshi MK. Numerical Investigation on the Temperature Dependence of the Cylindrical-Gate-All-Around Si-NWFET. Mod Phys Lett B. 2011; 25(29):2269–78.
15. Yan B, Zhou G, Duan W, Wu J, Gu L-B. Uniaxial-stress effects on electronic properties of silicon carbide nanowires. Applied Physics Letters. 2006; 89(2):1–3.
16. Rahman A, Guo J, Datta S, Lundstrom M. Theory of Ballistic Nanotransistors. IEEE Transactions on Electron Devices. 2003; 50(9):1853–64.
17. Koswatta SO, Nikonov DE, Lundstrom MS. Computational Study of Carbon Nanotube p-i-n Tunnel FETs. Electron Devices Meeting, IEDM Technical Digest; 2005. p. 518–21.
18. Lundstrom M. The Nanoscale MOSFET: Physics and Limits. Purdue University; 2010.