

Material Flow Control Procedure Considering the Status Information of Transporters

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Abstract

A semiconductor production system has sophisticated manufacturing operations and needs high capital investment for its expensive equipment, which warrants efficient real-time flow control for wafers. To dispatch carriers of wafers in the semiconductor lines, this paper presents an unload request logic, which determines the destination of a carrier of wafers when a carrier finishes its operation, and a load request logic, which determines the next carrier to fill the newly available buffer space when a carrier leaves a buffer. The dispatching procedure first determines the transportation time of each carrier to its destination by each unit of transportation equipment and determines the destination machine by the unload request logic or target carrier by the load request logic. When there is no available buffer space at the machine tool, the procedure allows carriers to stay at the current buffer and determines the delay time, which is used to determine the destination in the unload request logic. Performance of the material flow control procedure is verified by an example.

Keywords: Control, Material Flow, Semiconductor, Transporter, Wafer

1. Introduction

Semiconductor production lines belong to the equipment industry and it is important to control the wafers in a real time for the efficient use of machines. The control system of semiconductor production lines consists of two parts; the first part is scheduling and dispatching layers, and the second part is material flow control and machine control layers.

Although the dispatcher commonly used in the upper layer considers such current status information as the availability of machines, they do not consider future status information of machines and lots at the time of unload and load request. In particular, the transporters such as AGVs are separately taken into consideration after the completion of decision making by the dispatcher.

The semiconductor production lines are comprised of bays and the same type of machines with similar functions are grouped in the bays. Each of the groups has the predetermined operations that can be processed and the operation processing time is set equal to each other in the groups. The predetermined operations among groups may be duplicated. Several types of products are produced in

the line and the operations and layers in which the process flows are different for each type of products.

This paper presents the core logic for dispatching using information on the current and future state of systems in the semiconductor production lines where the same types of machines are grouped in the bays. The logic includes the procedure for selecting destination equipment by a lot which completes its processing and the one for selecting a lot for the next processing by a buffer which becomes available after unloading.

In the logic, considering such status of the transporter as the availability of the transporter, the transportation time from departure to arrival point, and the future transportation schedule information simultaneously, the logic determines the destination equipment and a lot to process next considering the possible lot delay time when the transporter arrives at the destination.

There are many difficult problems in the control of the LCD and semiconductor production systems due to the characteristics of the systems. In particular, re-entrant flow characteristic is the LCD and semiconductor production lines' own special one and is the factor that makes it difficult to design a line and schedule a process, etc.

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From the 1980s to 1990s, many researchers focused on single operational criterion of lot releasing, due-date scheduling, batch scheduling, WIP balancing or bottleneck feeding for fab scheduling. Since the mid 1990s, realizing that a single criterion cannot effectively control a complex fab, more integrated approaches appeared. Hierarchical approaches have widely been used for the integration. Uzsoy et al.^{17,18} contributed much to this turnaround by defining the characteristics and difficulties of semiconductor production, status of research, and suggesting directions for future research.

Lot releasing methods tries to avoid starvation of bottleneck machines using flow rate of a layer for a fab^{4,11,19}. For bottleneck feeding, mathematical programming and heuristic methods are frequently used considering such detailed aspects of litho machines as setup time and the number of masks^{1,10,12}. They focused on the bottleneck machine scheduling pointing out that the bottleneck machine played a major role in the performance of the whole line. Because most fab equipment is litho machines, heuristic models, MIP models, and sequencing rules are applied to the problems considering the number of masks and the balancing. And Koo et al.⁷ presented a vehicle dispatching algorithm for highly loaded semiconductor production considering bottleneck machines first.

For the integrated scheduling, many research used hierarchical approaches of WIP balancing and bottleneck feeding. TB (Two Boundary) method is for WIP balancing and many research used this method^{8,13,14}. Recently Chung and Jang³ proposed an MIP model integrating WIP balancing and bottleneck feeding for high-volume semiconductor fab scheduling. Tirkel¹⁶ developed flow time forecasting models using knowledge discovery in databases. The data include wafer lot transactions extracted from the manufacturing execution system of an 8-inch flash memory factory. The flow time is forecasted for a single lot at a given production step.

Related to the research for dispatching, Jang et al.^{5,6} presented an efficient policy for AGV and part routing in semiconductor and LCD production bays using information on the future state of systems where AGVs play a central role in material handling. Chand et al.² developed a family of rolling horizon procedures to minimize total completion time on a single machine with release time by using information about future job arrivals. Suh et al.¹⁵ presented an AGV routing procedure for wafer and LCD production using estimated expected waiting time for AGV service obtained by a stochastic modeling. Li et al.⁹

presented an adaptive dispatching rule whose parameters are determined dynamically by real-time information relevant to scheduling. They used such information as due date of a job, workload of a machine, and occupation time of a job on a machine to find the relations between weighting parameters and real-time state information to adapt these parameters dynamically to the environment.

2. Selection of Destination and Lot

In this section, we present a logic performing real time dispatching when the processing of a lot is completed at a processing machine or the buffer of a processing machine becomes empty. It consists of URL (Unload Request Logic) selecting a destination machine and a transporter when an unload request is made with the processing completion of a lot at a processing machine and LRL (Load Request Logic) selecting a lot when a load request is made with the availability of a machine buffer.

2.1 Occurrence of Blocking

Now suppose that the processing of lot L is completed in machine S at time T_0 , then the destination for the operation of the next step of lot L should be determined. Now consider the case when L is sent to an arbitrary machine D among NOM (Next Operation Machine) of L, selecting the machine D as an arrival point. Then according to the departure and arrival time of L, the following cases may be occurred.

- Occurrence of Blocking at the Arrival Point

Such a case that L is blocked at the arrival point because the buffer of the arrival point is not available when L arrives at the arrival point may be occurred.

Now let TV_{VL} be the assignment time of V to L when L is transported from S to D using transporter V, TD_{SL} be the departure time of L from S, TA_{DL} be the arrival time of L to D, then the transportation time of V becomes $TR_S + LT + TR_{SD} + UT$ and the waiting time of L waiting on the transporter due to the unavailability of the buffer of D when L arrives D is $TL_D - TA_{DL}$. Here, TR_S denotes the time required for V to travel from V to an arbitrary point S. In this paper, we consider the case when the buffer of arrival point is not available L is waiting on the transporter until the buffer of the arrival point becomes available instead L is sent either to another machine whose buffer is available

or to the stocker. At this time, if there are other lots being transported with L in V or planning to use V then the operations of these lots may be delayed.

- Occurrence of Blocking at the Departure Point

If L is blocked at the arrival point when L is sent to a machine among NOM upon completing of operation at once, we consider making the departure of L delayed at the departure point instead of departing from the departure point at once so that L can be arrived at the arrival point when the buffer of the arrival point becomes available. By doing this, the waiting time of L that may be happened at the arrival point can be avoided.

Now we calculate a new TV'_{VL} satisfying the condition of equation (1) when TL_D , the time when the buffer of the arrival machine becomes available, is given. Equation (1) means that L should be arrived at D after the buffer of D becomes available and is the condition that the buffer of the arrival point should be available when the transporter arrives at the destination. When the new TV'_{VL} is found, the transporter V is assigned to the lot L at this time.

$$TV'_{VL} \geq TL_D - TR_S - LT - TR_{SD} \quad (1)$$

Like this, blocking of lot at the arrival point can be avoided by delaying the departure of the lot at the departure point. The reason for this is to reduce the waiting time of the lot at the arrival machine and the delay time of the other lots connecting to the lot. In this case the delay time of the departure of L at the departure point is $TL'_{SL} - TD_{SL}$.

2.2 Composition of Connection Group

Now, let W_L be a transportation schedule of a transporter for lot L and if the W_L is newly set, then new transportation schedules including W_L are composed. Let the new transportation schedules including W_L be W_i , $i = 1, \dots, n$ and the set of these schedules be $W = \{W_1, W_2, \dots, W_n\}$. And let these W_i , $i = 1, \dots, n$ have serial numbers according to their start time. Then these transportation schedules W_i , $i = 1, \dots, n$ can be classified into groups by their start time and finish time.

$$W = \{G_1 \cup G_2 \cup \dots \cup G_w\}, G_i \cup G_j = \emptyset, \forall i \neq j, \text{ and } i, j = 1, \dots, w \quad (2)$$

Here, we define G_i as a connection group and $GI_i = \{i1, i2, \dots, in_i\}$ as an index set of W_i , $i = 1, \dots, n$, composing G_i . And each GI_i is composed to be satisfied with the following equation (3) and (4).

$$FW_{jj \leq k-1} > SW_k \text{ where } j, k \in GI_i \quad (3)$$

$$FW_j \leq SW_k \text{ where } j \in GI_i, k \in GI_{i+1} \quad (4)$$

Then each connection group is composed with transportation schedules connected to each other and the transportation schedules are not connected to each other between the connection groups. The equation (3) is the condition that the transportation schedules are connected to each other in the group and the equation (4) is the condition that the transportation schedules are separated from each other between the groups.

2.3 Delay Time of Lot

As transporters can carry multiple lots, the transporter may be carrying other lots together with the current lot L . Let us suppose that the transport is carrying another lot l . Then the process start time and finish time of l might be delayed because l arrives later than the scheduled time at the destination as the transport is waiting at the destination. And if there is another lot connected previously to the lot l , the lot may also be delayed. That is, if W_L is delayed then the start time and finish time of the transportation schedules after W_L may be delayed.

Now let the connection group G_i be composed of $G_i = \{W_{i1}, W_{i2}, \dots, W_{in_i}\}$ and let DG_i be the delay time of G_i . Then, if G_i is delayed then the transportation schedules composing G_i are also delayed and if we assume that all schedules are delayed with the same amount of time, DG_i can be calculated as equation (5) and (6). At this time, DT_{DL} is defined as the unloading delay time of L due to the waiting at the destination D . In the equation (5), SW_{i1} is the start time of G_i which is the start time of the first transportation schedule composing G_i and FW_{in_i} is the finish time of G_i which is the finish time of the last transportation schedule that compose G_i . ($SW_{(i+1)1} - FW_{in_i}$) is the slack time between G_i and G_{i+1} .

$$DG_i = \left(DT_{DL} - \sum_{k=1}^{i-1} (SW_{(k+1)1} - FW_{kn_k}) \right) \times n_i \text{ where } i > 1 \quad (5)$$

$$DG_i = DT_{DL} \times n_i \text{ where } i = 1 \quad (6)$$

Meanwhile, the transportation schedules in the connection group can have different delay times according to the status of the arrival points. Now, let us consider a case when a lot is moved by the transportation schedule W_{ij} , $j = 1, \dots, n_i$ in G_i . At this time, assume that W_{ij} is the transportation schedule moving lot l to machine m , and when l arrives at the machine m at time TA_{ml} late than the scheduled arrival time due to the delay of L , lot k is under processing at the machine m and there are other lots waiting for processing

at the buffer of m and let the set of these other lots be R . Then expected processing completion time of l at m , TC_{ml} , can be calculated as equation (7).

$$TC_{ml} = \max\left(TC_{mk} + \sum_{j \in R} PT_{mj}, TA_{ml} + DT_{ml} + UT\right) + PT_{ml} \quad (7)$$

That is, the expected processing completion time of lot l can be obtained by adding the processing time of lot l at the arrival machine to the maximum time between the processing completion time of a lot under processing at the arrival machine plus the processing time waiting for processing at the buffer of the arrival machine and the completion time of unloading lot l .

Thus the delayed time for the processing of l due to the late arrival of l to the destination can be calculated as equation (8), and if we let DG_{ij} be the delay time of W_{ij} then DG_{ij} can be calculated as equation (9).

$$TC_{ml} = \max\left(TA_{ml} + DT_{ml} + UT - TC_{mk} - \sum_{j \in R} PT_{mj}\right) \quad (8)$$

$$DG_i = FW_{ij} \left(DT_{DL} - \sum_{k=1}^{i-1} SW_{(k+1)l} - FW_{knk} \right) - TC_{mk} - \sum_{j \in R} PT_{mj} \quad (9)$$

Therefore, the delay time of lots in the whole transportation schedules can be calculated as equation (10).

$$LDT = \sum_{i=1}^w \sum_{j=1}^{n_i} DG_{ij} \quad (10)$$

2.4 Transportation via Stocker

Now, consider that lot L is not sent directly to a machine in NOM but sent to stocker K first and is chosen from the stocker later when the buffer of a machine in NOM becomes available. Then the lot delay time at the destination can be avoided but the processing start time of lot L may be late because of the extended transportation time to the destination. In this case the time required additionally for the transportation of lot L to the destination, ADT , is as equation (11). Where, N denotes the index of the processing machine farthest away from the stocker and $\left(\frac{1}{2}\right)TR_{NK}$ the average distance for an available transporter to travel to the stocker to move lot L in stocker to the destination.

$$ADT = TR_{SK} + \left(\frac{1}{2}\right)TR_{NK} + TR_{KD} - TR_{SD} + UT + LT \quad (11)$$

When transported via a stocker the utilization of the transporter in addition to the travel time to the destination increases and the average and maximum inventory levels also increase. After all, if the delay time of a lot is less than

ADT then it can be justified to send the lot to a machine in NOM even though it may be delayed at the arrival machine. Thus if the delay time of a lot is less than ADT then the destination of the lot is a machine in NOM.

2.5 Lot Selection Procedure

If a buffer of a processing machine becomes available after loading a lot at the buffer and there are no other lots reserving this buffer in advance then the available buffer selects a lot for the next processing. The candidates for selection are the lots currently waiting at the stocker and the lots currently under processing at POM (Previous Operation Machine). The selection criterion among these lots is how quickly the processing is completed upon arrival to the available buffer considering the delay time of lots.

Now suppose that a buffer B of a processing machine M becomes available, the procedure for B to select a lot is as follows:

- Select the earliest transportation schedule among the available time zones of the transporters to move the candidate lots to the destination buffer B of the machine M . Set the start time of the transportation schedule as the time later the finish time of a lot if the lot is under processing at the POM and the time later current time if the lot is waiting at the stocker. The transportation schedule set by this procedure may be inserted between existing transportation schedules or be connected to the existing transportation schedule.
- When the candidate lot l is transported by using the transportation schedule set as above, the expected processing completion time of lot l at machine M , TC_{MI} , is calculated as equation (12).

$$TC_{MI} = \max\left(TC_{mk} + \sum_{j \in R} PT_{mj}, TA_{MI} + UT\right) + PT_{MI} \quad (12)$$

And if the transportation schedule is connected with the existing transportation schedules, the lot delay time of the transportation schedules moved back due to the connection should be considered. Let the lot delay time be ΔT , and select the lot having the minimum time of TC_{MI} plus ΔT to the next processing lot.

3. Dispatching Procedure

The dispatching procedure presented in this paper to dispatch carriers of wafers in the semiconductor lines consists of URL (Unload Request Logic) to process the

unload request handling and LRL (Load Request Logic) to process the load request handling.

3.1 URL

Step 1: For each machine m in NOM of lot L completed at machine S

- 1.1 Determine W_L setting m to the arrival point.
- 1.2 If the buffer of m is available when L is transported by W_L , then calculate TC_{mL} .
- 1.3 If the buffer of m is not available, then calculate TC_{mL} and LDT for the next each case;
 - (i) In case that a transporter is waiting at m .
 - (ii) In case that departure of L is delayed at S .
- 1.4 Calculate rating R_m of m , i.e., $R_m = \min(TC_{mL} + LDT)$

Step 2: Determine the candidate of destination, CM, of L , i.e., $R_{CM} = \min_{m \in \text{NOM}} (R_m)$

Step 3: Determine the destination T of L , i.e.,
If $(R_{CM} - TC_{(CM)L}) \leq \text{ADT}$ then set $T = \text{CM}$, if not set $T = \text{Stocker}$.

3.2 LRL

Step 1: For each lot l that can be selected by buffer B of machine M that has just been available.

- 1.1 Determine W_l setting B to the arrival point.
- 1.2 Calculate expected processing completion time TC_{Ml} of l at M and lot delay time ΔT .

Step 2: Select lot $L = \{l | \min_l(TC_{Ml} + \Delta T)\}$ as the next processing lot.

3.3 Example

There are 6 machines from M0 to M5 in the system of this example and each of the processing time is shown in Table 1.

Two AGVs, V0, V1 are used as transporter in the system. The loading and unloading times of two AGVs are 0.5 minutes and 0.5 minutes respectively and the transportation times between each machine including stocker are 1.0 minutes.

Suppose that future processing and transportation schedules are as shown in Table 2 and Table 3 at the time T0.

Table 1. Processing time (Unit: Minute)

Machine	M0	M1	M2	M3	M4	M5
Processing Time	3.0	3.0	3.0	2.0	2.0	2.0

Table 2. Schedule of machine (Unit: Minute)

Machine	Lot	Start Time	Finish Time
M0	L	-	0.0
	L1	0.0	3.0
	L2	3.0	6.0
M1	L3	0.0	3.0
M2	L4	4.0	7.0
	L5	7.0	10.0
M3	L6	4.0	6.0
	L7	6.0	8.0
	L8	8.0	10.0
M4	L9	6.0	8.0
M5	L0	-	-

Table 3. Schedule of transport (Unit: Minute)

AGV	Buffer	TTW	Lot	Schedule					
				Time	0.0	1.0	1.5		
V0	B0	W0	L0	Place	K	M0	M0		
				Type	-	M	U		
				Time	2.0	3.0	3.5	6.5	7.0
		W1	L3	Place	M0	M1	M1	M4	M4
				Type	-	M	L	M	U
				Time	4.0	6.0	6.5	8.5	9.0
V1	B0	W1	L6	Place	M5	M3	M3	M5	M5
				Type	-	M	L	M	U
				Time	4.0	6.0	6.5	8.5	9.0

* K denotes stocker. M: Move, L: Loading, U: Unloading, W: Waiting.

Now, at the time T0, suppose that lot L is completed at M0. At this time V0 is carrying L0 to M0 passing through the stocker and V1 is parked at the position of M5. And let NOM of lot L be {M2, M3}.

- Set M2 as arrival point:
Determine W_L as shown in Table 4.
 $TA_{2L} = 4.5$ and at this time the arrival buffer is available.
 $TC_{2L} = \max(7.0 + 3.0, 4.5 + 0.5) + 3.0 = 13.0$ and as the delay time of lot L3 at M4 is 0, $LDT = 0.0$.
Therefore $R_{M2} = TC_{2L} + LDT = 13.0 + 0.0 = 13.0$.
- Set M3 as arrival point:
Determine W_L as shown in Table 5.
 $TA_{3L} = 5.5$ and at this time because the time when the buffer of M3 becomes available is $TL_3 = 6.5$ the arrival buffer is not available.
- In case of waiting
 $DT_{3L} = 1.0$ (Waiting time of lot L at M3)

Table 4. W_L in case that M2 is destination

AGV	Buffer	TTW	Lot	Schedule							
V0	B0	W_0	L0	Time	0.0	1.0	1.5	2.0			
				Place	K	M0	M0	M0			
				Type	-	M	W	U			
	W_1	L3	L3	Time	2.0	3.0	3.5	4.5	5.0	7.0	7.5
				Place	M0	M1	M1	M2	M2	M4	M4
				Type	-	M	L	M	W	M	U
	B1	W_L	L	Time	0.0	1.0	1.5	2.0	3.0	3.5	4.5
				Place	K	M0	M0	M0	M1	M1	M2
				Type	-	M	L	W	M	W	U

Table 5. W_L in case that M3 is destination

AGV	Buffer	TTW	Lot	Schedule							
V0	B0	W_0	L0	Time	0.0	1.0	1.5	2.0			
				Place	K	M0	M0	M0			
				Type	-	M	W	U			
	W_1	L3	L3	Time	2.0	3.0	3.5	5.5	7.0	8.0	8.5
				Place	M0	M1	M1	M3	M3	M4	M4
				Type	-	M	L	M	W	M	U
	B1	W_L	L	Time	0.0	1.0	1.5	2.0	3.0	3.5	5.5
				Place	K	M0	M0	M0	M1	M1	M3
				Type	-	M	L	W	M	W	U

$$TC_{3L} = \max(6.0 + 2.0 + 2.0, 5.5 + 1.0 + 0.5) + 2.0 = 12.0$$

$$TA_{4L3} = TA_{3L} + DT_{3L} + UT + TR_{34} = 5.5 + 1.0 + 0.5 + 1.0 = 8.0$$

$$TC_{4L3} = \max(8.0, 8.0 + 0.5) + 2.0 = 10.5$$

$$\text{If lot } L \text{ would not have waited at } M3, TC_{4L3} = \max(8.0, 7.0 + 0.5) + 2.0 = 10.0$$

$$\text{Thus } LDT = 10.5 - 10.0 = 0.5$$

$$\text{Therefore } R_{M3} \text{ in case of waiting} = TC_{3L} + LDT = 12.0 + 0.5 = 12.5$$

- In case of delay of departure

Determine W_L making L arrived at $M3$ after the buffer of $M3$ becomes available as shown in Table 6.

$$TC_{3L} = \max(6.0 + 2.0 + 2.0, 6.5 + 0.5) + 2.0 = 12.0$$

Expected arrival time of lot $L0$ scheduled to be arrived at $M0$, $TA_{0L0} = 1.0$

$TL_0 = 3.0$ (The time when the buffer of $M0$ becomes available)

Waiting time of $L0$, $DT_{0L0} = 3.0 - 1.0 = 2.0$

Delay time of $L3$ connected to $L0 = 2.0 - 0.5 = 1.5$

Thus $LDT = 2.0 + 1.5 = 3.5$

$$\text{Therefore } R_{M3} \text{ in case of delay of departure} = TC_{3L} + LDT = 12.0 + 3.5 = 15.5$$

Table 6. W_L making arrival after buffer of $M3$ becomes available

AGV	Buffer	TTW	Lot	Schedule							
V1	B0	W_1	L6	Time	4.0	6.0	6.5	7.0	9.0	9.5	
				Place	M1	M3	M3	M3	M5	M5	
				Type	-	M	L	W	M	U	
	B1	W_L	L	Time	0.5	2.5	3.0	4.0	6.0	6.5	7.0
				Place	M5	M0	M0	M1	M3	M3	M3
				Type	-	M	L	M	M	W	U

From the above cases (i) and (ii)

$$R_{M3} = \min(12.5, 15.5) = 12.5$$

$$R_{CM} = \min(R_{M2}, R_{M3}) = \min(13.0, 12.5) = 12.5 = R_{M3}$$

Thus destination candidate $CM = M3$

$$ADT = TR_{SK} + (1/2)TR_{NK} + TR_{KD} - TR_{SD} + UT + LT$$

$$= 1.0 + 1.5 + 3.0 + 0.5 + 0.5 = 3.5$$

$$12.5 - 12.0 < 3.5$$

Therefore the destination T of lot L should be $M3$ and wait at the destination after arrival. At this time,

$$TC_{3L} = 12.0, LDT = 0.5.$$

4. Conclusion

This paper presents a procedure for dispatching carriers of wafers considering the status information of transporters in the semiconductor production lines where the same types of machines performing similar functions are grouped in the bays. In particular, to dispatch the carriers of wafers, this paper presents an Unload Request Logic (URL), which determines a destination machine of the carrier for the next step operation when the carrier finishes its processing, and a Load Request Logic (LRL), which determines a carrier by a buffer for the next processing when the buffer becomes available after a carrier leaves the buffer. The procedure was to propose an efficient method from the perspective of a full production system in the URL and LRL considering the status of the transporters capable of multi-loading. The procedure determines the destination machine and the carrier to process next considering the possible lot delay time when the transporter arrives at the destination. When there is no available buffer space at the machine tool, the procedure allows carriers to stay at the current buffer and determines the delay time, which is used to determine the destination in URL.

There will be the future of research in the development of more sophisticated logic that can be applied to the next generation 450mm semiconductor line and development of the integrated approach to the upper layer scheduling module.

5. References

1. Akcali E, Uzsoy R. A sequential solution methodology for capacity allocation and lot scheduling problems for photolithography. Twenty-Sixth IEEE/CPMT International Electronics Manufacturing Technology Symposium; 2000. p. 374–81.
2. Chand S, Traub R, Uzsoy R. Rolling horizon procedures for the single machine deterministic total completion time scheduling problem with release dates. *Annals of Operations Research*. 1997; 70:115–25.
3. Chung J, Jang J. The WIP balancing procedure increasing throughput for semiconductor fabrication. *IEEE Transactions on Semiconductor Manufacturing*. 2009; 22(3):381–90.
4. Glassey C, Resende MGC. Closed-loop job release control for VLSI circuit manufacturing. *IEEE Transactions on Semiconductor Manufacturing*. 1988; 1(1):36–46.
5. Jang J, Suh J, Ferreira P. An AGV routing policy reflecting the current and future state of semiconductor and LCD production lines. *International Journal of Production Research*. 2001; 39(17):3901–21.
6. Jang J, Suh J, Liu CR. A look-ahead routing procedure for machine selection in a highly informative manufacturing system. *International Journal of Flexible Manufacturing Systems*. 2001; 13(3):287–308.
7. Koo P, Jang J, Suh J. Vehicle dispatching for highly loaded semiconductor production considering bottleneck machines first. *International Journal of Flexible Manufacturing Systems*. 2005; 17(1):23–38.
8. Lee Y, Park J, Kim S. Experimental study on input and bottleneck scheduling for a semiconductor fabrication line. *IIE transactions*. 2002; 34:179–90.
9. Li L, Sun ZJ, Zhou MC, Qiao F. Adaptive dispatching rule for semiconductor wafer fabrication facility. *IEEE Transactions on Science and Engineering*. 2013; 10(2):354–64.
10. Liao DY, Chang SC, Pei KW, Chang CM. Daily scheduling for R&D semiconductor fabrication. *IEEE transactions on Semiconductor Manufacturing*. 1996; 9(4):550–61.
11. Lou SXC, Kager PW. A robust production control policy for VLSI wafer fabrication. *IEEE Transactions on Semiconductor Manufacturing*. 1989; 2(4):159–64.
12. Lu SCH, Ramaswamy D, Kumar PR. Efficient scheduling policies to reduce mean and variance of cycle-time in semiconductor manufacturing plants. *IEEE Transactions on Semiconductor Manufacturing*. 1994; 7(3):374–88.
13. Pai PF, Lee CE, Su TH. A daily production model for wafer fabrication. *International Journal of Advanced Manufacturing Technology*. 2004; 23:58–63.
14. Shen Y, Leachman RC. Stochastic wafer fabrication scheduling. *IEEE Transactions on Semiconductor Manufacturing*. 2003; 16(1):2–14.
15. Suh J, Jang J, Koo PH. Development of a look-ahead AGV controller for a clean bay operation. *International Journal of Industrial Engineering*. 2003; 10(4):547–54.
16. Tirkel I. Forecasting flow time in semiconductor manufacturing using knowledge discovery in databases. *International Journal of Production Research*. 2013; 51(18):5536–48.
17. Uzsoy R, Lee CY, Martin-Vega LA. A review of production planning and scheduling models in the semiconductor industry part I: System characteristics, performance evaluation and production planning. *IIE Transactions*. 1992; 24(4):47–60.
18. Uzsoy R, Lee C, Martin-Vega LA. A review of production planning and scheduling models in the semiconductor industry part II: Shop-floor control. *IIE transactions*. 1994; 26(5):44–55.
19. Wein LM. Scheduling semiconductor wafer fabrication. *IEEE Transactions on Semiconductor Manufacturing*. 1988; 1(3):115–30.