

# Design of Multi-Segment Hybrid Type Content Addressable Memory in High Performance FinFET Technology

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## Abstract

Power dissipation due to memories has become a major concern of modern digital design. Scaling of CMOS technology has lead to short channel effects. Here CAM cells are designed using FinFET which have better gate control over drain to source current. The CAM cells designed with 30nm LG are used in multi-segment hybrid CAM architecture. The results are compared with the original hybrid CAM. It is observed that the energy metric of proposed architecture is 7% less compared to hybrid CAM.

**Keywords:** Content-Addressable Memory (CAM), FinFET, Hybrid-Type CAM

## 1. Introduction

In Content Addressable Memory (CAM), the input is associated with the data stored in the memory and output is the location where the content is stored. CAM can be used as a search engine for finding the matched contents in a database or a table. In CAM applications where more than one word may match, a priority encoder is used<sup>1</sup>. Internet is a combination of routers and switches. Packets are sent from source to destination with the help of router. The task of a router is to connect multiple networks and compare the destination address of packets such that the packet reaches proper destination. Routers use lookup operation which demands fast search operation thus lookup can be implemented using CAM. But there is tradeoff among the speed of CAM, silicon area and power consumption<sup>2</sup>. ICs use a few percentage of world's electricity today but power per chip is growing. If power consumption is not reduced, industry's future growth will be at risk. To achieve performance, lower power consumption and portability, CMOS devices have been scaling down for years. To control the power consumption, the supply voltage is

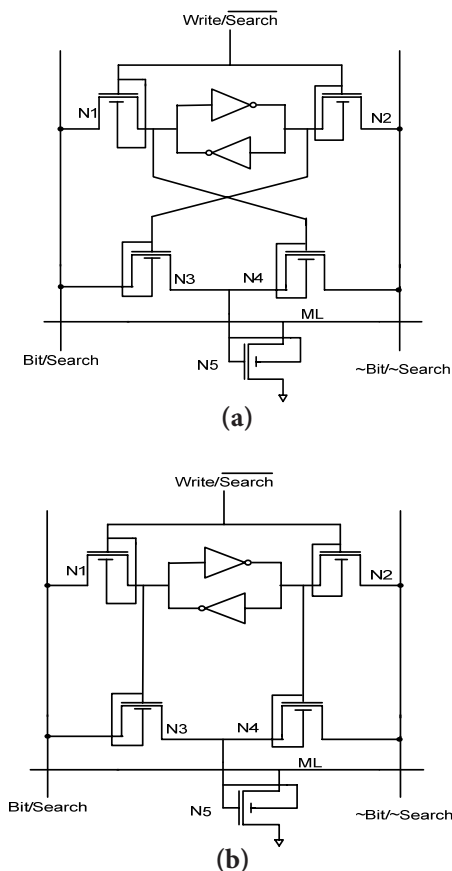
scaled down but leads to several problems such as short channel effects, drain induced barrier lowering, sub-threshold slope degradation, punch through, hot electron effect and leakage power<sup>3</sup>. Memory consumes 60–70% of the total power consumption in a chip<sup>2</sup>. Leakage power is a major concern in memories. FinFETs can enhance the drive current of MOS structures and can improve the very daunting short channel effect that affects I-V characteristics of the device<sup>4</sup>. In this paper, shorted gate FinFET is used in which the two gates are shorted together to give high current drive ( $I_{ON}$ ).

The multi-segment hybrid-type CAM was implemented in 30nm FinFET technology, the compact model used is BSIMCMG107.0.0\_20130712 (Berkeley Short-Channel IGFET Model Common Multi- Gate). Asymmetric Short Gate (ASG) FinFETs has no effect on parasitic capacitance<sup>5</sup>. The experimental results show impressive reduction in the search power consumption. The Match delay of all the design is also calculated to obtain the Energy Metric.

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## 2. Content Addressable Memory (CAM)

The CAM mainly consists of an array of memory cells. Each cell has two units, store unit and compare unit. The store unit, which uses Cross-Coupled 6T SRAM, is used for storing the bit. The compare unit made of pass transistor logic is used to compare the search bit and stored bit. The CAM cell can be of either XOR or XNOR type as shown in Figure 1. The output of compare unit is fed to gate terminal of pull-down transistor N5. Based on the output of compare unit, the transistor may turn ON or OFF. Match line is connected to the pull-down transistor. If the transistor is ON (OFF), the match line discharges (charges)<sup>2</sup>. Conventionally, there are two types of CAM designs: NOR type and NAND type. In any CAM design, there are two phases precharge and evaluation. In precharge phase, the match line is charged to high voltage level and in evaluation phase, the data in store unit and compare unit are compared.



**Figure 1.** Typical CAM Cell. (a) XOR type. (b) XNOR type.

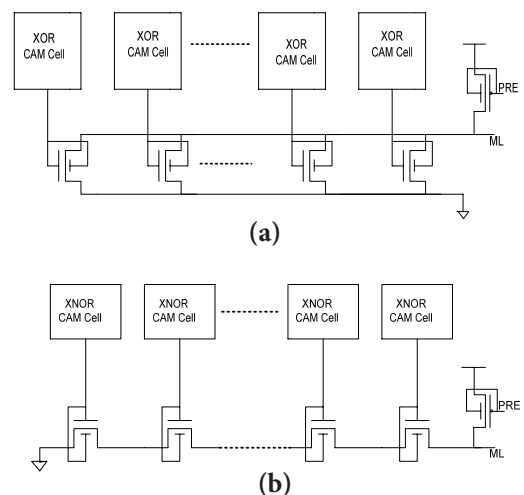
### 2.1 NOR Type CAM Array

The NOR type CAM array design<sup>5</sup> uses XOR type CAM cell. XOR CAM cell uses XOR logic in compare unit. Typical XOR CAM is shown the Figure 1(a) and the working is as follows: Initially the Match Line (ML) is at high voltage level. When Write Line (WL) is high, the transistors N1 and N2 are ON. The data on bit and ~bit lines will be stored in store unit via cross-coupled inverter pair. When WL is low (search), N1 and N2 are OFF and the compare unit compares the stored data with the data on search lines.

If the data matches, the output of compare unit is low which makes the transistor N5 to continue in OFF state. Therefore when there is a match, the match line retains at high voltage. When there is mismatch, transistor N5 is forced to ON by the compare unit which creates a path to discharge the match line.

In NOR type CAM array design, the pull-down transistors are arranged as NOR gate i.e. in parallel as shown in Figure 2(a). In precharge phase, the match line is charged to high voltage level and bits will be stored in store unit since WL is high. In evaluation phase, the stored bits in each CAM cell are compared with the bits on corresponding bit lines. If there is a mismatch in any of the CAM cells, match line discharges through that particular pull-down transistor. Hence the parallel NOR type CAM is faster. Search delay for NOR type CAM is given below, where  $t_{XOR}$ ,  $t_{Transistor}$  and  $t_{line}$  are XOR, transistor and matchline delay respectively. Where  $n$  is word length.

$$t_{NOR} = t_{XOR} + t_{Transistor} (n-1) t_{line}$$



**Figure 2.** Traditional CAM design. (a) NOR-Type CAM Array. (b) NAND-Type CAM Array.

## 2.2 NAND Type CAM Array

The NAND type CAM array design<sup>5</sup> uses XNOR type CAM cell. XNOR CAM cell uses XNOR logic in compare unit. Typical XNOR CAM is shown the Figure 1(b) and the working is as follows: Initially the Match Line (ML) is at high voltage level. When Write Line (WL) is high, the transistors N1 and N2 are ON. The data on bit and  $\sim$ bit lines will be stored in store unit via cross-coupled inverter pair. When WL is low (search), N1 and N2 are OFF and the compare unit compares the stored data with the data on search lines. If the data matches, the output of compare unit is high which makes the transistor N5 to turn ON. This creates a path for the match line to discharge. Therefore when there is a match, the match line discharges. When there is a mismatch, compare unit gives a low output, which makes the transistor N5 to turn OFF. Therefore, match line retains high level.

In NAND type CAM design, the pull-down transistors are arranged as NAND gate i.e. in series as shown in Figure 2(b). In precharge phase, the match line is charged to high voltage level and bits will be stored in the store unit since WL is high.

In evaluation phase, the stored bits in each CAM cell are compared with the bits on the corresponding search line. The match line discharges only when all the CAM cells have a match. Hence the series NAND type CAM is slower. Search delay for NAND type CAM is given below, where  $t_{\text{XNOR}}$ ,  $t_{\text{Transistor}}$  and  $t_{\text{line}}$  are XNOR, transistor and matchline delay respectively. Where  $n$  is word length.

$$t_{\text{NAND}} = t_{\text{XNOR}} + n(t_{\text{Transistor}} + t_{\text{line}})$$

## 3. Multi-Segment Hybrid Type CAM Design

### 3.1 Overview

In the above Hybrid CAM design<sup>6</sup> as shown in Figure 3, if the length of SEG\_1 is too long, the charge sharing problem would increase more. The search operation would consume more power if the SEG\_1 length is decreased. Length SEG\_1 is defined by optimization between power of NAND and NOR CAM<sup>6</sup>. Thus we have followed<sup>6</sup> in choosing SEG\_1 length. The NOR CAM cells consist of 26-bits, the drain of pull down transistor is connected with the common pre charge line. Since the PRE signal keeps ML2 high via P2 in precharge phase. The large line capacitance of ML2 consumes more power. Therefore to cut down the power consumption the Multi-Segment Hybrid type CAM is proposed.

The Multi-Segment Hybrid CAM design is shown in Figure 4 mainly focuses on the advantage of power efficiency of the NAND part of the hybrid CAM architecture. Here the CAM word is divided into three segments i.e. SEG\_1, SEG\_2 and SEG\_3. The SEG\_1 and SEG\_3 are NAND type CAM design in which the pull-down transistors are arranged in NAND type as shown in Figure 4, if there is match in all the XNOR CAM cells only then the pull-down transistor will discharge to 0 else will remain 1, where as SEG\_2 is NOR type CAM design in which the pull-down transistors are arranged in NOR type, if there is mismatch in any of the CAM cell the pull-down transistor will discharge to 0, else it will remain to 1. The CAM word is matched when the SEG\_1, SEG\_2 and SEG\_3 all are in matched condition and only then the match line will go to low.

### 3.2 Search Operation

The search operation is performed in two phases i.e. the ML precharge and the ML evaluation. In ML precharge phase, match line is charged to high and then in ML evaluation phase based on the match and mismatch of the words the match line will change the logic from high to low or low to high.

#### 3.2.1 ML Precharge Phase

In Figure4 during the precharge phase, the PRE signal is low. Match Line (ML) is charged to high through P3. In

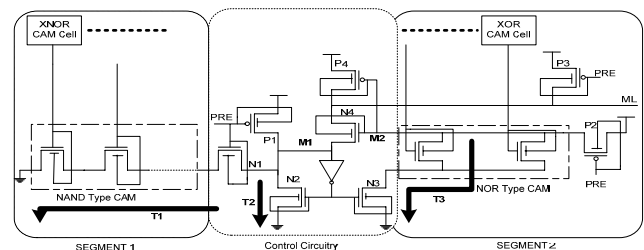


Figure 3. Existing hybrid CAM design.

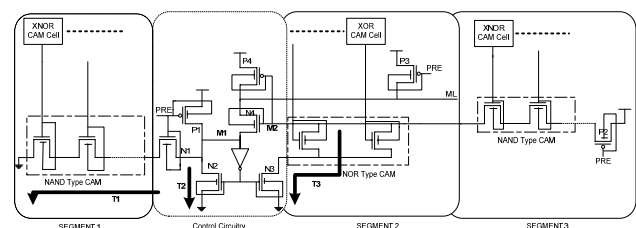


Figure 4. Proposed multi-segment hybrid CAM design.

the Figure4, T1, T2 and T3 are the pull-down paths in the circuit. The M1 node is at high because of transistor P1, which drives the transistors N2 and N3 OFF due to which the path T2 and T3 are disconnected from ground. The low PRE signal turns OFF transistor N1. Therefore all the pull-down paths are disconnected.

### 3.2.2 ML Evaluation Phase

In the evaluation phase, the PRE signal is high and the search bits are loaded on bit lines. In this paper, the CAM is divided into three segments SEGMENT-1 (SEG\_1), SEGMENT-2 (SEG\_2) and SEGMENT-3 (SEG\_3) as shown in the Figure 4. When all the three segments have match, then match line will discharge through any one of the pull-down paths. Since there are three segments, there can be eight possible cases as shown in the Table 1. Based on the voltage level on key node we are grouping these eight cases into four groups as follows:

#### 3.2.2.1 Group 1

It consists of case 1 and case 2 in which SEG\_1 and SEG\_3 has mismatch, SEG\_2 has mismatch or match.

When SEG\_1 and SEG\_3 have a mismatch, any one (or more than one of the transistors) is OFF which makes the pull-down path T1 to disconnect from ground. The node M1 will remain at high, which in turn keeps the transistors N2 and N3 OFF. Therefore, the pull-down paths T2 and T3 are disconnected from ground. Since T3 path is disconnected from the ground, the match or mismatch in SEG\_2 (NOR type) will not affect the output. Therefore, Match Line (ML) remains at logic high.

#### 3.2.2.2 Group 2

It consists of case 3 and case 4 in which SEG\_1 has mismatch, SEG\_2 has match or mismatch and SEG\_3 has match.

When SEG\_1 has a mismatch, any one (or more than one of the transistors) is OFF which makes the pull-down path T1 to disconnect from ground. The node M1 will remain at high, which in turn keeps the transistors N2 and N3 OFF. So, path T3 is disconnected from the ground, the match or mismatch in SEG\_2 (NOR type) will not affect the output. SEG\_3 has a match, all the pull-down transistors of NAND type in SEG\_3 are ON, the node M2 will be high turning transistor N4 ON. Since M1 is high the match line remains at logic high.

#### 3.2.2.3 Group 3

It consists of case 5, case 6 and case 7 in which SEG\_1 has match, SEG\_2 and SEG\_3 has match or mismatch.

1. When SEG\_1 has a match, all the pull-down transistors of NAND type are ON, which connects the path T1 to ground. The node M1 discharges via path T1. When there is a mismatch in SEG\_2, any one of the pull-down transistors is ON, connecting the T3 path to ground. The node M2 remains at low. Since T3 path is connected to the ground, the match or mismatch in SEG\_3 (NAND type) will not affect the output. Therefore, Match Line (ML) remains at logic high.
2. When SEG\_1 and SEG\_2 have a match, all the pull-down transistors of NAND type in SEG\_1 are ON, which connects the T1 path to ground. The node

**Table 1.** Key node Voltage High/Low (H/L) and Path Connected/Disconnected (O/X) for each case in the proposed hybrid-type CAM design

|        | SEG_1    | SEG_2    | SEG_3    | Path |    |    | Key Nodes |    |    | Result   |
|--------|----------|----------|----------|------|----|----|-----------|----|----|----------|
|        |          |          |          | T1   | T2 | T3 | M1        | M2 | ML |          |
| Case 1 | mismatch | mismatch | Mismatch | X    | X  | X  | H         | L  | H  | mismatch |
| Case 2 | mismatch | match    | Mismatch | X    | X  | X  | H         | L  | H  | mismatch |
| Case 3 | mismatch | mismatch | Match    | X    | X  | X  | H         | H  | H  | mismatch |
| Case 4 | mismatch | match    | Match    | X    | X  | X  | H         | H  | H  | mismatch |
| Case 5 | match    | mismatch | Mismatch | O    | O  | O  | L         | L  | H  | mismatch |
| Case 6 | match    | mismatch | Match    | O    | O  | O  | L         | L  | H  | mismatch |
| Case 7 | match    | match    | Mismatch | O    | O  | X  | L         | L  | H  | mismatch |
| Case 8 | match    | match    | Match    | O    | O  | X  | L         | H  | L  | match    |

M1 discharges via T1 path. When there is a match in SEG\_2, all the pull-down transistors in NOR type are OFF and SEG\_3 is mismatch the pull-down transistors are OFF. The node M2 will remain at low. Therefore, the match line remains at logic high.

#### 3.2.2.4 Group 4

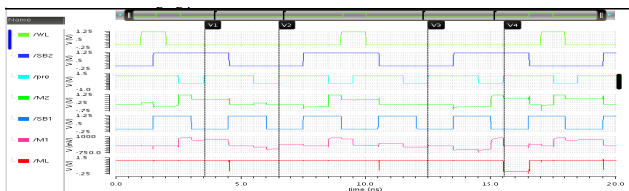
It consists of only case 8 in which SEG\_1, SEG\_2 and SEG\_3 all have a match.

When SEG\_1 and SEG\_3 have a match, all the pull-down transistors of NAND type in SEG\_1 are ON, which connects the T1 path to ground. The node M1 discharges via T1 path. When there is a match in SEG\_2, all the pull-down transistors in NOR type is OFF and M2 charges to high. The transistor N4 turns ON, which creates a discharging path for match line.

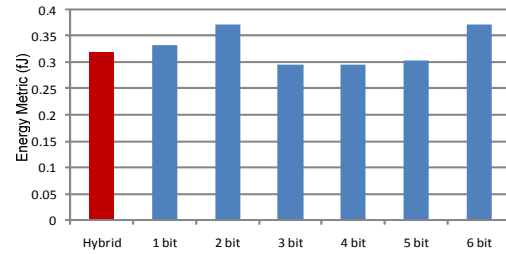
Therefore, when all the three segments are matched, the match line discharges from high to low.

## 4. Simulation Result

Simulation is done in Cadence Virtuoso platform. The Multi-Segment Hybrid-type CAM was implemented in 30nm FinFET Technology; the compact model used is BSIMCMG107.0.0\_20130712 (Berkeley Short-Channel IGFET Model Common Multi-Gate)<sup>3</sup>. To obtain the energy metric we need to calculate the search power consumption and match delay. The average current is taken by calculating the average of currents at each and every CAM cell. The search power consumption is calculated by multiplying the average current and supply voltage. The search delay is calculated by calculating the delay between the rising edge of the precharge and the falling edge of the match line where the matching has occurred. The energy metric is calculated by multiplying the search power consumption and match delay. The Multi-Segment Hybrid CAM has 12-bit NAND and 20-bit NOR Type CAM array.



**Figure 5.** Simulation result of the proposed Multi-Segment Hybrid CAM.



**Figure 6.** Energy metric of proposed CAM for different number of bits in SEG\_3.

**Table 2.** Performance metric of proposed and hybrid CAM design

|                      | Delay (ps)   | Power(mW)     | Energy Metric (fJ/bit/search) |
|----------------------|--------------|---------------|-------------------------------|
| <b>Hybrid CAM</b>    | 3.989        | 0.0798        | 0.3183                        |
| SEG_3 (6-bit)        | 4.848        | 0.0770        | 0.3732                        |
| SEG_3 (5-bit)        | 3.947        | 0.0769        | 0.3035                        |
| SEG_3 (4-bit)        | 3.899        | 0.0758        | 0.2958                        |
| <b>SEG_3 (3-bit)</b> | <b>3.947</b> | <b>0.0749</b> | <b>0.2956</b>                 |
| SEG_3 (2-bit)        | 4.968        | 0.0750        | 0.3723                        |
| SEG_3 (1-bit)        | 4.461        | 0.0745        | 0.3324                        |

The SEG\_3 is simulated for 1-bit to 6-bit and the experimental result is compared with the existing hybrid CAM also implemented with 30nm FinFET Technology. In the above simulation diagram the vertical lines shown represent the output of the corresponding groups i.e. V1 represent group 1 output, V2 represent group 2 output, V3 represent group 3 output and , V4 represent group 4 output. Table 2 shows the comparison result in term of delay power and energy metric.

## 5. Conclusion

In this paper, we have presented a Multi-Segment Hybrid CAM Design in FinFET Technology which can reduce the power consumption in the match line. The SEG\_3 is more efficient when 3-bit NAND Type CAM is used.

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