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Low Power CMOS Look-Up Tables using PROM

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Abstract

Field Programmable Gate Array (FPGA) based designs are the most popular trend towards semiconductor technology evolution. The important subsystem in a configurable logic block is a Look-Up Table (LUT) in the FPGA chip. If the power reduction techniques are implemented in the LUTs, there would be an overall very less power while implementing the design in FPGAs. This study mainly focuses on designing LUTs using Programmable Read Only Memory (PROM) circuits. To implement these LUTs, half adder, full adder, half subtract and full subtractor circuits are chosen with PROM concept. Both the conventional CMOS and pseudo-nMOS style architectures are built for the LUTs. Pseudo-nMOS based LUTs are offering less area and low power compared with conventional CMOS approach. A pseudo-nMOS based full adder LUT design produce 564.5 μm^2 layout area, which is less compared with 765.5 μm^2 produced by conventional CMOS full adder LUT. A pseudo-nMOS based full subtractor design produce 1.119 µW dynamic power dissipation, which is less compared with 3.905 µW produced by conventional CMOS full subtractor. Also the design cycle time for FPGAs are much less compared with ASICs. Simulation results are verified using Microwind and Digital Schematic (DSCH) Electronic Computer Aided (CAD) design tools with BSIM4 MOSFET model in 60 nm technology. This study conveys that how the Programmable Read Only Memory (PROM) can act as a Look-Up Table (LUT) within a FPGA architecture. Since engineers are designing the circuits with most care with circuit design, layout design, etc., Application Specific Integrated Circuits (ASIC) are the best at providing low power, high speed and low size at the cost of design cycle time. But with the current semiconductor technology growth, even FPGAs are being manufactured with high speed with more versatile functionalities.

Keywords: CMOS, FPGA, Look-Up Table, Microwind, PROM, Pseudo-nMOS

1. Introduction

According to Moore's law, the number of transistors become double once in eighteen months approximately. So the power dissipation in a system will be huge and the reliability may come down. So designers are still working towards better designs which will consume less power at the cost of performance or area[1]. A costly cooling mechanism requirement is another reason for low power designs. By modifying circuits in a system or sub-systems one may achieve low power dissipation. Same is not applicable to the batteries, since the battery technology is not developed as like semiconductor. Due to the explosive in nature, designers are always concentrating to design novel circuits for better results[2,3].

FPGAs are most popular and widely used semiconductor chips in industries. ASICs are performing good since the engineers start the designs from the scratch by considering all the optimization parameters like power, speed and area. But the design life cycle time is too high along with more costly CAD tools. FPGAs overcome these drawbacks and even provide better performance with current semiconductor technology trend.

This study is about the implementation of LUTs using PROM with adder circuit examples. To perform and verify the designs adders/subtractor circuits are considered. LUT can also being designed with switches like transmission gates, pass transistors and multiplexers. Pseudo-nMOS and conventional CMOS styles are used for the implementation. Here the ratioed logic like the

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pseudo-nMOS is used to reduce the area at the cost of performance. A conventional CMOS which is a ratio-less logic consumes more number of transistors in turn area. Other forms of CMOS logic styles like dynamic logic, domino logic, complementary pass-transistor, and transmission gate are also can be used for better results. More specifically for adders, a mirror circuit concept may also be implemented to produce equal rise and fall delay.

This study analyzes the adder circuit implementations using LUT design with pseudo-nMOS logic style approach. Results show that the proposed circuits are better as compared to the conventional approach in terms of power and area. This work further can be extended using dynamic and domino logic styles. Also FPGA interconnects will be designed to reduce the overall power dissipation further[4,5].

2. Adder Look-Up Table Circuits

We implement both adders and subtractors using PROM which can act as a LUTs[6]. Generally, FPGA may have many such LUTs to implement the function given by the designer. It may contain 3 inputs and 1 output is referred as 3LUT and 4 inputs and 1 output is referred as 4LUT. For example, let us analyze the usage of 4LUT for the following logic functions:

F = x
F = wxyz
F = w'x'y'z + w'xyz' + w'x'y'z' + w'x'yz
F = w + x + y + z
F = (w + x + y + z) (w' + x' + y' + z')

2.1 Half Adder LUT Designs

Figure 1. shows that the implementation of half adder using Programmable Read-Only Memory (PROM) with Pseudo-nMOS style of approach. The channel length of the pMOS transistors in the pull-up network are made with three times larger than the pull-down network transistors to reduce the speed. Since the gate of these pMOS transistors are connected to the ground, they are always in ON state. To do the necessary function, these transistors are weaker compared to the nMOS pull-down network. This is designed with the DSCH design tool and then converted to Verilog Hardware Description Language (HDL) as shown in Figure 2 using the default 0.12 µm technology foundry[7,8].

This Verilog code can be compiled with the Microwind design tool and the layout is generated as shown in Figure

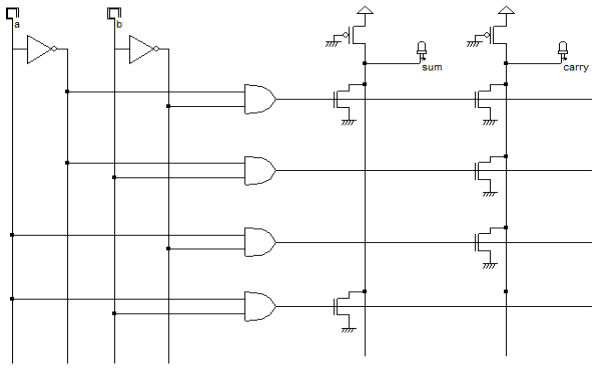

Figure 1. Half adder PROM circuit.

3. Microwind is a layout editor tool is used to draw a layout for the design. A simulation can also be done on the layout to check the functional verification.

```
module half_adder_prom(b,a,sum,carry);
input b,a;
output sum,carry;
not #(17) inv(w2,b);
not #(17) inv(w4,a);
and #(23) and2(w5,w2,w4);
and #(16) and2(w6,b,w4);
and #(16) and2(w7,w2,a);
and #(16) and2(w8,b,a);
pmos #(24) pmos(sum,vdd,vss); // 2.0u 0.12u
nmos #(24) nmos(sum,vss,w5); // 1.0u 0.12u
nmos #(24) nmos(sum,vss,w8); // 1.0u 0.12u
pmos #(31) pmos(carry,vdd,vss); // 2.0u 0.12u
nmos #(31) nmos(carry,vss,w5); // 1.0u 0.12u
nmos #(31) nmos(carry,vss,w6); // 1.0u 0.12u
nmos #(31) nmos(carry,vss,w7); // 1.0u 0.12u
endmodule
```

Figure 2. Half adder PROM - Verilog HDL list.

This Verilog code can be compiled with the Microwind design tool and the layout is generated as shown in Figure 3. Microwind is a layout editor tool is used to draw a layout for the design. A simulation can also be done on the layout to check the functional verification.

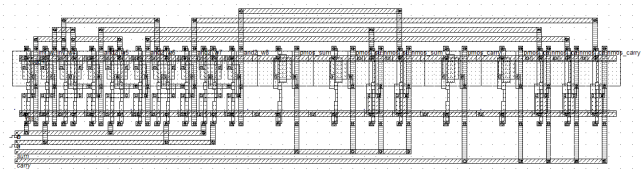

Figure 3. Layout of half adder PROM.

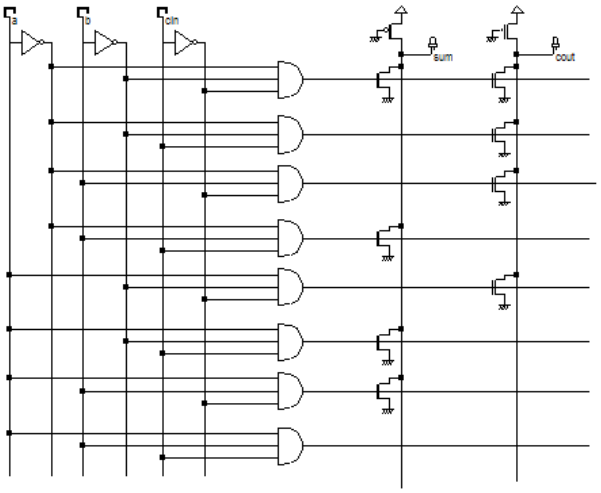

Figure 4. Full adder PROM circuit.

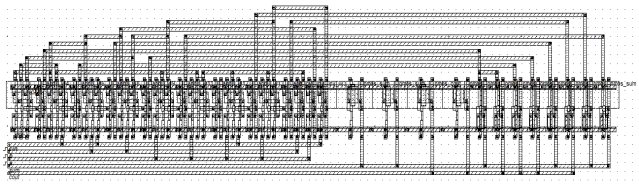

Figure 5. Layout of full adder PROM.

2.2 Full Adder LUT Designs

Similarly the full adder circuits are being implemented by expanding the 2-to-4 decoder to 3-to-8 decoder[2,9]. Figure 4 and 5 shows that the full adder Pseudo-nMOS schematic and layout respectively.

3. Subtractor Look-Up Table Circuits

Similar to adders, half and full subtractor circuits are implemented using PROM concept[10]. Adders and subtractors play a crucial role in computing applications. This kind of Filed-Effect Transistors (FET) programmable array are the most powerful in the aspect of area. Due to the pseudo-nMOS logic, the number of transistors are reduced almost half count compared to the conventional logic style.

3.1 Half Subtractor and Full Subtractor LUT designs

Figure 6. shows that the implementation of half subtractor using Programmable Read-Only Memory (PROM) with pseudo-nMOS style of approach. Psuedo-nMOS logic style has the main advantage of having less number of

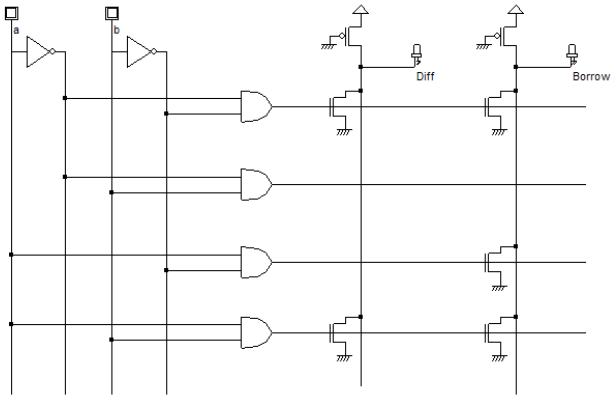

Figure 6. Half subtractor PROM circuit.

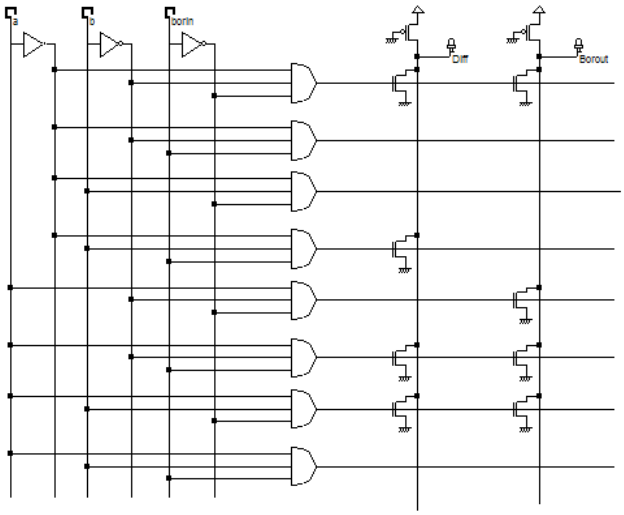

Figure 7. Full subtractor PROM circuit.

transistors to perform the required function as compared with static CMOS style. For example, N input logic gate requires 2N number of transistors while in the pseudo-nMOS only N+1 transistors are required. Mainly these kind of designs are more suitable with memory circuits since they occupy the large portion the size in the chip area. Since there is more demand on data storage part, engineers work towards efficient designs which will consume less area at the cost of little performance loss.

Figure 7. shows the schematic of full subtractor using pseudo-nMOS logic style. Figure 8 shows the verilog code generated with full subtractor using DSCH design tool.

```
module full_subtractor(borin,a,b,Diff,Bout);
input borin,a,b;
output Diff,Bout;
or #(13) or3(w4,w1,w2,w3);
```

```
not #(31) inv(w6,borin);
not #(31) inv(w8,a);
not #(31) inv(w10,b);
and #(16) and3(w1,a,w10,w6);
and #(9) and3(w11,a,w10,borin);
and #(23) and3(w12,a,b,borin);
and #(9) and3(w13,a,b,w6);
and #(23) and3(w2,w8,b,w6);
and #(16) and3(w14,w8,b,borin);
and #(23) and3(w3,w8,w10,borin);
and #(9) and3(w15,w8,w10,w6);
or #(16) or2(Diff,w12,w4);
or #(13) or3(w17,w14,w2,w3);
or #(16) or2(Bout,w12,w17);
endmodule
```

Figure 8. Full subtractor PROM - Verilog HDL list.

Figures 9. and 10. shows the generated layout diagrams of half subtractor and full subtractor respectively with the help of Microwind layout design tool.

3.2 Functional Verification

A functional verification can be done using DSCH schematic design tool for all the circuits. For example, simulation results of only full subtractor are presented in Figure 11.

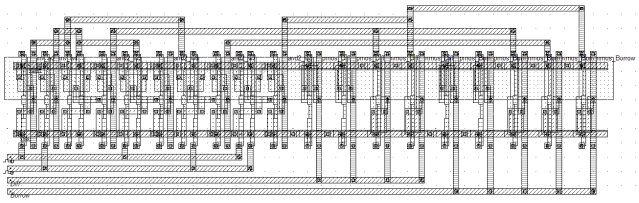

Figure 9. Layout of half subtractor PROM circuit.

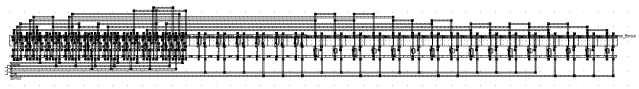

Figure 10. Layout of full subtractor PROM circuit.

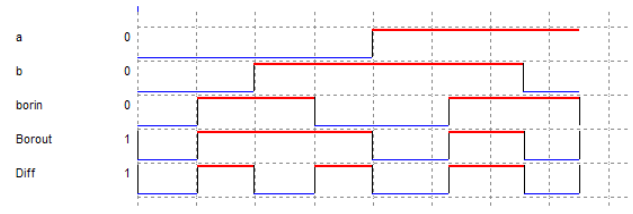

Figure 11. Full subtractor timing diagrams.

4. Simulation Results

All the above circuits are being implemented using DSCH schematic tool to verify the functionality and to generate Verilog HDL code. The Microwind layout editor tool is used to compile the Verilog HDL code and to generate the layout for the design. A functional verification can be done even on the layout to recheck again. This Microwind tool can act as a Design Rule Checker (DRC) for the layout to avoid any layout rule violation. All simulation results are obtained with default technology foundry of 0.12 µm, 6 Metal process and 1.2 V power supply voltage at 27°C. Also 90 nm, 60 nm and 50 nm process technology results are obtained with 1.0 V, 1.0 V and 0.5 V respectively.

Table 1. and 2. shows that the layout results of all PROM circuits using conventional CMOS style and pseudo-nMOS approach respectively. Tables 3 and 4 shows that the average power dissipation of all PROM circuits using conventional CMOS style and pseudo-nMOS style respectively. It conveys the pseudo-nMOS based PROM circuits consume low power dissipation. For example, pseudo-nMOS PROM full adder offers 13.790 µW where as traditional full adder consumes 18.123 µW. A pseudo-nMOS full subtractor consumes 14.516 µW where as conventional full subtractor dissipates 19.716 µW.

Table 1. Conventional CMOS PROM – layout results

Circuits	No. of NMOS transistors	No. of PMOS transistors	Layout Area (μm^2)
Half adder PROM	20	20	146.2
Half subtractor PROM	20	20	242.7
Full adder PROM	49	49	765.5
Full subtractor PROM	49	49	765.5

Table 2. Pseudo-nMOS PROM circuits - layout results

Circuits	No. of NMOS transistors	No. of PMOS transistors	Layout Area (μm^2)
Half adder PROM	19	16	202.4
Half subtractor PROM	19	16	202.4
Full adder PROM	43	38	564.5
Full subtractor PROM	51	41	627.4

Table 3. Average power dissipation (μw)

Conventional CMOS PROM circuits	120 nm	90 nm	60 nm	50 nm
Half adder	18.25	7.79	6.67	5.78
Half subtractor	18.0	7.23	6.23	4.44
Full adder	18.123	11.907	9.235	4.985
Full subtractor	19.716	14.084	10.804	3.905

Table 4. Average power dissipation (μw)

Pseudo-nMOS PROM circuits	120 nm	90 nm	60 nm	50 nm
Half adder	9.797	5.643	5.050	0.736
Half subtractor	5.702	3.527	2.784	0.473
Full adder	13.790	8.465	6.249	1.062
Full subtractor	14.516	9.046	6.633	1.119

5. Conclusions/Future Work

The three important VLSI design optimization parameters are the power, area and speed with any kind of system. Some circuits may perform with good speed at the cost of more power and some circuits may dissipate less power at the cost of area. Depends on the application the optimization can be achieved for a better trade-off.

This work further can be extended to construct LUTs using multiplexers and transmission gates with low power. Also different routing programmable switch circuits may also be considered to reduce the overall power dissipation of a FPGA chip. This study can be further tested with different benchmark circuits apart from adders and subtractors. FPGA parts like embedded Random Access Memory (RAM) and multipliers will also be designed with novel ideas to reduce the overall power dissipation. A low power SRAM architectures with efficient LUT designs will help to reduce the overall power dissipation in FPGA chips.

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