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Thermally Aware LVCMOS based Low Power Universal Asynchronous Receiver Transmitter Design on FPGA

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Abstract

Green communication is the latest research trend practiced by researcher in green computing and network communication. There is no extensive work in green UART design. In order to fill this research gap, we are going to design LVCMOS based energy efficient Universal Asynchronous Receiver Transmitter (UART) that will create an avenue for IO standards based green communication. UART (Universal Asynchronous Receiver Transmitter) is a kind of serial communication protocol; mostly used for short-distance low speed, low-cost data exchange between computer and peripherals. Various energy efficient techniques have been applied to the design along with the change in IO standards. It has been concluded that there occurs 97.65% reduction in clock power, 75.14% reduction in I/O power, 7.19% reduction in leakage power, 17.37% reduction in junction temperature, and 71.12% reduction in total power dissipation in case SSTL2_II IO/standard, thus it is considered to be most energy and power efficient IO standard to be used in the future.

Keywords: Energy Efficient, FPGA, LFM, LVCMOS, Thermal Aware, UART

1. Introduction

As shown in Figure 1, A which is sender at one time will behave like receiver at other time and B will also behaves like sender and receiver both, but at a time they can be either sender or receiver not both.

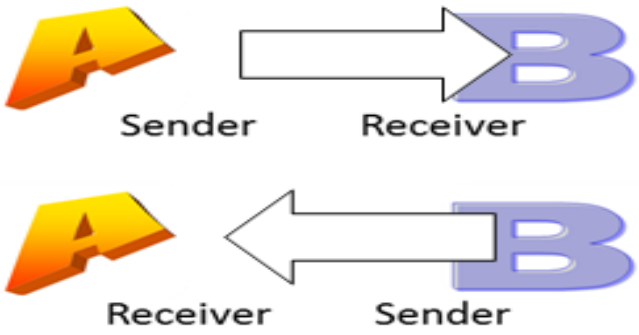

Figure 1. Anatomy of Communication.

So, we require 2 transmitters and 2 receivers in the communication between A and B as shown in Figure 1. So we can think of replacing four network devices with only two UARTs (Universal Asynchronous Receiver and Transmitter). UART has two clock signals. It will acts as either receiver or transmitter at once[1] it will act as receiver when receiver clock is high and act as transmitter when transmitter clock is high. Despite multiple usability in multiple domain of research, there is no extensive work in low power UART design. Low power UART is designed with asynchronous techniques and output load capacitance[2,3]. There is research gap in UART design. There is no LVCMOS IO Standard based UART design yet[5,6] UART design. In this work, thermally aware[9] and LVCMOS IO standard based energy efficient design is going to be designed[7]. LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor): LVCMOS

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is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC[8] the LVCMOS standards supported in Virtex-6 FPGAs are: LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33[8]. Frequency Scaling is the technique in which we vary the operating frequency of the device and then change in total power consumption is being analyzed at different frequencies. Energy efficiency can also be achieved by applying another energy efficient techniques such as clock gating, changing the output load, temperature and capacitance[10-12].

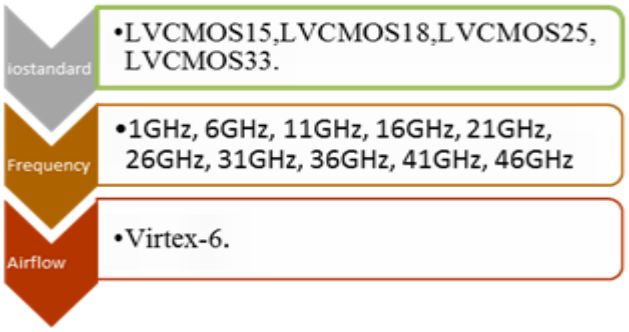

Figure 2. Parameters in Energy Efficient LVCMOS Based UART Design.

2. Power Analysis

2.1 When the Device is being Operated at is LVCMOS15 IO/Standard

Table 1. Power Dissipation with LVCMOS15 I/O Standard

Frequency	Clock	IOS	Leakage	Junction Temp	Total
1 GHz	0.011	0.010	0.042	25.2	0.065
6 GHz	0.086	0.060	0.042	25.7	0.201
11 GHz	0.159	0.111	0.043	26.1	0.332
16 GHz	0.231	0.161	0.043	26.5	0.462
21 GHz	0.296	0.211	0.043	26.9	0.585
26 GHz	0.367	0.262	0.044	27.4	0.714
31 GHz	0.438	0.312	0.044	27.8	0.542
36 GHz	0.508	0.362	0.044	28.2	0.971
41 GHz	0.579	0.413	0.045	28.6	1.099
46 GHz	0.649	0.463	0.045	29.1	1.227

From above analysis it is observed that there is 98.30% reduction in clock power, 97.83% reduction in IO power, 6.67% reduction in leakage power, 13.40% reduction in junction temperature and 94.70% reduction in total power dissipation when we scale down the frequency from 46GHz to 1GHz as shown in Table 1.

2.2 When the Device is being Operated at is LVCMOS18 IO/Standard

Table 2. Power Dissipation with LVCMOS18 IO Standard

Frequency	Clock	IOS	Leakage	Junction Temp	Total
1 GHz	0.011	0.012	0.042	25.2	0.068
6 GHz	0.086	0.074	0.043	25.7	0.215
11 GHz	0.159	0.136	0.043	26.2	0.357
16 GHz	0.231	0.197	0.044	26.6	0.498
21 GHz	0.296	0.259	0.044	27.1	0.633
26 GHz	0.367	0.320	0.044	27.6	0.773
31 GHz	0.438	0.382	0.045	28.0	0.912
36 GHz	0.508	0.444	0.045	28.5	1.052
41 GHz	0.579	0.505	0.045	28.9	1.192
46 GHz	0.649	0.587	0.046	29.4	1.332

From above analysis it is observed that there is 98.30% reduction in clock power 97.95% reduction in IO power, 8.69% reduction in leakage power, 14.28% reduction in junction temperature and 94.89% reduction in total power dissipation when we scale down the frequency from 46GHz to 1GHz as shown in Table 2.

2.3 When the Device is being Operated at is LVCMOS25 IO/Standard

Table 3. Power Dissipation with LVCMOS25 IO Standard

Frequency	Clock	IOs	Leakage	Junction Temp	Total
1 GHz	0.011	0.019	0.043	25.2	0.075
6 GHz	0.086	0.115	0.044	25.8	0.256
11 GHz	0.159	0.210	0.044	264	0.432
16 GHz	0.231	0.306	0.044	27.0	0.607
21 GHz	0.296	0.401	0.045	27.6	0.776
26 GHz	0.367	0.497	0.045	28.1	0.950
31 GHz	0.438	0.592	0.046	28.7	1.124
36 GHz	0.508	0.688	0.046	29.3	1.298
41 GHz	0.579	0.783	0.047	29.9	1.417
46 GHz	0.649	0.879	0.047	30.4	1.645

From above analysis it is observed that there is 98.30% reduction in clock power,97.83% reduction in IO power, 8.51% reduction in leakage power, 17.10% reduction in junction temperature and 95.44% reduction in total power dissipation when we scale down the frequency from 46GHz to 1GHz as shown in Table 3.

2.4 When the Device is being Operated at is LVCMOS33 IO/Standard

From above analysis it is observed that there is 98.30% reduction in clock power, 97.83% reduction in IO power, 12% reduction in leakage power, 21.18% reduction in junction temperature and 95.95% reduction in total power dissipation when we scale down the frequency from 46GHz to 1GHz as shown in Table 4.

Table 4. Power Dissipation with LVCMOS33 IO Standard

Frequency	Clock	IOs	Leakage	Junction Temp	Total
1 GHz	0.011	0.030	0.044	25.3	0.087
6 GHz	0.086	0.180	0.045	26.1	0.323
11 GHz	0.159	0.331	0.045	26.8	0.554
16 GHz	0.231	0.481	0.046	27.6	0.784
21 GHz	0.296	0.632	0.046	28.3	1.008
26 GHz	0.367	0.782	0.047	29.1	1.237
31 GHz	0.438	0.933	0.048	29.8	1.466
36 GHz	0.508	1.083	0.048	30.6	1.695
41 GHz	0.579	1.233	0.049	31.4	1.924
46 GHz	0.649	1.384	0.050	32.1	2.152

3. Results

3.1 Total Power Analysis at Different Io Standards of LVCMOS Logic Family

Table 5. Total Power Dissipation at Different IOSTANDARD

Frequency	LVCMOS 15	LCMOS 18	LVCMOS 25	LVCMOS 33
1 GHz	0.065	0.068	0.075	0.087
6 GHz	0.201	0.215	0.256	0.323
11 GHz	0.332	0.357	0.432	0.554
16 GHz	0.462	0.498	0.607	0.784
21 GHz	0.585	0.633	0.776	1.008
26 GHz	0.714	0.773	0.950	1.237
31 GHz	0.542	0.912	1.124	1.466
36 GHz	0.971	1.052	1.298	1.695
41 GHz	1.099	1.192	1.417	1.924
46 GHz	1.227	1.332	1.645	2.152

When we scale down frequency from 46GHz to 1GHz as shown in Table 5, there is 94.70% reduction in total power reduction at LVCMOS15, 94.89% reduction at LVCMOS18, 95.44% reduction at LVCMOS25, 95.95% reduction at LVCMOS33.

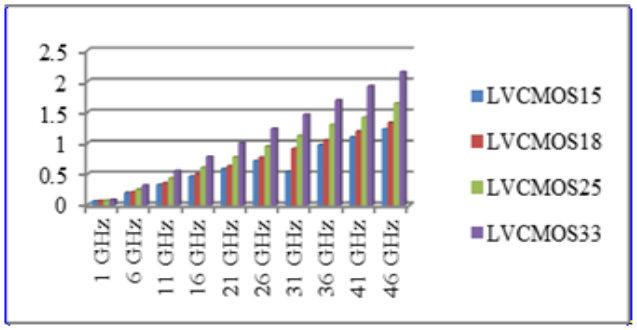

Figure 3. Total Power Dissipation of UART Using Different LVCMOS IO Standards.

3.2 Junction Temperature Analysis at Different Io Standards of LVCMOS Logic Family

Table 6. Junction Temperature at Different IO Standard

Frequency	LVCMOS 15	LVCMOS 18	LVCMOS 25	LVCMOS 33
1 GHz	25.2	25.2	25.3	25.3
6 GHz	25.7	25.7	26.1	26.1
11 GHz	26.1	26.2	26.8	26.8
16 GHz	26.5	26.6	27.6	27.6
21 GHz	26.9	27.1	28.3	28.3
26 GHz	27.4	27.6	29.1	29.1
31 GHz	27.8	28.0	29.8	29.8
36 GHz	28.2	28.5	30.6	30.6
41 GHz	28.6	28.9	31.4	31.4
46 GHz	**29.1**	**29.4**	**32.1**	**32.1**

When we scale down frequency from 46GHz to 1GHz as shown in Table 6, there is 13.40% reduction in junction temperature at LVCMOS15, 14.28% reduction at LVCMOS18, 17.10% reduction at LVCMOS25, 21.18% reduction at LVCMOS33.

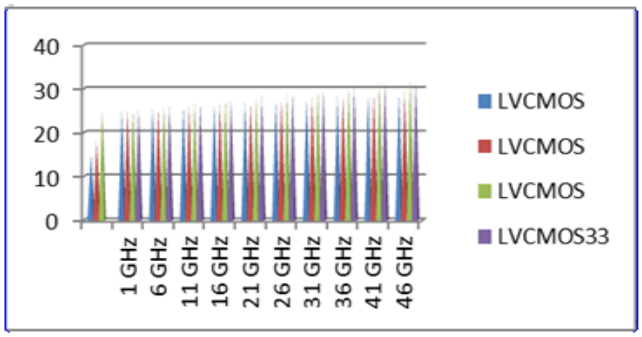

Figure 4. Junction Temperature of UART Using Different LVCMOS IO Standards.

4. Conclusion

The UART is being observed on different-different I/O Standard (LVCMOS). From above analysis, it is observed that changing IO Standard does not have much effect on leakage which is a static power but it is having a significant effect on dynamic power (IO power + Clock power) So we can conclude that there occurs the reduction in total power (Static + Dynamic Power) consumption (Figure 3.) and Junction Temperature (Figure 4.) if we decrease the range of frequency from 46 GHZ to 1 GHZ and if we choose LVCMOS33 IO standard out of all the IO standards of LVCMOS logic family.

5. Future Scope

We implement this UART on 28-nm Airtex-7 FPGA. There is a scope to implement this UART on latest 28-nm Kintex-7 FPGA to make the most energy efficient UART. We can also take different frequency ranges other than being used such as Wi-Fi frequencies or frequencies in range of MHZ or GHZ to make more efficient design of UART.

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